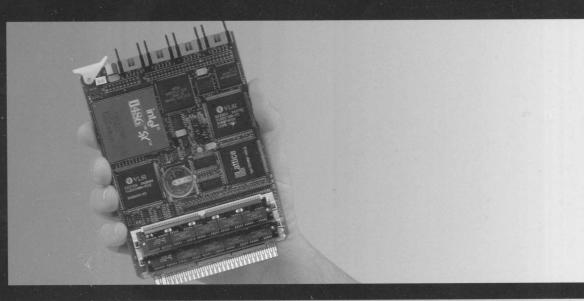
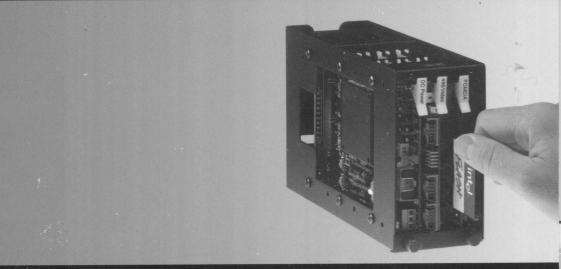
STD 3

Board and System Level Computer Products

Technical Data Book





McLaren Industrial MICS
Computer Sales Inc.

61 Keffer Circle Newmarket, ON L3X•1R8

TEL: (905) 898-7541 FAX: (905) 898-0506





More Than Products

While Ziatech's industrial computer products provide exceptional performance and reliability, Ziatech's Added Value program goes beyond products by providing a number of extraordinary services to Ziatech customers. These services speed project implementation at the outset and provide the security of continued support throughout the lifetime of the customer's project. The Added Value program includes:

- → A five-year warranty, with an optional extension to ten years (See the complete warranty in Appendix H.)
- The best technical support in the industry, available 12 hours a day. (Rated #1 for applications support in a Computer Design survey)
- → Professional training courses and a 24hour Bulletin Board Service
- **○** Lifetime sourcing
- Quick-turn repair service and customdesigned spare parts program

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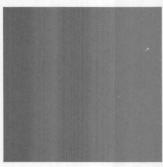
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Functional and Numeric Indices









Inside This Section

- Two ways to locate Ziatech products and services
- Also see the comprehensive subject index at the back of this publication

Functional and Numeric Indices





- * Two ways to locate Ziatech products and services
 - Also see the comprehensive subject index at the

Functional Index

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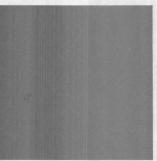
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About Ziatech/ New Products









Inside This Section 🕨

- Ziatech's commitment to innovation, reliability, and customer support
- Information on the latest products from Ziatech

About Ziatech

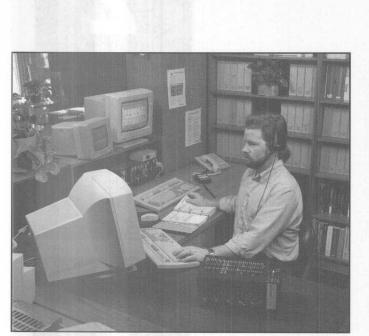


Engineers have relied on Ziatech's commitment to quality products and quality support services since 1976. This partnership with its customers has enabled Ziatech to become a technological and industry leader in control system engineering.

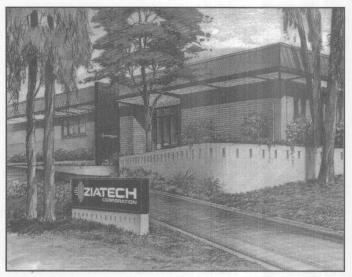
Technological Leadership

Ziatech incorporates new technologies into its products whenever they provide practical benefits to control system designers. STD 32, an extension of the STD Bus, employs EISA technology to provide 16- and 32-bit performance in a small industrial computer format.

Other Ziatech innovations include: the first use of surface mount technology on the STD Bus; the first implementation of multiple DOS-based processors that share peripherals across an STD 32 backplane; the first full, 32-bit processors on the STD Bus; and the first use of high-speed local bus video on the STD Bus.



Help is just a phone call away with Ziatech technical support engineers.



A new 60,000 square foot facility in San Luis Obispo, California houses west coast operations.

Reliable Products

Reliability is designed into each Ziatech product. A computer-based version of MIL-217E is used to calculate the Mean-Time-Between-Failure rates of existing Ziatech products and helps optimize the reliability of new designs. The use of highly integrated products, surface mount technology, and extensive burn-in and testing procedures enhances Ziatech product reliability.

Five-Year Warranty

Product manufactured by Ziatech are covered by a five-year warranty which can be extended to 10 years for added protection.

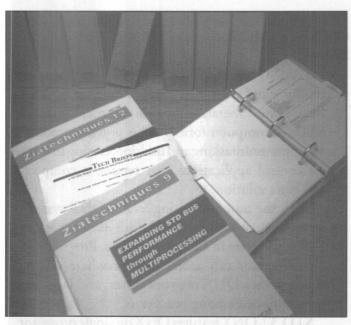


Technical Support

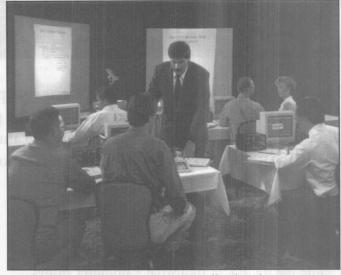
Ziatech's award-winning technical support team is on-line 12 hours every business day. Applications engineers at the California head-quarters and the Eastern regional office in Pennsylvania are ready to answer questions and help customers configure systems. From prepurchase advice to post-purchase technical support, Ziatech's technical support staff provides concise, timely assistance to Ziatech customers.

Bulletin Board Service

Ziatech's central Bulletin Board System (BBS) provides up-to-the-minute software updates, new product information, and 24-hour technical support. Customers are given VIP access, allowing them to leave messages for technical support personnel and to interact with other engineers who use Ziatech products. While customers are given special privileges, anyone with a 1200 or 2400 bps modem can access the general service by dialing (805) 541-8218.



Ziatech's product manuals and "How-To" literature simplify set up and configuration of Ziatech equipment.



The Systems Engineering Course offers hands-on training.

Systems Engineering Course

Hands-on, personalized training is what designers can expect from Ziatech's Systems Engineering Course. Offered three times a year, the course covers a variety of system-level topics and gives customers a unique opportunity to work with and learn from Ziatech engineers.

Easy-To-Use Documentation

All Ziatech product manuals are carefully organized and feature "Getting Started" sections that simplify set up and configuration of the product. Subject indexes in every manual make finding answers simple.

Detailed Application Literature

Ziatech publishes a library of "help literature" which answers specific application questions. Application notes explore the technical aspects of a variety of system configurations.

Ziatech Technical Briefs are written by Ziatech technical support engineers and offer concise answers to commonly asked technical questions. See Appendix A in this data book for a complete list of Tech Briefs and Application Notes.

New Products:



Ziatech continually develops new products that put the latest technologies to work in embedded and industrial control applications. The following products have appeared since the publication of the last data book, or have been upgraded significantly to warrant mention here. Data sheets for most of these new products are included in this publication. If you are interested in a product not included in this data book, please contact Ziatech.

New Systems Products

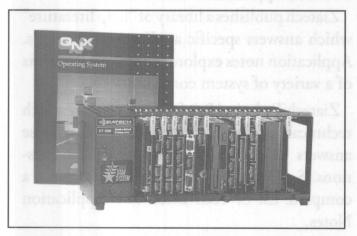
Compact, Industrial Computer

The microCATTM Industrial Computer brings together several one-slot, space-saving peripherals in a single system. The configuration pictured on this page includes a single board 486 computer and a 32-bit local bus Super VGA/Flat Panel Display

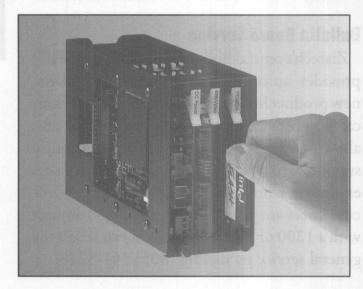


interface sharing a single slot, a PCMCIA interface, and a removable, single-slot DC to DC power supply.

The entire system measures just 2.8 x 5.2 x 8.5 inches and is housed in a 3-slot STD 32 card cage. System designers can configure their own small system using products from Ziatech and other STD 32 manufacturers. Product choices include single board computers, one-slot floppy and hard drives, PCMCIA 2.0 interfaces, network, modem and other communications cards, and a variety of STD 32 enclosures. *Call Ziatech for more information*.



STAR-QNX combines the multitasking QNX operating system with Ziatech's multiprocessing STAR SYSTEM.



The microCAT is ideal for limited-space applications.

QNX-based Multitasking and Multiprocessing Systems

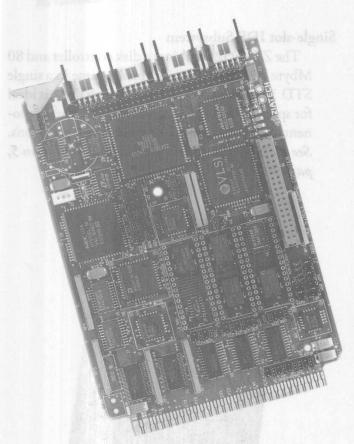
STAR-QNX and STD 32-QNX bring the multitasking and networking capabilities of the QNX Real-Time Operating System to the industrial STD 32 computer format. This potent combination puts multitasking and multiprocessing to work on control applications that require a compact, real-time solution.

With the multiprocessing STAR-QNX system, up to seven processors—each with its own copy of QNX—operate in a single card cage. Programs on any processor can access files anywhere on the network via a QNX network driver, and tasks can be partitioned among processors.

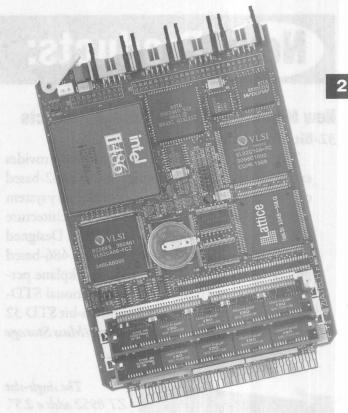
STD 32-QNX features QNX on single processor STD 32 systems. See the STD Bus Software Section 13, pages 13-35 and 13-39.

New Low Temperature (LT) Products

Three products are available in low temperature (LT) versions for the first time: the ZT 89LT02 Single Board 486 Computer, the ZT 89LT11 Scalable Processor Board (a full 32-bit 486 processor board), and the ZT 89LT21 PCMCIA 2.0 Interface. These products utilize CMOS components, which consume less power than TTL products, and operate in a temperature range of -40° to +65° Celsius. All of Ziatech's LT products are compatible with TTL-based STD and STD 32 computer products. See the "CT" and "LT" Products Section 17, page 17-1 for a complete list of Ziatech LT (Low Temperature) and CT (CMOS, TTL-compatible products.



The ZT 8802 combines economical performance with a variety of I/O capabilities.



The ZT 89LT02 combines 486 processor performance and low temperature operation.

New Processors

Ziatech's processor cards and single board computers range from the economical 8088 to the powerful 66 MHz 486DX2, with a low-cost 386 computer due in the second half of 1994 and a Pentium-based design scheduled for introduction in early 1995.

Single Board V40 Computer

The latest Ziatech single board computer, the ZT 8802, provides, a DOS-compatible STD 32 processor with versatile I/O for cost-conscious control applications. The ZT 8802 contains an NEC V40 processor, which is code-compatible with the Intel 8088, and features an interrupt controller, three counter/timers, and a serial channel integrated into the core processor. Two additional serial ports, 48 points of digital I/O, an SBX expansion module connector, 512 Kbytes of EPROM/flash, and up to 1 Mbyte of RAM round out the ZT 8802 feature set.

This new single board computer supports both DOS and non-DOS environments, and is available in a CT version with an extended temperature range from -40° to +85° Celsius. See the STD Bus Computers Section 3, page 3-7.

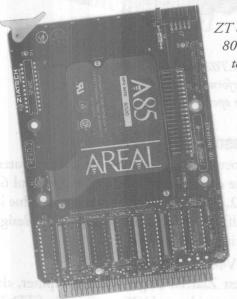
New Products:



New Memory and Mass Storage Products

32-Bit Memory System

The ZT 8920 32-Bit Memory System provides extended memory capabilities to STD 32-based computers. The versatile single slot memory system accommodates full 32-bit Extended Architecture (EA) data transfers over the STD 32 Bus. Designed primarily to support high-end 386- and 486-based processors, the ZT 8920 increases backplane performance up to 16 times that of traditional STD-80 designs. It also supports 8-, and 16-bit STD 32 processors. See the STD Bus Memory/Mass Storage Section 5, page 5-7.

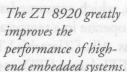


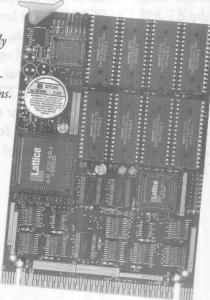
The single-slot ZT 8952 adds a 2.5", 80 Mbyte hard drive to STD 32 systems.

Two New SCSI-2 Controllers

Improved peripheral performance comes to STD 32 computers with the advent of two new SCSI-2 controllers. The ZT 8955 provides one 8-bit SCSI-2 channel, and provides 8- or 16-bit performance over the STD 32 system backplane. Full 32-bit performance is available with the RISC-based ZT 8956, which provides one 16-bit or two 8-bit SCSI-2 channels.

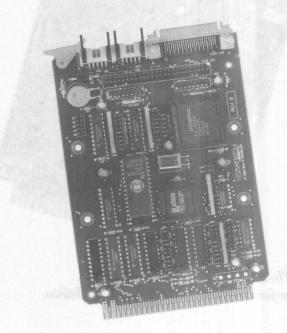
The Adaptec-compatible interfaces can use the many software packages written for this standard. Both interfaces allow an STD 32-based computer to simultaneously support up to seven SCSI-2 peripherals. See the STD Bus Memory/Mass Storage Section 5, pages 5-21 and 5-23.





Single-slot IDE Subsystem

The ZT 8952 combines a disk controller and 80 Mbyte IDE hard drive for the first time in a single STD 32 enclosure slot. The 2.5-inch drive is ideal for space critical applications, and is a key component of most microCAT computer configurations. See the STD Bus Memory/Mass Storage Section 5, page 5-17.

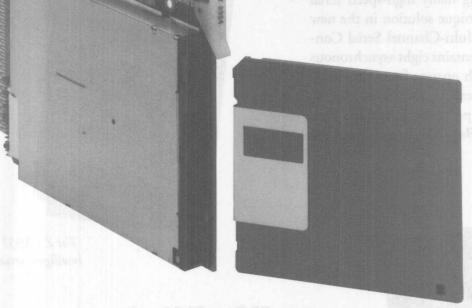


The ZT 8955 provides SCSI-2 capabilities and performance to STD 32 systems.

The single-slot, low-profile ZT 8954 microfloppy drive fits in a single STD 32 slot.



The ZT 8954 integrates a controller and a half-inch high, 1.44 Mbyte Slimline floppy drive into a single STD 32 slot. It is intended for use with STD 32 processors that have built-in Direct Memory Access (DMA) capability, and supports all floppy disk formats. See the STD Bus Memory/Mass Storage Section 5, page 5-19.



New Video Interfaces

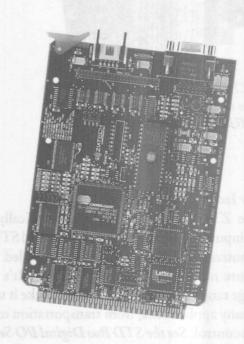
Super VGA/FPD and Keyboard Interface

This new STD 32 interface provides 8- and 16-bit Super VGA and keyboard I/O to STD 32 systems, supporting most monochrome and color CRT monitors and flat panel displays. The ZT 8982 also features video select circuitry which enables up to eight interfaces to share a single monitor and keyboard in an STD 32 system. See the STD Bus Video I/O Section 6, page 6-7.

Local Bus Video Interface

The latest 32-bit local bus interface from Ziatech provides the same Super VGA and flat panel support found on the ZT 8982 STD 32 card, but in a module that connects directly to the ZT 8902 Single Board 486 Computer. Together, the single board computer and the zVID2 local bus video interface require but a single slot, and boost graphics performance up to ten times that of backplane video solutions. See the STD Bus Computers Section 3, page 3-23.

The new ZT 8982 provides high-performance SVGA operation of CRTs and flat panel displays.



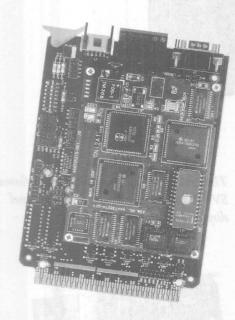
New Products:



New Industrial Interfaces

Intelligent Serial Controller

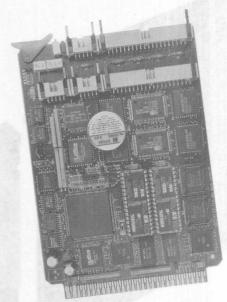
Applications requiring many high-speed serial channels now have a unique solution in the new ZT 8932 Intelligent, Multi-Channel Serial Controller. The ZT 8932 contains eight asynchronous RS-232 channels, which operate faster than conventional serial ports thanks to the ZT 8932's onboard 16-bit NEC V53 processor, RAM, and flash memory. See the STD Bus I/O Control Processors Section 4, page 4-15.



The ZT 88CT93 connects STD 32 systems to PLCs and a variety of GENIUS I/O network modules.

Optically Isolated Industrial I/O interface

The ZT 88CT73 provides eight optically isolated inputs and eight outputs for industrial STD 32 computers, and operates over an extended temperature range of -40° to +85° Celsius. It's wide voltage range and current capacities make it useful for many applications, from transportation to machine control. See the STD Bus Digital I/O Section 9, page 9-21.

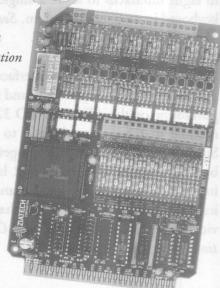


The ZT 8932 high-speed intelligent serial interface.

GE Fanuc PLC Interface

The ZT 88CT93 STDIM (STD Interface Module) connects STD 32 computers to PLCs, remote I/O, and other computers on the GE Fanuc GeniusTM I/O network. This new interface allows control system designers to integrate small STD 32 computers into a PLC environment. See the STD Bus Network I/O Section 8, page 8-3.

The ZT 88CT73 offers optical isolation for inputs and outputs.



Enclosures

Ziatech's newest card cages combine rugged construction, STD 32 backplanes and removable power supply modules. Designed for harsh environments where shock and vibration, temperature extremes, and electrical noise are present, the ZT 210 card cages are available in 9-, 12-, 15-, 18- and 21-slot widths using STD 32 backplanes that support 8-, 16- and 32-bit data transfers.

The ZT 210's power supply modules can be easily removed or replaced for quick servicing or adapting the system to changing power requirements.

Another new enclosure, the ZT 220, provides a compact, open frame card cage for applications that require just a few STD 32 or STD cards, and don't require multiprocessing. See the STD 32 Enclosures Section 14, pages 14-17 and 14-31.



Ziatech's new ZT 210 Series card cages feature rugged construction and removable power supply modules for use with limited-space applications



NVAS, Ziatech's Network Variable Access Software is now available for use in the Windows operating environment.

New Software

LONWORKSTM WindowsTM Support

New Network Variable Access Software (NVAS) for Windows provides Windows applications with access to network variables on LONWORKS Control Networks. This allows system designers to quickly and easily integrate a PC or STD 32 system into Windows-based LONWORKS network. See the LONWORKS Control Network Products Section 16, pages 16-9 and 16-11.

IEEE 488 Interfaces Software Drivers

New device drivers make it easier to integrate PC and STD interfaces into OS/2 and Windows-based IEEE 488 systems. WIN.488, part of Ziatech's simple to use EZ.488 software package, provides a driver to help integrate GPIB hardware interfaces into Windows environments. OS2.488 provides similar support for OS/2-based STD 32 or PC systems. See the IEEE 488 Products Section 20, pages 20-17, and 20-19.

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Zianech e newest card cages combineratyged construcción. STD 32 backplanes and removable power supply modales. Designed for harsh environments where shock and vibration, remperature extremes, and electrical noise are present, the ZT 210 card cages are available in 9-, 12-, 15-, 18- and 21-slot widths asing STD 32 backplanes that support 8-, video and 31-bit data transfers.

The 2.7.210's hower supply modules can be easily removed or replaced for quick servicing or adaption the system to changing power requirements.

Another new enclosure, the ZT 220, provides a compact, spen frame card cage for applications that country intra few STD 32 or STD cards, and don't require multiprocessing. See the STD 32 Enclosures Service 14, pages 14-17 and 14-31.



N. 2. Zamech's Nemunk Varieble Arrest Software is now available for use in the Whalour operating ownsament.



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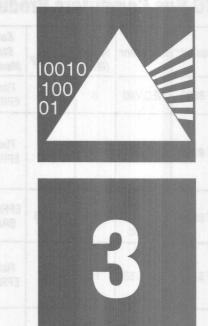
LONWORGTM Windows M Support

New Network Variable Act on oftware (NVAS) for Windows provides Window applications with access to network variables of a NW ORES Control Networks, This allows com designers to quickly and easily integrate a PortSTD 32 system into Windows-based LONV. All network. Service the LONW ORES Control Network of Products Section 16, pages 16-9 and 16-11.

IEEE 468 Interfaces Software Living

New device drivers make it make to integrate Pond STD interfaces and OSA Windows-based HEE 488 systems. Wilsl. 60 part of Ziareco sample to use EZ 488 software or deute provides driver to help integrated TPG hardware interfaction. Windows environments. OS2 488 provides similar support for OS/2-box a STO 32 or Postems. See that IEEE 488 in valuer Section 215 pages 20-17, and 20-18.

STD Bus Computers





Most of Ziatech's industrial computer products are based on the STD 32 and STD Bus standards. For a complete description of the STD 32 Bus architecture, including a "short form" specification, see

Appendix D of this publication.

STD Bus Computers Product Feature Guide

Product*	Processor	CPU Speed (MHz)	RAM Capacity	Solid State Memory	Serial Port(s)	Printer Port(s)	Parallel lines	Other I/O	Counter/ Timer	Bus Data Width	Multi- processor	Interrupts	Ext. Temp
ZT 8801	NEC V40	8	1 MB	Flash/ EPROM	(1)V40 RS-232/485	No	48	SBX	3 16-bit	8	No	8	+
ZT 8802	NEC V40	8	1 MB	Flash/ EPROM	(1)V40 RS-232 (2)COM RS-232	No	48	SBX	3 16-bit	8	No	8	•
ZT 8809A	NEC V20/ Intel 80C88	8	640 KB	EPROM/ BRAM	(2)COM RS-232/485	Yes			3 16-bit	8	No	8	*
ZT 8901	NEC V53	16	1 MB	Flash/ EPROM	(2)COM RS-232/485 1-V53 RS-232	No	48	SBX	3 16-bit	8/16°	Yes	8	*
ZT 8902	80486 SX/DX/ DX2	25/33/ 50/66	16 MB	Flash	(2)COM RS-232 DTE only	Yes	24	Local Bus	6 16-bit	8/16	Yes	15	٠
ZT 8911	80486 SX/DX/ DX2	33/66	128 MB	Flash	(2)COM RS-232	Yes	24	LED Display, Speaker	8 16-bit	8/16/ 32 •	Yes; Includes Arbiter and Memory	15	•

[◆] Feature included or available ▲ Accepts future generation processors via CPU expansion modules

Also Inside This Section

- zVID2 Local Bus Super VGA/FPD Adapter
- Application Specific Automation Processor (ASAP™)

[•] Requires an STD 32 backplane for data transfers greater than 8 bits

^{*} Note: All CPUs include power-fail detection

ZT 8801

Single Board V40 Computer

A low-cost, highly integrated, single board STD Bus computer with versatile I/O.

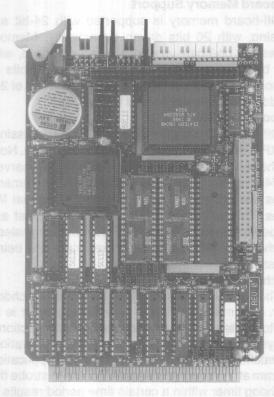
The ZT 8801 is a low-cost STD Bus computer with a unique combination of I/O ideal for embedded control applications. The NEC V40 processor is code-compatible with the Intel 8088 CPU and features an interrupt controller, three counter/timers, and a serial channel integrated with the core processor.

The serial channel on the ZT 8801 is configurable to RS-232 or RS-485 standards and is complemented on-board by up to 48 points of digital I/O, an SBX

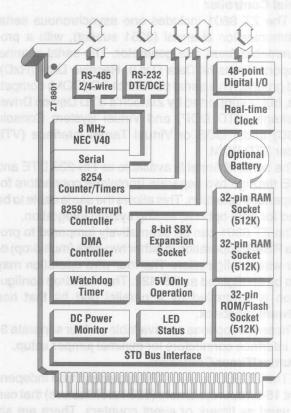
expansion module connector, and up to 512 Kbytes EPROM/flash, and 1 Mbyte of RAM.

The ZT 8801 is supported by Ziatech's STD DOS and STD ROM software environments. Common I/O software support is provided by Ziatech's STD Device Driver Package (STD DDP).

The ZT 88CT01 offers the same features as the ZT 8801, but combines low power consumption with an extended operating range -40° to +85° Celsius.



- STD 32- and STD-compatible
- 48 points digital I/O (ZT 16C49)
- · Eight points of event sense
- NEC V40 processor (8088 code-compatible)
- 8 MHz operation
- DMA controller (71071)
- Interrupt controller (8259)
- Three counter/timers (8254)
- RS-232/485/422 serial channel (8251)
- SBX expansion module connector



- Up to 1 Mbyte RAM and 512K EPROM or flash EPROM
- Optional battery for RAM and real-time clock
- Watchdog timer (DS 1232)
- Real-time clock (DS 1202) with scratch pad RAM
- Backplane cascade interrupt support
- +5V-only operation (+12V required for flash programming)
- ZT 88CT01 option for -40° C to +85°C operation

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40 $^{\circ}$ to +85 $^{\circ}$ C. (Users should make adjustments for temperature rise in enclosures.)



Functional Considerations NEC V40 Processor

The NEC V40 is a highly integrated microprocessor featuring an 8088-compatible CPU and many standard I/O devices. The 8088-compatible V40 CPU executes all code written for the 8088/8086 family of microprocessors. In addition, its instruction set includes string I/O, expanded rotate and shift, and bit and nibble manipulation.

The standard I/O devices found in the V40 include an interrupt controller (8259A-compatible), three counter/timers (8254-compatible), and a serial controller (8251A-compatible).

The V40 is fabricated with CMOS technology to provide an increase in both temperature range and noise immunity, with a reduction in power consumption.

Serial Controller

The ZT 8801 includes one asynchronous serial communication channel (8251 subset), with a programmable baud rate generator. The serial channel supports Transmit Data (TxD), Receive Data (RxD), and ground. This serial port is not PC (COM) compatible, but is supported by Ziatech's STD Device Driver Package (STD DDP) and Virtual System Console (VSC) under DOS or Virtual Target Interface (VTI) under STD ROM.

The serial channel is available as RS-232 DTE and DCE through two separate frontplane connectors for jumperless selection. This allows the same cable to be used for both options, easing system integration.

The ZT 8801 can be alternatively jumpered to provide RS-485 operation in either two-wire (multidrop) or four-wire configuration. The four-wire operation may also be configured as RS-422. The multidrop configuration is controlled by a parallel port bit that has software readback.

These four options are available on four separate 3pin interface connectors for minimal jumper setup.

Counter/Timer Controller

The ZT 8801's V40 CPU provides three independent 16-bit counter/timers (8254 architecture) that can be used as timers or event counters. There are six programmable counter/timer modes: interrupt on end of count, frequency divider, square wave generator, software triggered, hardware triggered, and retriggerable one-shot. One of the counter/timers is available through a frontplane connector to be used as required by the application. The other two counter/timers can be used for baud rate generation for the V40 serial channel, and for interrupt generation for timed and periodic interrupts.

Parallel I/O (ZT 16C49)

The ZT 16C49 ASIC provides 48 points of parallel I/O with eight points of event sense operation. The

I/O is configured as six 8-bit ports, with each point configurable as an input or output. The outputs each sink 12mA and are non-glitching on power up. Eight of these points can be used on-board, leaving 40 bits of external I/O. The eight internal signals may be alternately used for parallel I/O, leaving the board in a default state that provides the most capability. Interfacing to Opto 22-compatible I/O modules is available through optional cabling.

Local Memory Support

The ZT 8801 is populated with three 32-pin memory sockets dedicated for use by the V40 microprocessor. One socket supports up to 512 Kbytes of EPROM. The two RAM sockets each support 128 Kbyte or 512 Kbyte RAMs. Each RAM socket has an optional battery backup. The EPROM socket supports +5V Flash, with an option for +12V Flash Memory.

Off-board Memory Support

Off-board memory is supported with 24-bit addressing, with 20 bits driven dynamically. Memory ranges not on-board are considered off-board, with STD bus cycles performed. The upper four bits of memory address are driven low to allow the use of 24-bit addressed memory boards (STD 32®).

Off-board I/O Support

Off-board I/O is supported by full 16-bit addressing. IOEXP is driven low in the range FC00 to FFFFh. Note that the very top I/O space (FFF0 to FFFFh) is reserved for V40 configuration (*See Figure 1*). No command cycles are driven on the backplane for internal I/O cycles. This will prevent 8- or 10-bit cards that are mapped between FC00 and FFFFh from being selected when the V40 configuration registers are being accessed.

Watchdog Timer

The ZT 8801 includes a single-stage watchdog timer. The main function of a watchdog timer is to monitor system operation and take corrective action if the system fails to operate as designed. In operation, the watchdog timer must be strobed by the application program at a predetermined rate. Failure to strobe the watchdog timer within a certain time period results in the ZT 8801/88CT01 being reset. The watchdog timer is enabled through jumper selection. The time period is selectable between nominal values of 150ms, 600ms, and 1.2 seconds.

Reset Operation

The ZT 8801 includes a precision DC power monitor with a 4.7V $_{\rm CC}$ trip point. During power-on, the power monitor holds the ZT 8801 in reset until a minimum of 250ms and a maximum of 1000ms after V $_{\rm CC}$ reaches the trip point. At this point the local CPU is free to operate. The ZT 8801 holds the STD Bus in reset until after it is out of local reset. The ZT 8801 also include a push-button reset that will cause a system SYSRESET*.

Low Power/Extended Temperature

The ZT 88CT01 is designed and tested for -40° to +85° Celsius operation in harsh environments. This product is designed for use in conjunction with Ziatech's other LT (low temperature) and CT (CMOS, TTL-backplane-compatible) products for mobile and outdoor applications.

SBX Expansion Module Connector

The SBX expansion module connector provides an alternative to expanding the I/O capabilities of the ZT 8801 through the STD Bus. The SBX interface is electrically, mechanically, and functionally equivalent to the IEEE 959-1988 specification developed by Intel. This makes available hundreds of off-the-shelf I/O modules.

	TV/ enchelotion	
FFF0-FFFF	V40 Configuration	IOEXP
FC00-FFEF	STD Bus	driven low
FB80-FBFF	SBX 1 Chip S.	schossepak
FB00-FB7F	SBX 0 Chip S.	Cables (se aT 90061
FA80-FAFF	RTC	2T 901S
FA00-FA7F	Parallel ASIC	
00E0-F9FF	STD Bus	sion. See the Data Book
00D0-00DF	DMA Controller	software mapped
00C0-00CF	STD Bus	
00B0-00BF	V40 Serial Port	software mapped
0050-00AF	STD Bus	
0040-004F	Counter/Timers	software mapped
0030-003F	STD Bus	
0020-002F	Interrupt Controller	software mapped
0000-001F	STD Bus	
all addresses shown in hex		

Figure 1. ZT 8801 Local I/O Map

Real-Time Clock

The real-time clock provides timekeeping/calendar functions as well as 24 battery-backed bytes of RAM. The real-time clock provides seconds, minutes, hours, day, date, month, and year information. The end-of-month date is automatically adjusted for months less than 31 days, including leap-year correction. Both 12-hour and 24-hour modes are supported with an AM/PM indicator.

Specifications

Electrical

• STD 32 (SA8) and STD-80 (8 MHz) compatible

Power Req.	Min.	Тур.	<i>Max.</i> 5.25V	
Supply Voltage, Vcc	4.75V	5.00V		
Supply Current, V _{CC} =5.0V (with 512Kbyte ROM, 1Mbyte RAM) (ZT 8801) (ZT 88CT01)	JUS conn bay, 1 Mby by, 1 Mby), MS-DC	620mA 430mA	1A 800mA	
Aux Voltage, V _{aux} Only needed for Flash programming.	11.4V	12V	12.6V	

Environmental	
Operating Temperature (ZT 8801) Operating Temperature (ZT 88CT01)	0° to 65° Celsius -40° to +85° Celsius
Storage Temperature (ZT 8801)	-45° to +85° Celsius
Storage Temperature (ZT 88CT01 with battery)	-40° to +100° Celsius
Storage Temperature (ZT 88CT01 without battery)	-55° to +105° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

Mechanical

- Size- and backplane-compatible with the STD 32 and STD-80 mechanical specifications
- Occupy one STD slot (0.625" or 15.90mm)
- Connectors
 - P1: STD 32 and STD Bus connector
 - J1: Interrupt interface (10-pin)
 - J2: Counter/Timer interface (10-pin)
 - J3: RS-485 4-wire transmit (3-pin)
- J4: RS-485 2-wire transceiver/4-wire receiver (3-pin)
 - J5: RS-232 DTE (3-pin)
 - J6: RS-232 DCE (3-pin)
 - J7: 48-point digital I/O interface (56-pin)
 - J8: 8-bit SBX interface (36-pin)



Dimensions:

4.5" (11.43cm) x 6.5" (16.51cm) x height Height from top surface: 0.38" (9.65mm) without battery

0.48" (12.12mm) with battery

1.10" (27.94mm) maximum with SBX module

Reliability

MTBF: 26 years

MTTR: five minutes (based on board replacement)

Ordering Information

The base configurations of the ZT 8801 and ZT88CT01 Single Board V40 Computers come without RAM, PROM, or BIOS and are ordered as ZT 8801-(or ZT 88CT01) P0R0S0.

The recommended DOS configuration, a ZT 8801 or a ZT 88CT01 Single Board V40 Computer (8MHz) with 128 Kbyte Flash Memory, 1 Mbyte static RAM installed (2 x 512 Kbyte chips), MS-DOS 5.0 and Ziatech's Industrial BIOS installed in flash memory, and a 1 amphour lithium (extended temperature) battery, is ordered as a ZT 8801- (or ZT 88CT01-) P1R4S1B.

ZT 8801	Single Board V40 Computer
ZT 88CT01	Single Board V40 Computer,
	extended temperature
ZT M8801	Single Board V40 Computer manu

Must choose one option from each category: PROM, ROM, and Flash EPROM Choices

PO No PROM

P1 256 Kbyte flash memory, 200ns 512 Kbyte ROM, 150ns*

*Note: The ZT 88CT01 is not available with choice P3.

RAM Choices

RO	No RAM
R1	128 Kbyte static RAM, 100ns
R2	256 Kbyte static RAM, 100ns
	(2 x 128 Kbyte chips)
R3	512 Kbyte static RAM, 120ns
R4	1 Mbyte static RAM, 120ns (2 x 512

Software Choices

	force Addings or brains a supported a cold a
SO	No software installed on board
S1	Microsoft MS-DOS and Ziatech's
	Industrial BIOS installed in flash
	memory. Requires options P1R2B
	or greater

Kbyte chips)

Miscellaneous Options

1 amp-hour lithium battery, extended temperature

Development Environments:

ZT 94001

STD DOS Development Environ-
ment. See Software Section for
more details. Includes Host devel-
opment disk containing VSC,
PROM PREP, Flash programs,
and other utilities. STD Device
Driver Package (STD DDP) with
support for STD 32 I/O cards and
peripherals, ZT 7502/00 BIOS di-
agnostic card, full MS-DOS, and a
serial cable (requires options
P1R3S1B or greater)

ZT 94002

STD ROM Development Environment. STD ROM development system for PROM-based target systems. Includes Virtual Terminal Interface (VTI), Paradigm LO-CATE, and startup modules, STD DDP, Paradigm DEBUG/RT, and serial cable (requires options P1R2 or greater)

Accessories

Cables (see Data Book cable section for details):

ZT 90069 3.3' (1m) serial cable, 3-pin to 25-pin female D-shell connector

ZT 90156 8" (20.3cm) printer interface cable, 56-pin connector to 25-pin female D-shell

Warranty - Five years with an optional five-year extension. See the full warranty statement in the Technical Data Book appendix. Batteries are not covered by Ziatech's warranty.





ZT 8802

Single Board V40 Computer

Highly integrated, single board, DOS-compatible STD Bus computer with versatile I/O

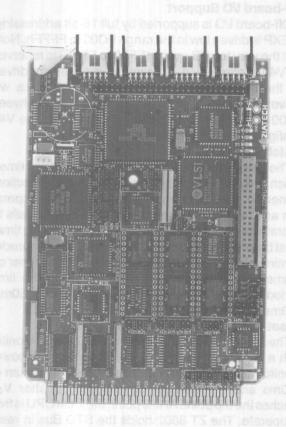
The ZT 8802 is a low-cost STD Bus computer with a generous complement of I/O for all applications. It uses the NEC V40 processor, which is code-compatible with the Intel 8088 CPU and features an interrupt controller, three counter/timers, and a serial channel integrated into the core processor. Two additional serial channels are available via 16450-compatible parts (IBM PC/AT® standard).

The three serial channels on the ZT 8802 are compatible with the RS-232-C standard and are complemented by 48 points of digital I/O, an SBX

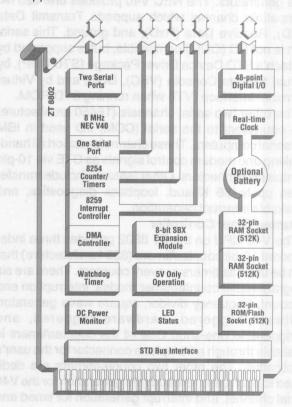
expansion module connector, 512 Kbytes of EPROM/ flash, and up to 1 Mbyte of RAM.

The ZT 8802 is supported by Ziatech's STD DOS and STD ROM software environments. Common I/O software support is provided by Ziatech's STD Device Driver Package (STD DDP).

The ZT 88CT02 is designed and tested for -40° to +85° Celsius operation in harsh environments. This product is designed for use in conjunction with Ziatech's other LT (low temperature) and CT (CMOS, TTL-backplane-compatible) products for mobile and outdoor applications.



- STD 32- and STD-compatible
 - 48 points of digital I/O (16C49)
- Eight points of event sense
- NEC V40 processor (8088 code-compatible)
- DMA controller (71071)
- Interrupt controller (8259)
- Three counter/timers (8254)
- Three serial channels (8251, 16450)



- SBX expansion module connector
- Up to 1 Mbyte RAM and 512 Kbyte ROM/flash
- · Optional battery for RAM and real-time clock
- Watchdog timer
- Real-time clock with scratch pad RAM
- Backplane cascaded interrupt support
- +5 volt-only operation (+12 volt required for flash programming)

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40 $^\circ$ to +85 $^\circ$ C. (Users should make adjustments for temperature rise in enclosures.)



Functional Considerations NEC V40 Processor

The NEC V40 is a highly integrated microprocessor featuring an 8088-compatible CPU and many standard I/O devices. The V40 CPU executes all code written for the 8088/8086 family of microprocessors. The chip's expanded instruction set also includes string I/O, rotate and shift instructions, and bit and nibble manipulation.

Standard I/O devices in the V40 include an interrupt controller (8259A-compatible), three counter/timers (8254-compatible), and a serial controller (8251A-compatible).

The V40 is manufactured with CMOS technology to provide an increase in both operating temperature range and noise immunity. CMOS fabrication also provides a reduction in power consumption.

Serial Controllers

The ZT 8802 includes three asynchronous serial communication channels, all with programmable baud rate generators. The NEC V40 provides one 8251A-compatible channel which supports Transmit Data (TxD), Receive Data (RxD), and ground. This serial port is not PC (COM) compatible, but is supported by Ziatech's STD Device Driver Package (STD DDP), by Virtual System Console (VSC), DOS, and by Virtual Terminal Interface (VTI) when running STD ROM.

The other two serial channels (16450 architecture) are equivalent to the serial (COM) I/O used in IBM personal computers. These channels support all handshaking and modem control signals as DTE via 10-pin frontplane connectors. Other features include transfer rates up to 56 Kbaud, loopback diagnostics, and maskable interrupt generation.

Counter/Timer Controller

The V40 CPU on the ZT 8802 provides three independent 16-bit counter/timers (8254 architecture) that can be used as timers or event counters. There are six programmable counter/timer modes: interrupt on end of count, frequency divider, square wave generator, software triggered, hardware triggered, and retriggerable one-shot. One of the counter/timers is available through a frontplane connector for the user's application. The other two counter/timers are dedicated to such uses as baud rate generation for the V40 serial channel, and interrupt generation for timed and periodic interrupts.

Parallel I/O (ZT 16C49)

The ZT 16C49 ASIC provides 48 points of parallel I/O with eight points of event sense I/O. The I/O is configured as six 8-bit ports, with each point configurable as an input or output. The outputs each sink 12mA and are non-glitching on power-up. Eight of these points are normally utilized on-board, leaving 40 bits of external I/O. On-board use can be disabled, making all 48 bits of parallel I/O available to the user. The 48 lines are available through a 56-pin connector. Accessory cables interface to one or two 24-position

I/O module mounting racks, such as Ziatech's ZT 2226 24-Channel I/O Mounting Rack or equivalent.

Local Memory Support

The ZT 8802 has three 32-pin memory sockets dedicated to the V40 microprocessor. One socket supports up to 512 Kbytes of EPROM. The remaining two sockets will support either 128 Kbyte or 512 Kbyte RAM chips for a maximum capacity of 1 Mbyte RAM. Each RAM socket can be individually battery backed. The EPROM socket supports +5V Flash memory, with an option for +12V Flash memory.

Off-board Memory Support

Off-board memory is supported with 24-bit addressing, with 20 bits driven dynamically. Memory ranges not on-board are considered off-board, with STD bus cycles performed. The upper four bits of memory address are driven low to allow the use of 24-bit addressed memory boards to be used (STD 32® feature).

Off-board I/O Support

Off-board I/O is supported by full 16-bit addressing. IOEXP is driven low in the range FC00 to FFFFh. Note that the very top I/O space (FFF0 to FFFF) is reserved for V40 configuration. No command cycles are driven on the backplane for internal I/O cycles. This will prevent 8- or 10-bit cards that are mapped between FC00 and FFFFh from being selected when the V40 configuration registers are being accessed.

Watchdog Timer

The ZT 8802 include a single-stage watchdog timer, which may be enabled through a jumper selection. Generally, the watchdog timer monitors system operation and takes corrective action if the system fails to operate as designed. In operation, the watchdog timer must be strobed by the application program at a predetermined rate. Failing to strobe the watchdog timer on a timely basis results in a ZT 8802 reset. The time period is selectable between nominal values of 150ms, 600ms, and 1.2 seconds.

Reset Operation

The ZT 8802 includes a precision DC power monitor with a 4.7V_{CC} trip point. During power-on, the power monitor holds the ZT 8802 in reset for a minimum of 250ms and a maximum of one second after V_{CC} reaches the trip point. At this point, the local CPU is free to operate. The ZT 8802 holds the STD Bus in reset until after they are out of local reset. It also includes a push-button reset that will cause a system SYSRESET*.

SBX Expansion Module Connector

The SBX expansion module connector provides an alternative to expanding the I/O capabilities of the ZT 8802 through the STD Bus. The SBX interface is electrically, mechanically, and functionally equivalent to the IEEE 959-1988 (MULTIMODULE) specification developed by Intel. Hundreds of off-the-shelf SBX I/O modules are available.

Real-Time Clock

The real-time clock provides timekeeping/calendar functions, as well as 24 battery-backed bytes of RAM (with optional battery). The real-time clock provides seconds, minutes, hours, day, month, and year information. The end-of-month date is automatically adjusted for months less than 31 days, including leap-year correction. Both 12-hour and 24-hour modes are supported with an AM/PM indicator.

Low Power/Extended Temperature

The ZT 88CT02 is designed and tested for -40° to +85° Celsius operation in harsh environments. This product is designed for use in conjunction with Ziatech's other LT (low temperature) and CT (CMOS, TTL-backplane-compatible) products for mobile and outdoor applications.

Software

Ziatech offers two software development systems for ZT 8802 applications: STD ROM and STD DOS. STD ROM allows users to develop ROM-based (non-DOS) STD applications on an IBM or compatible PC. The PC, which is connected to the STD system through a serial link, runs Paradigm's DEBUG/RT. This allows the designer to use high-level languages such as C and Assembly for system development.

The second development system, STD DOS, is the popular DOS operating system residing in flash memory on the ZT 8802. Applications can be developed much faster with STD DOS by programmers familiar with DOS. STD DOS includes support for many peripherals such as disks and video. It is supported by a large number of development tools such as editors, compilers, assemblers, and debuggers.

Specifications

Electrical

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, V _{CC} =5.0V (with 512Kbyte ROM, 1Mbyte RAM)		550mA	900mA
Aux Voltage, V _{aux}	11.4V	12.0V	12.6V

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 specifications.
- Occupies one STD slot (0.625" or 1.602cm spacing).
- Connectors

D4.	OTD OO	- IOTO	D	
P1:	SID 32	and SID	Bus	connector

- J1: Interrupt interface (10-pin)
- J2: Counter/timer interface (10-pin)
- J3: COM2 (10-pin)
- J4: COM1 (10-pin)
- J6: 48-point digital I/O interface (56-pin)
- J7: V40 serial port (3-pin)
- J8: 8-bit SBX interface (36-pin)

Environmental				
Operating Temperature	0° to 65° Celsius			
Storage Temperature (ZT 8802)	-40° to +85° Celsius			
Storage Temperature (ZT 88CT02 with battery)	-40° to +100° Celsius			
Storage Temperature (ZT 88CT02 without battery)	-50° to +105° Celsius			
Non-Condensing Relative Humidity	less than 95% at 40° Celsius			

STD 32 Compliance Levels

• Permanent Master: SA8-I, ICA, MB

Note: SA8 is equivalent to STD-80 Series Rev. 2.3

(5 and 8 MHz)

Reliability

MTBF: 30 years

MTTR: five minutes (based on board replacement)

Ordering Information

The base configuration of the ZT 8802 (or ZT 88CT02) Single Board V40 Computer does not include RAM, PROM, or BIOS, and is ordered as: ZT 8802 (or ZT 88CT02) -P0R0S0.

The recommended DOS configuration is a ZT 8802 (or ZT 88CT02) Single Board V40 Computer (8 MHz) with 256 Kbytes Flash memory, 1 Mbyte static RAM installed, MS-DOS 5.0 and Ziatech's Industrial BIOS installed in flash memory, and a lithium battery, and is ordered as: ZT 8802 (or ZT 88CT02)-P1R4S1B.

ZT 8802 Single Board V40 Computer
ZT 88CT02 Single Board V40 Computer,
extended temperature

ZT M8802 Single Board V40 Computer manual

Must choose one option from each category:

PROM and flash EPROM Options:
P0 No PROM

P1 256 Kbyte flash memory

P2 512 Kbyte ROM

RAM Options (all extended temperature):

RO No RAM

R1 128 Kbyte static RAM

R2 256 Kbyte static RAM

R3 512 Kbyte static RAM

R4 1 Mbyte static RAM

Software Options:

SO No software installed on board

S1 Microsoft MS-DOS and Ziatech's Industrial
BIOS installed on board (requires options
P1R2B or greater)



Miscellaneous Options:

B 1 amp-hour lithium battery, extended temperature

Development Environments

Either STD DOS or STD ROM are required with initial system purchase. Manuals for hardware are free with the purchase of a STD DOS or STD ROM development environment.

ZT 94028

STD DOS Development Environment; Includes host development disk containing VSC, PROMPREP, FLASH, and other utilities. Also includes STD Device Driver Package (STD DDP) with support for STD 32 I/O cards and peripherals, ZT 7502/00 BIOS diagnostic card, full MS-DOS, and two serial cables (requires options P1R3S1B or greater)

ZT 94029

STD ROM Development Environment; STD ROM development system for PROM-based target systems. Includes Virtual Terminal Interface (VTI) installed on PROM, Paradigm LOCATE and startup modules, STD DDP, Paradigm DEBUG/RT, and two serial cables (requires options P1R2 or greater)

Accessories

Cables (see Data Book cable section for details):

ZT 90069 40" (1m), serial cable, 3-pin to

25-pin female D-shell

ZT 90089 40" (1m), digital I/O cable,

56-pin both ends

ZT 90136 40" (1m), serial cable, 10-pin to

9-pin male D-shell

ZT 90156 8" (20.3cm), printer interface cable,

56-pin to 25-pin female D-shell

Boards (see separate data sheet for details):

ZT 2223 Industrial I/O Adapter Board
ZT 2225 Industrial I/O Cable Adapter
ZT 2226 24-Channel I/O Mounting Rack

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix. Batteries are not covered by Ziatech's warranty.

ZT 8809A

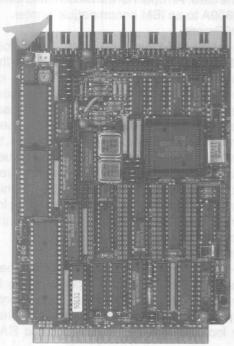
Single Board V20 Computer

Highly-integrated STD Bus V20 single board computer for use with DOS or PROM-based software

The ZT 8809A is a single board STD Bus computer that utilizes the NEC V20, a superset of Intel's 8088.

The ZT 8809A contains IBM PC/XT peripheral devices such as three 16-bit counter/timers, an interrupt controller, two PC-compatible serial ports (COM1 and COM2), and a Centronics printer interface (LPT1). The single board computer contains a wait state generator and can accommodate up to 640 Kbytes of RAM and 512 Kbytes EPROM.

For applications that require improved computational performance, an optional 8087 math coprocessor can be added via Ziatech's zSBX 337 module.

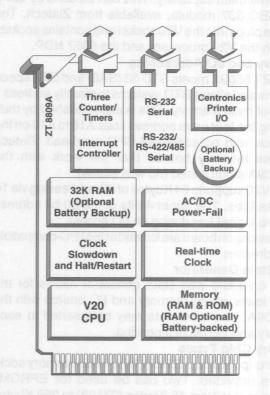


- 8 MHz V20 or optional 80C88 microprocessor
- · 8087 math coprocessor option
- Three 16-bit counter/timers (8254)
- Interrupt controller (8259A)
- · Wait state generator
- Real-time clock (DS1215)
- · 32 Kbytes of static RAM
- Optional memory of up to 640 Kbytes RAM and 512 Kbytes EPROM
- Two PC-compatible serial ports: one RS-232; one RS-232 or RS-422A/485

The ZT 8809A is supported by STD DOS, Ziatech's implementation of Microsoft® MS-DOS® on the STD Bus, enabling STD Bus systems to execute PC-compatible software and development tools.

The ZT 8809A is also supported by STD ROM, Ziatech's software development environment for ROM-based (non-DOS) systems.

The ZT 88CT09A version is available for low power and extended temperature (-40° to +85° C) operation.



- Centronics printer I/O port (PC-compatible)
- AC/DC power-fail protection with interrupt
- Optional battery backup for real-time clock and all RAM
- Direct 20-bit addressing of 1 Mbyte memory
- Extensive development system support
- Available with STD DOS or STD ROM
- ZT 88CT09A for extended temperature operation
- Burned-in at 55° C and tested to guarantee reliability

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40 $^{\circ}$ to +85 $^{\circ}$ C. (Users should make adjustments for temperature rises in enclosures.)



Functional Considerations NEC V20 Processor

The NEC V20 processor is a CMOS superset of the Intel 8088 processor. It is capable of executing the entire 8088 instruction set plus additional instructions for bit processing, packed BCD operations, and high-speed multiplication and division operations. The microprocessor resides in a 40-pin DIP socket to allow 8088 emulators to be used if desired. For further information on the V20, refer to the NEC Microcomputer Products Data Book, Volume 2.

The ZT 8809A is available in an extended temperature version, the ZT 88CT09A, which utilizes the 80C88 processor. The ZT 88CT09A is designed with low power and wide temperature range components for harsh environments.

The Intel 8087 Numeric Data Processor (NDP) can be added to the ZT 8809A for applications that require additional math capability. This can be done by using the zSBC 337 module, available from Ziatech. The module plugs into the V20 socket and contains sockets for both the V20 processor and the 8087 NDP.

Memory and I/O Addressing

The ZT 8809A meets STD 32 (SA8) and STD specifications and allows STD systems to directly address 1 Mbyte of main memory. This is accomplished by multiplexing the four extra address lines A16 to A19 on the data bus with no additional CPU overhead. Ziatech supplies memory boards that will work with the ZT 8809A at full speed (no wait states).

The V20 supports 64 Kbytes of I/O addressing via 16 address lines. The upper 4 bits of the 20-bit address field are logical low during an I/O access.

All devices on board are located at IBM PC-compatible I/O addresses.

Wait State Generator

The on-board wait state generator allows for the use of lower speed memory and I/O boards with the ZT 8809A. One wait state may be inserted in each memory and I/O cycle if needed.

Memory Chip Types

Four unpopulated, 32-pin, byte-wide memory sockets are provided. Two can be used for EPROMs ranging in size from 16 Kbytes (27128) to 256 Kbytes (27020), and are addressed at the top end of the 1 Mbyte memory address space. Either an STD ROM or STD DOS PROM occupies one of these EPROM sockets during development. The remaining two sockets can be used for static RAMs ranging in size from 32 to 512 Kbytes, and are addressed at the bottom of the memory address space. One of the two EPROM sockets may be used for RAM contiguous with the RAM in the other two sockets. Each pair of sockets can be optionally disabled to allow for the use of additional memory boards.

The ZT 8809A includes an additional 32 Kbytes of static RAM that is not socketed. Ziatech's STD DOS system stores important system configuration data in this memory. Battery backup is optional.

Serial I/O

Two 16450-compatible serial ports are provided. (The 16450 is a faster version of the 8250 used in the IBM PC/XT.) Each serial port is programmable for a baud rate of 50 to 56,000 baud. One serial port is RS-232 compatible (DCE or DTE), and the other may be configured as either RS-232 or RS-422A/485. All serial line drivers are included on board, and each port is accessed via a 14-pin connector at the front of the card.

Parallel I/O

The ZT 8809A also contains a parallel interface that can be used to drive a Centronics or compatible printer. The interface consists of eight I/O data lines plus four additional I/O signals, four inputs, and an interrupt/input signal.

All signals are available via a 20-pin connector on the front of the card. An optional transition cable connects the ZT 8809A to an IBM or compatible printer.

Counter/Timers

An on-board 8254 provides three 16-bit counter/ timers. Each of these is independently software-programmable to one of six modes. Some of the possible uses for these timers include event counter, real-time clock, digital one-shot, rate generator, square wave generator, and complex waveform generator. Each timer may be clocked by the on-board 1.19318 MHz oscillator (which is a DOS-compatible frequency), or from an off-board source. Each may generate an interrupt to the on-board interrupt controller; this is a jumper-selectable option. The gate inputs, clock inputs, and interrupt outputs are brought to a 10-pin connector at the front of the card.

Real-Time Clock

A real-time clock (RTC), with optional battery backup, is available on the ZT 8809A. It occupies no I/O or memory address spaces; however, it communicates with the processor via a serial bit-stream and shares a memory location with the 32 Kbyte static RAM on board.

Either the RTC or the RAM is enabled, based on the serial information the RTC receives. The RTC provides time in milliseconds, seconds, minutes, and hours, and provides the date in days, months, and years.

Interrupt Controller

The 8259A interrupt controller supports up to eight levels of programmably-prioritized interrupts and is expandable to 64 levels. The interrupt modes are also programmable. All sources of on-board interrupts are handled by the 8259A but can be optionally jumpered to off-board interrupt sources. One backplane interrupt input plus five frontplane interrupt inputs can be used.

Additional "slave" 8259A interrupt controllers can be added via the STD Bus, and an off-board "master" 8259A can be used in place of the one on board. **AC/DC Power-Fail Detection**

AC and DC power-fail detection is provided via a precise temperature-compensated reference circuit to ensure reliable battery-backed operation. (Battery backup is optional.) The AC power is sensed via an optional AC transformer. When AC power is determined to be failing, an early warning is sent to the processor via a non-maskable interrupt request (NMIRQ*). Then when the DC power drops below 4.75V, a reset is sent to the processor.

Optional Battery Backup

Battery backup, in conjunction with the AC/DC powerfail detection, can be ordered for the RAM sockets plus the 32 Kbyte static RAM and real-time clock (RTC). This optional 1 amp-hour lithium battery provides reliable data retention of ten years, typically, when only the 32 Kbyte RAM and RTC are battery-backed.

Software

Ziatech offers two software development systems for ZT 8809A applications: STD ROM and STD DOS. STD ROM allows users to develop ROM-based (non-DOS) applications using an IBM or compatible PC. The PC, which is connected to the ZT 8809A through a serial link, runs Paradigm's DEBUG/RT. This allows the use of high-level languages such as C and Assembly for system development.

The second development system, STD DOS, is the popular MS-DOS operating system residing in ROM on the ZT 8809A. The ZT 8809A supports MS-DOS 5.0 in its "ROMed" form. DOS actually executes from EPROM, leaving most of the RAM for application programs. Applications can be developed much faster with STD DOS by programmers familiar with DOS. STD DOS includes support for many peripherals such as disks, video, etc. It is supported by a large number of development tools such as program editors, compilers, assemblers, and debuggers.

For more information on Ziatech's STD ROM or STD DOS development capabilities, see their respective data sheets.

Numeric Data Processor Module

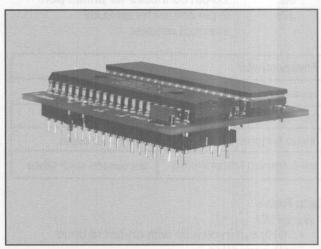
The zSBC 337 Numeric Data Processor Module allows an 8087 Numeric Data Processor (NDP) to be added to the ZT 8809A computer. The 8087 coprocessor operates in unison with the V20, increasing math performance by a hundredfold. Increased math capabilities include 68 additional instructions for extended arithmetic; seven added data types including integers, floating-point, and BCD; and built-in error handling.

The zSBC 337 is a 2" x 2" (5.1cm x 5.1cm) module with two 40-pin sockets for housing the 8088 or NEC V20 and 8087 processors. The base side holds a 40-pin dual in-line socket. A user-supplied spacer socket

plugs into the location normally occupied by the 8088 on the CPU board, and the module's base side socket plugs into the spacer socket. The zSBC 337 is functionally equivalent to Intel's iSBC 337.

Low Power/Extended Temperature

The ZT 88CT09A is designed and tested for -40° to +85° Celsius operation in harsh environments. This product is designed for use in conjunction with Ziatech's other LT (low temperature) and CT (CMOS, TTL backplane compatible) products for mobile and outdoor applications.



zSBC 337 NDP (angled view)

Specifications

Electrical

STD 32- and STD-compatible

Power Req.	Min.	Тур.	Max.
Supply Voltage, V _{CC}	4.75V	5.0V	5.25V
Supply Current, V _{CC} = 5.0V ZT 8809A ZT 88CT09A	Soard VI Soard V	0.8A 0.2A	1.6A 0.54A
Aux Voltage, V _{aux+}	11.4V	12.0V	12.6V
Aux Current, V _{aux+} =12.0V		15mA	25mA
Aux Voltage, V _{aux} -	-12.6V	-12.0V	-11.4V
Aux Current, Vaux-=-12.0V	-	15mA	25mA

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 mechanical specifications
- Measures 4.5" x 6.5" (11.4cm x 16.5cm)
- Height: 0.42" (10.7mm)
 With the 8087 (zSBC 337) installed,

height = 0.82" (20.8mm)

With battery installed, height = 0.50" (12.7mm)
With 128 Kbytes RAM module installed,

height = 0.60" (15.2mm)

· Weight: 10 oz. (283.5g) fully loaded



Specifications and Management and April 2016

Mechanical (continued)

Connectors

Seven user connectors: J1 through J7 in addition to the STD Bus connector P1

J1, J2: 14-pin locking connectors for serial ports

J3: 10-pin locking connector for timers J4: 10-pin locking connector for

interrupt controller

2-pin connector for AC power input J5: 20-pin connector for printer port J6:

J7: 2-pin connector for 8087

interrupt request

Environmental		
Operating Temperature, ZT 8809A	0° to 65° Celsius	
Operating Temperature, ZT 88CT09A	-40° to +85° Celsius	
Storage Temperature	-40° to +85° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

Data Rates

Serial I/O:

· 56 Kbaud maximum with on-board baud rate generator

Parallel I/O:

• 128 Kbytes/sec. maximum at 5 MHz

Reliability

 MTBF: 32 years (ZT 8809A); 38 years (ZT 88CT09A)

MTTR: five minutes (based on board replacement)

Ordering Information

Single Board V20 Computer ZT 8809A ZT M8809A Single Board V20 Computer manual ZT 88CT09A Single Board 80C88 Computer, extended temperature

The minimum configuration comes without RAM, PROM, or BIOS and is ordered as: ZT 8809A-P0R0S0.

The recommended DOS configuration has 256 Kbytes EPROM, 200ns, 640 Kbytes static RAM, 120ns, DOS and BIOS installed in PROM, and a 1 amp-hour lithium extended temperature battery. This is ordered as: ZT 8809A-P2R5S1B.

Must choose one option from each category: **PROM Options**

PO No EPROM

P2 256 Kbytes EPROM, 200ns

RAM Options

RO No RAM

R1 128 Kbytes static RAM, 100ns

R2 256 Kbytes static RAM, 100ns

R3 384 Kbytes static RAM, 100ns

R4 512 Kbytes static RAM, 120ns R5 640 Kbytes static RAM, 120ns

Software Options

S0 No software installed on board

S1 DOS and BIOS installed in PROM (Requires Options P2R1B or greater)

Choose miscellaneous options as needed:

Miscellaneous Options

B 1 amp-hour lithium battery, extended temperature

M Numeric Data Processor Module and 8087-2 math coprocessor (for use with ZT 8809A CPU)

Development Environments

Either STD DOS or STD ROM required with initial purchase. Manuals for hardware are free with the purchase of a STD DOS or STD ROM development environment.

ZT 94004 STD DOS Development Environment Includes host development disk containing VSC, PROMPREP, FLASH, and other utilities. STD Device Driver Package (STD DDP) with support for STD 32 I/O cards and peripherals, ZT 7502/00 BIOS diagnostic card, full Microsoft MS-DOS, and a serial cable. (Requires options P2R4S1B or greater.)

ZT 94005

STD ROM Development Environment. STD ROM development system for PROM-based target systems. Includes Virtual Terminal Interface (VTI) installed on PROM, Paradigm LOCATE and Startup modules, STD DDP, Paradigm DE-BUG/RT, and a serial cable.

Refer to Ziatech's STD ROM and STD DOS Technical Data Sheets and Ziatech's price list for system configurations and options.

Warranty - Five years with an optional five-year extension. See the full warranty statement in the Technical Data Book appendix. Batteries are not covered by Ziatech's warranty.



STO32°

ZT 8901

Single Board V53 Computer

A highly integrated, single board STD 32[®] computer for embedded applications requiring advanced 80286 performance, abundant on-board memory, and industrial I/O.

The ZT 8901 Single Board V53 Computer is intended for embedded applications where performance, size, and reliability are high priorities. It operates at 16 MHz with a high-speed on-board bus, yet is completely compatible with STD 32 and STD Bus designs. The ZT 8901 also supports multiple bus-master operation, allowing multiple processors to operate in a single STD 32 backplane.

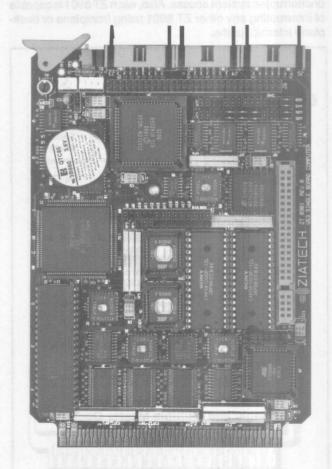
In addition to its STD 32 capabilities, the ZT 8901 features ample on-board memory and I/O, making it an effective stand-alone single board computer.

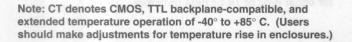
The NEC V53 microprocessor on the ZT 8901 is code-compatible with the 80286 microprocessor (real mode), while providing better performance and many additional features.

The ZT 8901 is supported by STD ROM for embedded applications, STD DOS for DOS-based systems, and the STAR BIOS for multiprocessing DOS-based applications in an STD 32 STAR SYSTEM™.

The ZT 89CT01 version is available for extended temperature operation (-40° to +85° C) at 12.5 MHz.

- STD 32- and STD-compatible
- 16 MHz V53 processor
- · Numeric data processor socket
- 80286 code-compatible for real mode operation
- 16 Mbyte memory address range
- · Up to 1 Mbyte static RAM, optional battery
- Up to 1 Mbyte PROM/512 Kbyte flash PROM
- 64 Kbyte I/O address range
- STD 32 multiple bus-master operation
- One RS-232 serial port (8251)
- Two RS-232/422-485 serial ports (16552), one with DMA
- One interrupt controller (8259)
- Three 16-bit counter/timers (8254)
- Three DMA channels (8237 or 71071)
- · 8-bit or 16-bit SBX with DMA
- 48 parallel I/O lines (Opto 22-compatible)
- Real-time clock, optional battery
- AC/DC power-fail detection
- · Single-stage watchdog timer
- Push-button reset
- Dynamic 8- and 16-bit bus sizing
- · Low power CMOS with sleep mode
- Software-programmable LED
- Standard STD size with no porches or extensions
- Burned in at 55° C and tested to guarantee reliability
- ZT 89CT01 for extended temperature operation







Functional Considerations

STD Bus Interface

The ZT 8901 supports both STD 32 and STD Bus backplane architectures. In an STD backplane, all data transfers between the ZT 8901 and the bus are reduced to 8 bits. In an STD 32 backplane, dynamic bus sizing signals determine the width of the data transfer between the ZT 8901 and other boards.

The bus address, data, and control signals are held static during local operations for reduced power consumption. External masters, such as fixed and floppy disk controllers, are supported through the bus request/bus acknowledge protocol.

Multiple Bus-master Operation

The ZT 8901 can be jumper-configured for STD 32 multimaster operation. With the addition of the ZT 89CT39 Slot X Arbiter Card, as many as seven ZT 8901 boards can be used in a single STD 32 system. This architecture permits any of the ZT 8901 boards to access STD Bus memory and I/O using a fixed or rotating priority scheme.

In operation, a ZT 8901 gains permission for a system access from the arbiter. The ZT 8901 then completes the system transfer and either releases control of the system resources (bus release mode) or holds control of the system resources until requested to release by the arbiter (bus hold mode). A locking mechanism is supported to guarantee uninterrupted system access. Also, each ZT 8901 is capable of interrupting any other ZT 8901 using frontplane or backplane interrupt paths.

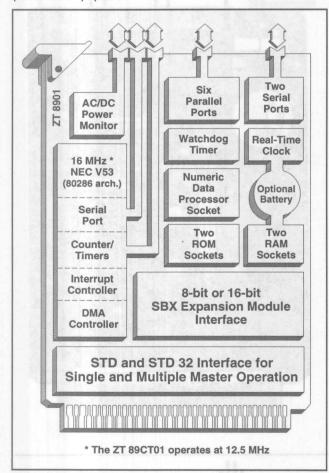


Figure 1. The ZT 8901 Functional Block Diagram

NEC V53 Processor

The NEC V53 is a highly integrated, 16-bit CMOS microprocessor. The V53 includes several standard peripherals in addition to a CPU with an architecture similar to the 80286. Design of the processor has been optimized to execute instructions up to 20% faster than an 80286 operating at the same clock frequency.

The primary difference between the V53 CPU and the 80286 is in the method used to address memory between the 1 Mbyte and 16 Mbyte address range. The V53 uses an extended addressing method to software bank select 16 Kbyte memory blocks from the 16 Mbyte physical address range to the 1 Mbyte logical address range. It does not support the protected address mode available on the 80286.

Extended Math Performance Option

The ZT 8901 features a socket for an 80287 or IIT 2C87 numeric data processor for applications that require additional math capability. Plugging the numeric data processor into the socket provides more than 70 added instructions for extended arithmetic, trigonometric, exponential, and logarithmic functions. These added instructions are supported by seven additional data types, including integers (16-, 32-, and 64-bit), floating-point (32-, 64-, and 80-bit), and Binary Coded Decimal (18-digit).

Memory Addressing

The ZT 8901 supports a 16 Mbyte memory addressing range. This address space is divided between memory local to the ZT 8901 and space available for STD Bus memory expansion. Local memory operations use a 16-bit data path to transfer data at a rate of 16 Mbytes per second.

In an STD system, all backplane memory operations are implemented with 8-bit data transfers. In an STD 32 system, dynamic bus sizing is used to support both 8-bit and 16-bit data transfers for backplane memory.

Four 32-pin memory sockets are organized into two pairs to support the 16-bit nature of the V53. One socket pair accepts RAM devices (32 Kbyte, 128 Kbyte, and 512 Kbyte) with a standard 0.6-inch (15.2mm) DIP footprint. The RAM devices support battery backup with the addition of the optional battery. The other socket pair accepts EPROM and flash memory devices (from 128 Kbyte to 512 Kbyte) with a standard PLCC footprint.

An extractor tool (the ZT 98034) is required to remove the PLCC devices from the sockets. A programming adapter (the ZT 98035) may also be required to program the PLCC devices with a PROM programmer having a 32-pin, 0.6-inch (15.2mm) DIP socket.

I/O Addressing

The ZT 8901 supports a 64 Kbyte I/O address range. This address space is divided between I/O local to the ZT 8901 and space available for STD Bus I/O expansion.

In an STD system, all backplane I/O operations are implemented with 8-bit data transfers. In an STD 32 system, dynamic bus sizing is used to support both 8-bit and 16-bit data transfers for backplane I/O. The STD Bus IOEXP signal is driven low for backplane I/O operations in the address range from FC00 through FFFFh. This prevents boards that decode IOEXP and fewer than 16 bits of address from being redundantly mapped. All devices local to the ZT 8901, except the SBX expansion module, operate with 8-bit data transfers. The SBX expansion module is jumper-selectable for either 8-bit or 16-bit data transfers.

ZT 8901 Single Board V53 Computer

Serial I/O

Three asynchronous serial I/O ports are available, each with a programmable baud rate generator. The V53 provides one serial channel (8251 architecture for asynchronous operation) configured for RS-232 DTE operation with a maximum transfer rate of 640K baud. This serial channel supports transmit data (TxD), receive data (RxD), and ground through a 3-pin frontplane connector. An optional cable is available to connect the V53 serial channel to a male 25-pin, D-shell connector.

The other two serial channels (16450 architecture) are equivalent to the serial I/O used in IBM personal computers. These channels support all handshaking and modem control signals and are jumper-selectable for RS-232 or RS-422-485 operation, as well as DCE or DTE. Other features include transfer rates up to 115.2K baud, loopback diagnostics, maskable interrupt generation, software-selectable 16-byte FIFO for both transmit and receive buffers, and software-selectable DMA-driven data transfers.

Optional cables are available to connect these serial channels to a male or female 25-pin D-shell connector.

Parallel I/O

Six 8-bit parallel ports provide a total of 48 buffered parallel I/O lines. Each I/O line is programmable for input or output with readback operation. The outputs sink 12mA and do not glitch during power-up or power-down, features that are especially useful for industrial applications. The I/O signals and fused power are accessible through a 56-pin frontplane connector. An interface adapter is available to connect the parallel I/O to two 8-, 16-, or 24-position I/O module mounting racks, such as those offered by Ziatech and Opto 22.

Interrupts
The interrupt controller (8259 architecture) supports eight maskable inputs and cascade operation for up to 43 interrupts. Features of the interrupt controller include level- and edge-triggered sensing, fixed and rotating priorities, and the ability to mask individual inputs. There are 15 possible interrupt sources selected through jumper configuration. The interrupt sources include counter/timers, serial I/O, SBX expansion module, real-time clock, STD Bus, and a frontplane connector.

Counter/Timers

Three independent, 16-bit counter/timers (8254 architecture) act as timers or event counters. There are six programmable counter/timer modes: interrupt on end-of-count, frequency divider, square wave generator, software-triggered, hardware-triggered, and retriggerable one-shot. Two of the counter/timers can generate maskable interrupts and the third is available through the frontplane to be used as required by the application.

Watchdog Timer

The watchdog timer monitors system operation. If jumperenabled, the watchdog timer must be strobed at a periodic rate by the application software. Failure to strobe the watchdog timer results in a system reset.

Real-Time Clock

The real-time clock (National Semiconductor 8572A) performs timekeeping functions and includes 44 bytes of RAM. With the optional battery installed, these features continue to operate when power is removed. Timekeeping features include resolution down to 0.01 seconds, 12- or 24-hour operation, leap year adjustment, rollover status, time comparison and periodic interrupts, and automatic time logging in the event of a power failure.

DMA Controller

The DMA controller is programmable for either 8237 (8-bit) or 71071 (16-bit) operating modes. Regardless of the mode selected, there are three DMA channels for high-speed data transfer between local memory and local I/O. DMA channel 0 is dedicated to transfers between the SBX expansion module and local memory. DMA channel 1 is dedicated to transfers from the COM2 serial channel receive buffer to local memory. DMA channel 2 is dedicated to transfers from local memory to the COM2 serial channel transmit buffer.

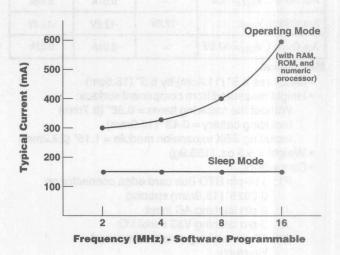
Features of the DMA channels include single-byte transfers, block transfers, fixed or rotating channel priorities, and (71071 only) 2.3 Mbytes per second transfer rates for 8-bit I/O and 4.6 Mbytes per second transfer rates for 16-bit I/O.

SBX Expansion Module Socket

The SBX expansion module socket provides an alternative to expanding the I/O capabilities of the ZT 8901 through the STD Bus. The SBX interface is electrically, mechanically, and functionally equivalent to the IEEE 959-1988 specification developed by Intel. This makes available hundreds of off-theshelf I/O modules. The interface supports both 8- and 16-bit modules and includes DMA capabilities for high-speed data transfers.

Extended Temperature Operation

The ZT 89CT01 is designed with low-power and extended temperature CMOS technology for a typical power consumption of less than 600 mA with the optional numeric data processor, 256 Kbytes of ROM, and 256 Kbytes of RAM installed. The ZT 8901 also supports a software programmable operating frequency and sleep modes for even lower power consumption. The figure below is a graph of typical power consumption versus programmed frequency for both operating and sleep modes.



AC Power-Fail Protection

With the addition of an optional AC transformer, the ZT 8901 monitors AC power to permit an orderly shutdown during a power failure. When AC power falls below an acceptable operating range, a non-maskable interrupt is generated to notify the V53 processor of the impending power failure. The application software can then save critical data before the processor is reset.



Software

Ziatech offers two software development systems for ZT 8901 applications: STD ROM and STD DOS. STD ROM allows users to develop ROM-based (non-DOS) STD applications on an IBM or compatible PC. The PC, which is connected to the STD system through a serial link, runs Paradigms DEBUG/RT. This allows high-level languages such as C and Assembly to be used for system development.

The second development system, STD DOS, is the popular DOS operating system residing in flash memory on the ZT 8901. Applications can be developed much faster with STD DOS by programmers familiar with DOS. STD DOS provides support for many peripherals such as disks and video. It is supported by a large number of development tools such as editors, compilers, assemblers, and debuggers.

When enhanced by the STAR BIOS, the ZT 8901 can work in the same backplane with other processors, each running DOS and sharing disks and video to provide real-time DOS-based control systems (see the STD 32 STAR SYSTEM™ data sheet).

Specifications

 Compatible with STD 32, STD-80, and IEEE 959-1988 SBX specifications

Electrical

DC Operating Characteristics:

Power Req.	Min.	Тур.	Max.
Supply Voltage, V _{CC}	4.75V	5.0V	5.25V
Supply Current, V _{CC} =5.0V ZT 8901 ZT 89CT01	d engit er d engit er agorij aus	.45A .35A	.85A .75A
Aux Voltage, V _{aux+}	11.4V	12.0V	12.6V
Aux Current, Vaux+=12.0V		0.01A	0.02A
Aux Voltage, V _{aux} -	-12.6V	-12.0V	-11.4V
Aux Current, Vaux-=-12.0V	_	0.01A	0.02A

Mechanical

- Measures 4.5" (11.4cm) by 6.5" (16.5cm)
- Height measured from component surface:
 Without the following items = 0.38" (9.7mm)
 Including battery = 0.43" (10.9mm)
 Including SBX expansion module = 1.15" (29.2mm)
- Weight = 5.5 oz. (155.9g)
- Connectors
 - P1: 114-pin STD Bus card edge connector on 0.0625" (15.9mm) spacing
 - J1: 2-pin latching AC input
 - J2: 3-pin latching V53 serial I/O
 - J3: 16-pin latching counter/timer and interrupts
 - J4: 14-pin latching COM2 serial I/O
 - J5: 14-pin latching COM1 serial I/O
 - J6: 56-pin parallel I/O
 - J7: 44-pin latching SBX expansion module

STD 32 Compliance Levels

See the STD 32 Brochure in the Data Book appendix for STD 32 Compliance Level definitions.

 Permanent Master: SA16, SA8 - I, ICA, IXL, IXP, MB, MD • Temporary Master: SA16, SA8 - {MD} I, ICA,

IXL, IXP

Memory Slave: SA8

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz)

Environmental	
Operating Temperature (ZT 8901)	0° to 65° Celsius
Operating Temperature (ZT 89CT01)	-40° to +85° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

Reliability

- MTBF: 20 years
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8901	Single Board	V53 Compute

ZT 89CT01 Single Board V53 Computer, extended

temperature

ZT M8901 Single Board V53 Computer manual

Must choose one option from each category:

Flash Options:

P0	No flash EPROM, 180ns
P1	256 Kbytes flash EPROM, 180ns
P2	512 Kbytes flash EPROM, 180ns

RAM Options:

R4

	: [1] [1] [1] [1] [1] [1] [1] [1] [1] [1]
R0	No RAM
R1	256 Kbytes static RAM, 100ns
R2	256 Kbytes static RAM, 55ns
R3	1 Mbyte static RAM, 120ns

1 Mbyte static RAM, 55ns (Option R4 cannot be battery backed)

Software Options:

Jones	Optiono.
SO	No software installed on board
S1	DOS and BIOS installed

(Requires Options P1R1B or greater)

Miscellaneous Options:

B 1 amp-hour lithium battery (ext. temp.)
M 80287 Numeric Coprocessor, 20 MHz

Development Environments

Either STD DOS or STD ROM is required with initial system purchase. Manuals for hardware are free with the purchase of a STD DOS or STD ROM development system.

ZT 94007

STD DOS Development Environment. Includes host development disk containing VSC, PROM-PREP, FLASH, and other utilities. STD Device Driver Package (STD DDP) with support for STD 32 I/O cards peripherals, ZT 7502/00 BIOS diagnostic card, full Microsoft MS-DOS, two serial cables, and a PLCC extractor tool. (Requires options P1R3S1B.)

ZT 94008

STD ROM Development Environment. STD ROM development system for PROM-based target systems. Includes Virtual Terminal Interface (VTI) installed on PROM, Paradigm LOCATE and Startup modules, STD DDP, Paradigm DEBUG/RT, two serial cables, and a PLCC extractor tools.





ZT 8902 Single Board 486 Computer

A compact, cost-effective STD 32® computer with 486 CPU performance options for single or multiple processor control applications.

The ZT 8902 is a highly integrated 486-based computer on a single STD 32® board. It combines high performance with industrial reliability and small size. The board can operate as a single CPU or as a permanent or temporary master in multiprocessing environments such as Ziatech's STD 32 STAR SYSTEM™.

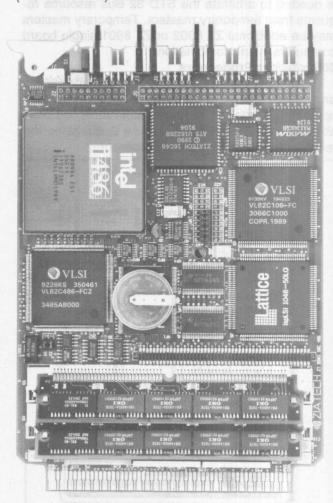
The ZT 8902 is available with processor options ranging from the low-cost 25 MHz 486sx to the 66 MHz 486Dx2. It supports up to 2 Mbytes of flash memory, up to 16 Mbytes of DRAM, two serial ports, a printer port, 24 points of industrial digital I/O and additional counter/timers. The board's STD 32 bus transfers provide high bus bandwidth and compatibility with

existing STD I/O cards. An optional plug-in adapter board adds high-speed, 32-bit "local bus" Super VGA video to the ZT 8902 without taking up an extra slot. This gives the ZT 8902 high resolution graphics capability and high-speed video performance, and frees the backplane from handling video data.

The ZT 8902 is AT-compatible and is supported by Ziatech's Industrial BIOS and Microsoft® MS-DOS®. It will also run UNIX®, OS/2®, QNX®, and other operating systems.

The ZT 89LT02 contains the same features, but combines low power and low temperature operation (-40° to +70° C) for harsh environments.

- STD 32- and STD-compatible
- Occupies a single backplane slot
- · Optional 32-bit local bus video support
- Multiprocessing STAR SYSTEM-compatible
- 25 to 66 MHz 486sx/px/px2 operation
- 4, 8, or 16 Mbytes of DRAM
- 1 or 2 Mbytes of flash memory
- Standard AT peripherals include DMA controllers, interrupt controllers, counter/timers, and real-time clock/CMOS RAM
- Additional counter/timers (8254)
- 24-point digital I/O interface
- Centronics printer port
- Two RS-232 serial ports (16450)
- Watchdog timer
- Push-button reset
- AC/DC power-fail detection
- Compatible with Microsoft MS-DOS, Microsoft Windows™ 3.1, OS/2, UNIX, QNX, and VRTX32
- STD DOS and STAR BIOS options
- Standard 4.5" x 6.5" board format
- Speaker interface
- +5V-only operation (flash memory programming requires ±12V)
- ZT 89LT02 option provides for -40° to +70°C operation
- Burned in at 55° C and tested to guarantee reliability



Note: LT (low temperature) denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40° to +70° C. (Users should make adjustments for temperature rise in enclosures.)



Functional Considerations

STD Bus Interface

The ZT 8902 supports both STD and STD 32 backplane architectures. In an STD backplane, all data transfers between the ZT 8902 and the bus are reduced to 8 bits. In an STD 32 backplane, dynamic bus sizing signals determine the width of the data transfer between the ZT 8902 and the bus.

Multiprocessing Operation

The ZT 8902 supports multiprocessing operation for sharing STD Bus memory and I/O resources with additional ZT 8902 single board computers, or other STD 32 masters. Other Ziatech multiprocessing offerings include the ZT 8911 Scalable Processor Board (permanent master), and the ZT 8901 Single Board V53 Computer (permanent/temporary master). The STD 32 multiprocessing architecture includes a single permanent master and up to six temporary masters. The ZT 8902 is easily configured for either permanent or temporary master operation. When operating as a permanent master, the ZT 89CT39 Slot X Arbiter Card is needed to arbitrate the STD 32 Bus resource requests from temporary masters. Temporary masters may be additional ZT 8902 or ZT 8901 single board computers in any combination.

486sx/Dx/Dx2 Processors

The ZT 8902 supports the 486sx, 486px, and 486px2 processors. The processors are distinguished by their operating speeds and the floating-point functions available on all but the 486sx. **Figure 2** illustrates the relative performance of these processors.

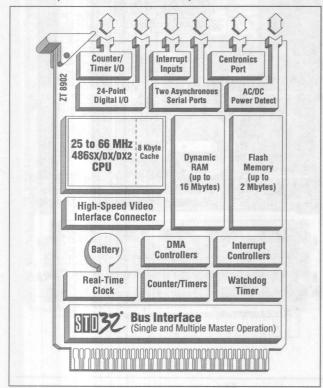


Figure 1. The ZT 8902 functional block diagram

Memory and I/O Addressing

The ZT 8902 includes two 64-pin SIMM sockets that support up to 16 Mbytes of DRAM. The ZT 8902 also includes flash memory soldered directly on the board, and many I/O peripherals required for industrial control applications. The STD I/O expansion signal (IOEXP) is supported to limit the addressing redundancy of I/O boards that decode fewer than 16 bits of address. Data transfers are dynamically adjusted to support standard architecture (SA) memory boards with an 8-bit or 16-bit data path.

Local Bus Video

Video is supported with a separate STD video expansion board or with a small adapter board that plugs directly onto the ZT 8902. Ziatech's STD 32 video expansion boards include the ZT 8982 Super VGA/Flat Panel and Keyboard Interface and the ZT 8842 VGA/Flat Panel and Keyboard Interface.

Ziatech's zVID2 Local Bus Super VGA/Flat Panel Video Adapter adds local bus Super VGA and Flat Panel video capability to the ZT 8902. The plug-in zVID2 adapter operates at the CPU speed (25 or 33 MHz) and utilizes a full 32-bit data bus width. This increases video performance up to 10 times over boards that operate at the ISA bus speed (8 MHz) and use a 16-bit data width. The ZT 8902 with the zVID2 adapter installed provides 486 processing and high-performance Super VGA video in a single STD 32 backplane slot.

Serial I/O

There are two on-board PC-compatible serial ports. The serial ports are implemented with a $\pm 5V$ -only charge pump technology to eliminate the need for a $\pm 12V$ supply. Both serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115.2 Kbaud.

The serial ports are configured as DTE and are available through 10-pin frontplane connectors. Optional cables interface the frontplane connectors to 9-pin D-shell connectors. A null-modem option is also available to convert the DTE configuration to DCE. Adapter boards that provide RS-485 operation are available from Ziatech.

Printer Interface

The ZT 8902's parallel printer port can be connected to a Centronics-compatible printer. The printer interface is available through a 20-pin frontplane connector. An optional cable is available to interface the frontplane connector to a Centronics printer.

Parallel I/O

The ZT 8902 has three 8-bit parallel I/O ports for a total of 24 parallel I/O lines. Each line is programmable as an input or an output with readback. The outputs sink 12mA and do not glitch during power-up or power-down. The 24 lines are available through a

50-pin frontplane connector. Optional cables interface the frontplane connector to an 8-, 16-, or 24-position I/O module mounting rack, such as Ziatech's ZT 2226 24-Channel I/O Mounting Rack or those offered by Opto 22.

Interrupts

The ZT 8902 includes two interrupt controllers providing a total of 15 interrupt inputs. The interrupt controller supports level-triggered and edge-triggered inputs, fixed and rotating priorities, individual masking, and programmable logic to reduce noise sensitivity. Interrupt sources include counter/timers, serial I/O, real-time clock, keyboard, printer, and multiple master communications. There are also five STD 32 Bus and five frontplane interrupt sources.

Counter/Timers

Six counter/timers are included on the ZT 8902. There are six programmable operating modes: interrupt on count, frequency divider, square wave generator, software-triggered, hardware-triggered, and one-shot. Three of the counter/timers are dedicated to supporting local devices. Three additional counter/timers are available through a 10-pin frontplane connector.

Watchdog Timer

The watchdog timer optionally monitors system operation. Failure to strobe the watchdog timer within a fixed time period results in a system reset.

Real-Time Clock

The real-time clock performs timekeeping functions and includes 66 bytes of battery-backed CMOS RAM. Timekeeping features include an alarm function, a maskable periodic interrupt, and a 100-year calendar. **Keyboard Controller**

The ZT 8902 includes a PC/AT keyboard controller that operates when the zVID2 local bus video adapter is installed. The keyboard connector is located on the zVID2 adapter.

AC Power-Fail Protection

With the addition of an AC transformer, the ZT 8902 monitors AC power to permit an orderly shutdown during a power failure. When AC power falls below an acceptable operating range, a non-maskable interrupt is generated to notify the CPU of the impending power failure. When the application software receives this notification, it saves critical data before the CPU is reset.

Low Power/Extended Temperature

The ZT 89LT02 is designed and tested for -40° to +70° Celsius operation in harsh environments. The companion zVID2 is also available in an LT (low temperature) version. These products are designed for use in conjunction with Ziatech's other LT and CT products for mobile and outdoor applications.

Software

The ZT 8902 is supported by Ziatech's STD DOS and STAR BIOS. STD DOS is the MS-DOS operating

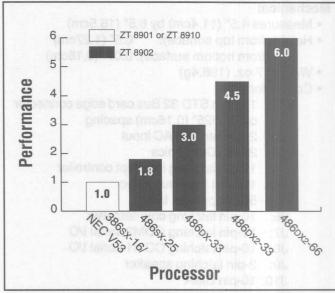


Figure 2. The ZT 8902's performance relative to that of the ZT 8901 (V53) and 386sx processors

system residing in flash memory on the ZT 8902. Applications can be developed much faster using the STD DOS built-in disk and video services. STD DOS is also supported by many development tools such as editors, compilers, assemblers, and debuggers. Under STD DOS, the flash memory is recognized as a read/write disk, and is supported by Microsoft's Flash File 2.0 (FF2).

STAR BIOS permits STD DOS to operate concurrently on more than one ZT 8902 in a single STD 32 backplane. This allows all the processors in a system to share resources, such as disk and video, across the backplane. See the STD 32 STAR SYSTEM™ data sheet for more information.

Specifications

 Compatible with the STD 32 and STD-80 Bus specifications

Electrical

Power Output	Min.	Тур.	Max.
Supply Voltage, V _{CC}	4.75V	5.00V	5.25V
Supply Current, VCC = 5.0V	M.F.UFIC	xeBBA sHu	1 8S a ri
486SX-25*	ibril 2'rlop	0.9A	1.5A
486SX-33*	s se ben	boro el end	raem da
486DX-33*	brace o	1.2A	2.0A
486DX2-50*	A ROBERT	1.3A	2.2A
486DX2-66*	Uteteoms	1.5A	2.5A
Aux Voltage, V _{aux+}	11.4V	12.0V	12.6V
Aux Current, Vaux+ = 12.0V	-	0.010A	0.030

^{*}Four Mbytes of DRAM and flash memory



Mechanical

- Measures 4.5" (11.4cm) by 6.5" (16.5cm)
- Height (from top surface): 0.5" (1.27cm)
 (from bottom surface): 0.07" (0.18cm)
- Weight: 7 oz. (198.4g)
- Connectors
 - P1: 136-pin STD 32 Bus card edge connector on 0.0625" (0.16cm) spacing
 - J1: 2-pin latching AC input
 - J2: 20-pin Centronics
 - J3: 10-pin latching interrupt controller
 - J4: 100-pin local bus video
 - J5: 50-pin parallel I/O
 - J6: 10-pin latching counter/timer
 - J7: 10-pin latching COM2 serial I/O
 - J8: 10-pin latching COM1 serial I/O
 - J9: 2-pin latching speaker
 - J10: 10-pin DMA

Environmental		
Operating Temperature (ZT 8902)	0° to 65° Celsius	
Operating Temperature (ZT 89LT02)	-40° to +70° Celsius	
Storage Temperature	-40° to +85° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

STD 32 Compliance Levels

See The STD 32 brochure in the appendix of the *Technical Data Book* for more details regarding STD 32 Compliance Level descriptions.

- Permanent Master: SA16, SA8-I, MB, SDM A8, SDMA16, SDMABP
- Temporary Master: SA16, SA8-{MD}, I, SDM A8, SDMA16, SDMABP
- Memory Slave: SA16

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz)

Reliability

- MTBF: 21 years
- MTTR: five minutes (based on board replacement)

Ordering Information

Example: A ZT 8902 Single Board 486 Computer with a 25 MHz 486sx CPU, 4 Mbytes of RAM installed, and MS-DOS and Ziatech's industrial BIOS installed in flash memory, is ordered as a ZT 8902-C1R1S1.

ZT 8902 ZT 89LT02 Single Board 486 Computer Single Board 486 Computer,

low temperature

ZT M8902

Single Board 486 Computer manual

Must choose one option from each category: CPU Choices

C1 25 MHz 486SX, installed C2 33 MHz 486DX, installed C3 50 MHz 486DX2, installed C4 66 MHz 486DX2, installed C5 33 MHz 486SX, installed

Flash EPROM Choices

P1 1 Mbytes flash, installed P2 2 Mbytes flash, installed

RAM Choices

R1 4 Mbytes DRAM, installed R2 8 Mbytes DRAM, installed R3 16 Mbytes DRAM, installed (two slots total)

Software Choices

S1 Microsoft MS-DOS 5.0 and Ziatech's industrial BIOS installed in flash memory

S2 Microsoft MS-DOS 5.0 and
Ziatech's STAR BIOS
(multiprocessing) installed in
flash memory

Select from the following options as needed: Video Options

V2 zVID2 Local Bus Super VGA and Flat Panel Video Adapter, installed

Development environment (for first purchase):

ZT 94015 STD DOS Development Environment; Includes host development disk containing VSC, PROMPREP, FLASH and other utilities, and Ziatech's Device Driver Package (STD DDP) with support for STD 32 I/O cards and peripherals, ZT 7502/00 BIOS diagnostic card, full Microsoft MS-DOS, a serial cable, and a printer cable.

Note: See the STD 32 STAR SYSTEM data sheet for STAR Development options.

Accessories

Cables (see Data Book cable section for details):

ZT 90071 24VAC wall transformer, 2-pin female
ZT 90072 10' (3m), 50-pin both ends
ZT 90074 3' (91cm), 20-pin to 25-pin female
D-shell
ZT 90136 3.3' (1m), 10-pin to 9-pin male
D-shell
ZT 90166 10" (25.4cm) video/keyboard, zVID2

to panel mount connector
ZT 90167 10" (25.4cm) video/keyboard, zVID2

to desktop-style connector
ZT 90168 10" (25.4cm) multi-video/keyboard.

ZT 90168 10" (25.4cm) multi-video/keyboard, connects seven zVID2 adapters to

desktop-style connector



zVID2

Local Bus Super VGA/FPD Adapter

High-speed Super VGA/Flat Panel Display Adapter brings local bus video performance and flat panel support to Ziatech's ZT 8902 Single Board 486 Computer

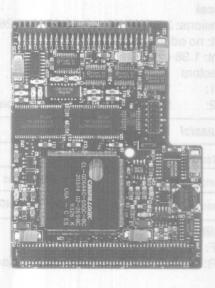
The zVID2 is a 32-bit, high-performance, local bus Super VGA and flat panel display (FPD) adapter for the ZT 8902 Single Board 486 Computer (SBC). The zVID2 operates at the full speed of the CPU, using a 32-bit data path. This allows it to substantially outperform interfaces that use the system backplane or a motherboard's ISA chipset for graphics.

The zVID2 supports most monochrome and color FPDs on the market, including 8- and 16-bit single- and dual-scan color Super Twisted Nematic (STN) panels, and 9-, 12-, and 18-bit Thin Film Transistor (TFT) color panels. The zVID2 contains 1 Mbyte of video memory

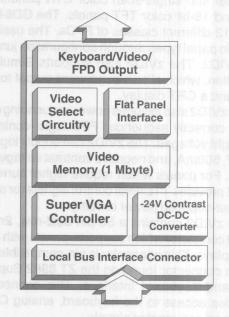
and supports CRT resolutions up to $1024 \times 768 \times 256$ colors, non-interlaced, and $1280 \times 1024 \times 16$ colors, interlaced.

Users can also access the ZT 8902 SBC's keyboard interface, making the zVID2 a space efficient video/keyboard solution. The low-profile zVID2 and ZT 8902 together fit in a single card cage slot.

The zVID2 allows each ZT 8902 SBC in a multiprocessing STD 32 STAR SYSTEM™ to have a separate video display, or to be "daisy-chain" connected in a multiprocessing system, allowing multiple zVID2-equipped processors to share a monitor and keyboard.



- 32-bit high-performance local bus interface
- Supports CPU bus speeds up to 33 MHz
- Up to 10 times the graphics performance of busbased video solutions
- Eliminates backplane bus traffic for video operations
- Microsoft® Windows™ hardware performance features
- One slot for zVID2 and ZT 8902 SBC
- Supports shared or separate video displays in multiprocessing STAR SYSTEMs



- 1 Mbyte high-speed video memory
- Hardware-compatible with IBM Super VGA standard
- 1024 x 768 x 256 colors non-interlaced
- 1280 x 1024 x 16 colors interlaced
- Supports 8- and 16-bit dual- and single-scan color STN panels
- Supports 9-, 12-, and 18-bit color TFT panels
- Simultaneous display of CRT and LCD panels with resolutions up to 1024 x 768 x 256 colors
- Power sequencing circuitry for FPDs



Functional Considerations

Local Bus Interface

The zVID2 connects directly to the ZT 8902 Single Board 486 Computer through a 100-pin board-to-board local bus connector.

The local bus interface intercepts 486 CPU read and write cycles sent to video memory or I/O addresses, preventing the ZT 8902's chipset from performing STD Bus transactions. The local interface uses all 32 data bits and operates at the full speed of the 486 CPU's external data bus (up to 33 MHz).

VGA Controller

The zVID2 design incorporates the Cirrus GD6440 VGA controller. The GD6440 is fully hardware register-compatible with the IBM Super VGA standard and features several Windows performance enhancements such as color expansion and packed pixel memory addressing.

Flat Panel Support

The zVID2 supports most types of monochrome and color Flat Panel Displays (FPDs), including 8- and 16-bit dual- and single-scan color STN panels and 9-, 12-, and 18-bit color TFT panels. The GD6440 supports 12 different classes of FPDs. The user selects specific panel types through configuration jumpers on the zVID2. The zVID2 also supports SimulSCAN™ operation, which allows concurrent output to both an FPD and a CRT display.

The zVID2 also includes power sequencing circuitry, which correctly sequences FPD logic, contrast, and backlight voltages. The zVID2 can supply logic power at +5V, 500mA, and negative contrast voltage at -24V, 30mA. For panels which require higher currents, the zVID2 provides TTL level control signals for sequencing user-supplied power circuitry.

The zVID2 contains a 50-pin dual-row, 2mm horizontal connector which supports panels with up to 18-bit displays. This connector is pin-compatible with the 50-pin connector found on the ZT 8982 Super VGA/FPD and Keyboard Interface. This connector also provides access to the keyboard, analog CRT, and power-on sequencing signals.

Video Memory

The zVID2 contains a full 1 Mbyte of high-speed fast page mode DRAM, allowing it to support high resolution color graphics modes such as $1024 \times 768 \times 256$ colors non-interlaced and $1280 \times 1024 \times 16$ colors interlaced. The video memory is mapped to the standard A0000h to BFFFFh VGA memory space.

Video ROM BIOS

The video BIOS for the zVID2 has been combined with the system BIOS and occupies 32 Kbytes in the CPU's memory. On power-up, the BIOS is automatically installed during system initialization.

Video Select Circuitry

The zVID2 is capable of sharing monitors and

keyboards with other zVID2 modules. This feature is controlled by the zVID2's on-board video/keyboard select circuitry, which consists of a video switch and a software controlled video/keyboard select signal. Up to seven ZT 8902/zVID2 pairs can be daisy-chain connected in a Ziatech STD 32 STAR SYSTEM™ to share a common display and keyboard. Using software control, the user can "hot key" to any of the single board computers with a simple key stroke.

Software

The zVID2 is fully supported by Ziatech's BIOS (Version 4.12 or later). The zVID2 includes a driver/ utility disk with high-resolution drivers for various software packages such as Microsoft Windows 3.x, and various utilities for performing functions such as changing video modes.

Specifications

Electrical

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	175mA	196mA	260mA

Mechanical

- Dimensions: 3.75" (9.50cm) x 2.860" (7.26cm)
- · Height: no additional slots
- Weight: 1.38 oz. (39.1g)
- Connectors

P1: 100-pin local bus interface P2: 50-pin video/keyboard/flat panel

Environmental		
Operating Temperature	0° to 65° Celsius	
Storage Temperature	-40° to +85° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

Reliability

- MTBF: 49 years
- MTTR: five minutes (based on board replacement)

Ordering Information

Local Bus Super VGA/Flat Panel
Display Adapter
ZT 8982/zVID2 software utilities and

Accessories

Cable (See Data Book cable section for details):

ZT 90166

10" (25.4cm) video/keyboard to
panel mount connector

ZT 90167

10" (25.4cm) video/keyboard to
desktop-style connector

manual

ZT 90168 10" (25.4cm) multi-video/keyboard, converts seven zVID2s to desktop-

style connector



STD32°

ZT 8911

Scalable Processor Board

Full 32-bit, STD 32[®] scalable processor board supports the 486 and future generation CPUs in single and multiple processor systems.

The ZT 8911 Scalable Processor Board is a high-performance processor platform designed for the most demanding industrial computing applications. It can operate as a powerful processor in a single CPU system, or as the permanent master in a multiple processor system. It fully implements all of the advanced features of the STD 32 Bus and Intel's 486 processor architecture. The ZT 8911 incorporates a replaceable CPU module that accommodates performance options ranging from the 33 MHz 486SX/DX up to the 66 MHz 486DX2. This module accommodates up to 128 Kbytes of high-speed cache memory. This modular concept also allows the ZT 8911 to support the next generation of CPUs.

The ZT 8911's memory design supports 32 Mbytes of RAM on board, with a 128-bit memory width for optimum cache fills and maximum performance. The STD 32 backplane interface supports multiple master operation, slot-specific interrupts, multiple DMA channels, and full 32-bit operation with transfer rates up to 32 Mbytes-per-second.

By adhering to the STD 32 Bus Specification, the ZT 8911 combines high-performance features with an industrial design. Its industrial features include a watchdog timer, AC

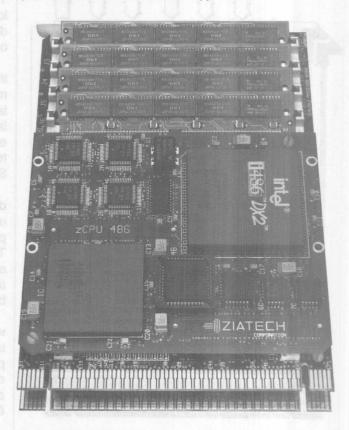
power-fail detect circuitry for system integrity, additional counter/timers for real-time programming, as well as 24 lines of general purpose digital I/O. On-board flash EPROM provides solid-state disk and boot support for MS-DOS® and other operating systems, plus the ability to boot off-board to allow BIOS updating. The ZT 8911 is fully supported by Ziatech's Industrial BIOS.

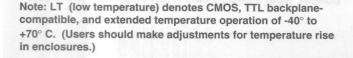
The ZT 8911 also supports other operating systems such as UNIX®, OS/2®, QNX®, and Microsoft® Windows™.

In multiprocessing environments like Ziatech's STD 32 STAR SYSTEM™, the ZT 8911 operates as both the arbitration card and the permanent master. It occupies both Slot X and the first user slot, and implements the full STD 32 feature set, including bus arbitration, multiple high-speed DMA channels, and slot-specific interrupts. 32 Kbytes of static RAM act as common memory for interprocessor communication in a STAR SYSTEM.

The ZT 89LT11 is designed and tested for -40° to +70° Celsius operation in harsh environments. This product is designed for use in conjunction with Ziatech's other LT (low temperature) and CT (CMOS, TTL-backplane-compatible) products for mobile and outdoor applications.

- 33 MHz 486SX/DX to 66 MHz DX2 operation
- Optional second-level 64/128 Kbyte cache
- Numeric coprocessor support (486DX/DX2)
- 4 to 32 Mbytes of DRAM (four 64-pin SIMM sockets)
- 1 or 2 Mbyte of flash for BIOS and solid state disk
- STD 32-compatible with support for STD peripherals
- STD 32 Extended Architecture (EA) and Standard Architecture (SA) Support
- 32 Mbyte/second STD 32 Bus transfer rate
- Centronics printer port
- Two serial (COM) ports (16C552)
- Real-time clock (146818A CMOS static RAM)
- Two 8259 interrupt controllers (15 interrupts)
- Two 8237 superset DMA controllers
- · Speaker interface with on-board speaker
- Extra 8254 counter/timers for user
- 24-point digital I/O interface (16C48)
- 32 Kbytes common memory for STD 32 STAR SYSTEMs
- · Compatible with DOS, OS/2, Windows, UNIX
- · STD DOS and STAR BIOS options
- Off-board boot feature for flash memory update
- · Watchdog timers (non-maskable interrupt and reset)
- Push-button reset
- AC/DC power-fail detect
- Diagnostic POST-code LEDs
- STD 32 arbiter for STD 32 STAR SYSTEM multiprocessing (up to six temporary masters)
- ZT 89LT11 operation from -40° C to +70° C







Functional Considerations Performance

The ZT 8911 Scalable Processor Board is the most powerful CPU available on the STD Bus architecture. Featuring 32 Mbyte/second data transfers, 32-bit backplane performance, and a tuned, 128-bit memory architecture with optional cache, the ZT 8911 provides maximum processing power for demanding applications.

The ZT 8911's memory architecture is designed to take advantage of 486DX2 technology. Equipped with Intel's 486DX2, applications can realize up to 70% performance improvement. Adding a second-level cache boosts average performance an additional 15%. **STD 32 Bus Interface**

The ZT 8911 supports the full feature set of STD 32 transfers. Standard Architecture (SA) 8- and 16-bit transfers are supported as well as 8-, 16-, and 32-bit Extended Architecture (EA) transfers. EA transfers provide up to 32 Mbyte/second transfer rates. The ZT 8911 operates in an STD 32 backplane and supports single processor operation as well as Permanent Master operation in multiprocessing applications (e.g., the STD 32 STAR SYSTEM™). Both EA and SA peripherals can be mixed in ZT 8911 systems, with

Interrupt Inputs Counter/ Timer I/O AC/DC Power Detect 8911 17 24-point Two COM On-Board, Centronics Digital I/O Interface Off-hoard Serial Ports Speaker Watchdog 33-66 MHz Ontiona 486DX/DX2 POST-Code LEDs CPU Battery Replaceable CPU Module Two Interrupt Controllers Real-time Clock 4 to 128 Mbyte Three 8254 Dual-Port System RAM 8 Khyte Counter/Timers Config. RAM 32 Kbyte STARBIOS BIOS/Flash Slot-Specific File System **Shared SRAM** Addressing Interface STD 32 Arbiter/ (32 Mbyte/sec. Transfers)

Figure 1. The ZT 8911 functional block diagram

the ZT 8911 dynamically detecting the type and data transfer rate of the peripheral. Standard Architecture transfers can access STD peripherals.

The ZT 8911 also interfaces to the STD 32 Slot X connector, which provides backplane Direct Memory Access (DMA), additional interrupt support (one per slot), and arbitration services for Temporary Masters. Through Slot X, the ZT 8911 can independently address each STD 32 peripheral for slot-specific configuration, allowing jumperless setup of peripheral boards.

Multiprocessing Operation

In a multiprocessing application, the ZT 8911 serves as the Permanent Master and provides Slot X services for up to six SA and EA Temporary Masters. In addition, BUSRQ*/BUSAK* masters are supported. Shared memory (32 Kbytes) is provided for message passing between STD 32 masters, eliminating the need for a separate memory board for this function.

Arbitration is implemented as a two-stage process to allow true concurrent CPU operation. Temporary Masters (e.g., Ziatech's ZT 8901 Single Board V53 Computer or ZT 8902 Single Board 486 Computer) are awarded the STD 32 Bus, independent of access to the ZT 8911's DRAM subsystem. This allows the processor on the ZT 8911 to continue to operate out of DRAM while the Temporary Master is using backplane resources, such as a floppy disk or hard disk. Only if the Temporary Master explicitly addresses a memory location within the ZT 8911's DRAM address range does a second-level arbitration occur for DRAM ownership.

As a Permanent Master in multiprocessing systems, the ZT 8911 provides bus cycle conversions between mismatched master and peripheral boards. SA masters accessing EA peripherals have their cycles translated to the correct protocol by the ZT 8911, transparent to the SA master. EA masters likewise have access to SA slaves via the ZT 8911 cycle conversion logic.

Scalable Processing

The ZT 8911 is designed with processor independence in mind. The zCPU 486 Replaceable CPU Module is a plug-on board that allows the user to scale the processor performance according to application needs. The processor module interface is a 32-bit data/32-bit address interface that is not processor-specific. This allows future processors such as Intel's Pentium™ to be supported.

Ziatech offers processor modules at 33 MHz with or without an external (to the 486) cache. Cache options include 64 or 128K of write-through cache, which is particularly important for 486DX2 operation. The secondary cache allows zero wait state accesses for noncache hits to the internal 8 Kbyte cache of the 486. Cache Options

The 486 includes an 8 Kbyte, 4-way set associative, posted write-through cache on-chip. For processor



Figure 2. The ZT 8911 occupies Slot X and one user slot (Slot 0) in an STD 32 industrial enclosure.

speeds below 33 MHz, adding a second level cache provides a performance boost by minimizing the latency for level 1 cache misses in the 486. At higher processor speeds, it becomes imperative to have an external cache to maximize the benefit of the additional speed. A 66 MHz 486DX2 offers little performance improvement for applications that constantly overflow the internal 8 Kbyte cache of the 486. Therefore, external caching is recommended when the ZT 8911 is equipped with the 486DX2 processor.

In a multiprocessing system where the system DRAM is shared, the memory bus bandwidth usage should be minimized. This minimizes the arbitration cycles for the system.

The cache on the zCPU 486 Replaceable CPU Module has a 2-way set associative, write-through architecture. The zCPU 486 offers 64 Kbytes of cache, with 128 Kbytes available as a special order.

The ZT 8911's memory design allows snooping of backplane cycles for cache-line invalidation to maintain cache coherency. If a Temporary Master in the STD 32 Bus writes to a memory location that is cached, the ZT 8911 performs a cache-line invalidation so that the local processor on the ZT 8911 does not operate on cached data that differs from the DRAM copy.

Memory Architecture

The ZT 8911 DRAM architecture is optimized for 486 burst performance. Up to four 32-bit-wide DRAM (SIMMs) can be accessed in parallel by the 128-bit

DRAM interface during a burst read. This allows minimal wait state performance for non-cache cycles.

Off-board accesses can be performed at up to 32 Mbytes/second by the STD 32 Bus when accessing Extended Architecture peripherals. EA or SA memory cycles are performed on the STD 32 Bus depending upon the type of memory being accessed. The default designates SA transfers to be performed unless an EA memory board responds to the address generated.

The DRAM subsystem is also dual-ported with STD 32 Bus masters. This allows true, concurrent processing by the ZT 8911 when the STD 32 bus is "owned" by a Temporary Master. The ZT 8911 has four 64-pin SIMM sockets and supports up to 128 Mbytes of memory using double-sided, 16-Mbit SIMMs. Current offerings allow up to 16 Mbytes using four 8-Mbyte SIMMs.

Flash Memory

The ZT 8911 is equipped with flash memory that allows for in-circuit BIOS upgrades as well as Flash File Operation for data logging and solid-state program storage. One Mbyte is standard, with 2 Mbytes available as an option. The BIOS supports this device as a read/writeable disk. Flash memory requires 12 volts for programming.

I/O Addressing

Off-board I/O accesses support both Standard Architecture STD I/O boards and the latest Extended Architecture I/O board. EA I/O can be up to 32 bits wide, accommodating the higher bandwidth requirements of current and future systems. SA I/O transfers can be up to 16 bits wide and support all STD-80 Series I/O peripherals. The IOEXP signal is dynamically driven to allow access to older 8-bit address I/O peripherals to limit redundant mapping of these peripherals.

Slot-Specific I/O Addressing

The ZT 8911 supports slot-specific addressing for up to 14 STD 32 slots. Each slot has a specific decode signal (AENx*). This signal is driven active when the permanent master (ZT 8911) is accessing the slot. In the future, slot-specific addressing will be used for jumperless setup of adapter boards under software control.

Serial I/O

The ZT 8911 includes two PC-compatible serial ports. The serial ports are implemented with a ± 5 V-only charge pump technology to eliminate the need for a ± 12 V supply. Both serial ports include a complete set of handshaking and modem control signals, maskable interrupt generation, and data transfer rates up to 115.2 Kbaud.

The serial ports are configured as DTE and are available through 10-pin frontplane connectors. Optional cables interface the frontplane connectors to 9-pin D-shell connectors. Adapter boards to provide RS-485 operation are available from Ziatech.



Parallel I/O

The ZT 8911 has three 8-bit parallel I/O ports for a total of 24 parallel I/O lines. Each line is programmable as an input or an output with readback. The outputs sink 12 mA and do not glitch during power-up or power-down. The 24 lines are available through a 50-pin frontplane connector. Optional cables interface the frontplane connector to an 8-, 16-, or 24-position I/O module mounting rack, such as Ziatech's ZT 2226 I/O Mounting Rack or those offered by Opto 22.

Interrupts

The ZT 8911 has two interrupt controllers that are supersets of the 8259. Up to 15 independent interrupt sources are provided by the architecture of the ZT 8911. The ZT 8911 is the first STD CPU to interface to STD 32's Slot X connector, which allows for a slot-specific interrupt to the first 14 slots in the STD 32 chassis. This, coupled with the four bussed interrupts on the STD 32 Bus, and five frontplane interrupts, gives the ZT 8911 total flexibility in handling interrupts. The interrupt controllers on the ZT 8911 allow most interrupt levels to be individually programmed for edge or level sensitive operation. This allows easy sharing of interrupts for those configured in level sensitive mode.

On-board interrupt sources include counter/timers, serial I/O, real-time clock, printer interface, DMA controller, and the STAR SYSTEM multiprocessing interrupt. On- and off-board non-maskable interrupts are also supported.

Direct Memory Access

The ZT 8911 is the first STD processor to support backplane Direct Memory Access (DMA) without frontplane handshaking signals. Each of the first 14 slots in an STD 32 chassis has an independent DMA request/acknowledge handshake with the Slot X interface on the ZT 8911. This allows DMA devices to perform high bandwidth (up to 32 Mbyte/sec.) transfers on the backplane. Separate control signals are provided for the DMA device on the backplane so that no frontplane cabling is necessary. The ZT 8911 supports up to six DMA devices at one time.

Watchdog Timer

The ZT 8911 provides two methods for fail-safe operation. A watchdog timer for driving reset to the system is implemented with a Dallas Semiconductor 1238 device. If enabled, the watchdog timer will drive reset unless strobed within the time configured. An alternate, or parallel approach uses the fail-safe timer to generate a non-maskable interrupt (NMI) when it is not strobed within its programmed delay. The fail-safe timer is implemented as a programmable 8254-style counter/timer.

Counter/Timers

The ZT 8911 has three 8254-style counter/timers. Each 8254 has three counter/timers, for a total of nine. Three of these counter/timers implement the IBM

AT-compatible functions of system timer (SYSTICK), refresh, and speaker tone generation. One counter/timer implements the fail-safe timer which will generate an NMI if not strobed within its programmed time. One counter/timer limits the band-width of the host processor's clock to slow the execution speed of the host processor. Three additional non-dedicated counter/timers are provided for application use. These may be interfaced with the outside environment via a 10-pin connector, or controlled locally.

Real-Time Clock

The real-time clock performs timekeeping functions and includes 128 bytes of battery-backed CMOS RAM. Timekeeping features include an alarm function, a maskable periodic interrupt, and a 100-year calendar.

Printer Interface

The ZT 8911's parallel printer port can be connected to a Centronics-compatible printer. The printer interface is available through a 20-pin frontplane connector. An optional cable is available to interface the frontplane connector to a Centronics printer.

AC Power-Fail Protection

With the addition of an AC transformer, the ZT 8911 monitors AC power to permit an orderly shutdown during a power failure. When AC power falls below an acceptable operating range, a non-maskable interrupt is generated to notify the CPU of the impending power failure. When the application software receives this notification, it saves critical data before the CPU is reset.

Software

Software support for the ZT 8911 is built into Ziatech's STD DOS and STAR BIOS. STD DOS is the MS-DOS operating system residing in a PROM on the ZT 8911. Applications can be developed much faster with STD DOS using its built-in disk and video services. STD DOS is also supported by a large number of development tools such as editors, compilers, assemblers, and debuggers.

STAR BIOS permits STD DOS to operate concurrently on more than one CPU in a single STD 32 backplane. This

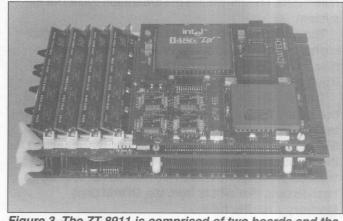


Figure 3. The ZT 8911 is comprised of two boards and the 486 processor module.

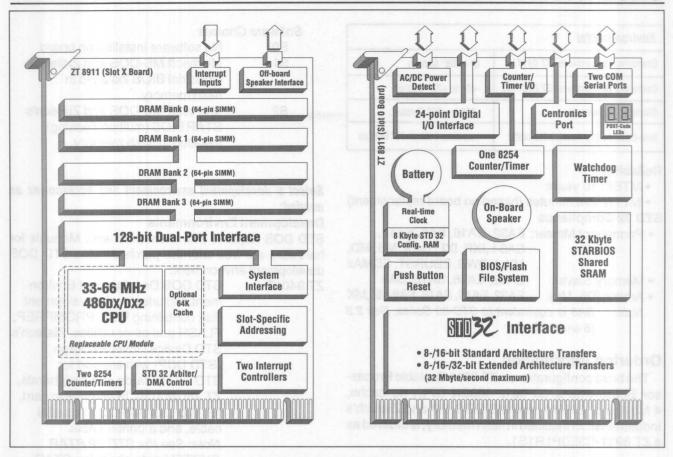


Figure 4. Functional blocks for the top Slot X Board (left), and the bottom Slot 0 Board (right)

allows all the processors in a system to share resources, such as disk and video, across the backplane. See the STD 32 STAR SYSTEM data sheet for more information.

Specifications

- Compatible with the STD 32 Bus Specification
- Supports STD and STD 32 peripheral boards

Electrical

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, V _{CC} = 5.0V (with 33 MHz 486DX, 64K Cache, 16 MB RAM)	ons dtiwer	2.3A	3.5A
Aux Voltage*, Vaux+	11.4V	12.0V	12.6V
Aux Current, Vaux+ = 12.0V	-	20mA	60mA

*Required for flash memory programming only Mechanical

- Occupies one user slot (Slot 0) in addition to Slot X.
 (Must be used in an STD 32 system)
- Measures 4.5" (11.4cm) by 6.5" (16.5cm)
- Height: 1.3" (33mm), including DRAM and 486 CPU module with heat sink
- Weight: 15.5 oz. (439.4g)

Connectors:

Slot X board

J1	10-pin	frontplane	interrupt	interface
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Slot 0 board

J7	2-pin	latching	AC power-fail	input
10	40 .			

J8	10-pin	latching	counter/timer
	intorfoc	0	

(Specifications continued next page.)



J10 10-pin latching COM 1 serial I/O

J11 20-pin Centronics

J12 50-pin parallel I/O (24-point)

Environmental	0 0
Operating Temperature (ZT 8911)	0° to 65° Celsius
Operating Temperature (ZT 89LT11)	-40° to +70° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

Reliability

• MTBF: 10 years

MTTR: five minutes (based on board replacement)

STD 32 Compliance

Permanent Master: EA32, EA16, EA8, SA16,

SA8-I, IXP, IXL, GAX, MB, MD, MX, NOWS, EBURST, EDMAX

Memory Slave: EA32, EA16, SA16, SA8

Arbiter (D6, M6): EA32, EA16, SA16, SA8-MD, MX
 Note: SA8 is equivalent to STD-80 Series, Rev 2.3

(5 and 8 MHz).

Ordering Information

The base configuration, a ZT 8911 Scalable Processor Board with a 33 MHz 486SX CPU, no cache, 4 Mbytes of DRAM, and MS-DOS 5.0 and Ziatech's Industrial BIOS installed in flash memory, is ordered as a ZT 8911-C3E0P1R1S1.

ZT 8911 Scalable Processor Board

ZT 89LT11 Scalable Processor Board, extended

temperature (special order)

ZT M8911 Scalable Procesor Board manual

Must choose one option from each category: CPU Choices

C1 33 MHz 486DX, installed C2 66 MHz 486DX2, installed C3 33 MHz 486SX, installed Contact Ziatech for other CPU choices.

Cache Choices

E0 No cache

E1 64 Kbytes cache memory installed

E2 128 Kbytes cache memory installed

(special order)

Flash Choices

P1 1 Mbyte flash, installed P2 2 Mbytes flash, installed

RAM Choices

R1 4 Mbytes DRAM, installed R2 8 Mbytes DRAM, installed R3 16 Mbytes DRAM, installed R4 32 Mbytes DRAM, installed

Software Choices

No software installed on board
Microsoft MS-DOS and Ziatech's industrial BIOS installed in
flash memory
Microsoft MS-DOS and Ziatech's STAR BIOS (multiprocessing) installed in flash memory

Select a development environment and accessories as needed:

Development Environments

STD DOS required with initial purchase. Manuals for hardware are free with the purchase of a STD DOS development environment.

ZT 94017

STD DOS Development Environment. Includes host development disk containing VSC, PROMPREP, FLASH and other utilities. Ziatech's STD Device Driver Package (STD DDP) with support for STD 32 I/O cards and peripherals, ZT 7502/00 BIOS diagnostic card, full Microsoft MS-DOS, a serial cable, and a printer cable.

Note: See the STD 32 STAR SYSTEM data sheet for STAR development options.

Accessories

Cables (see Data Book cable section for details):

ZT 90072 10' (3m), 50-pin both ends
ZT 90157 3' (91cm) for printer, 20-pin to
25-pin female D-shell
ZT 90136 40" (1m), 10-pin to 9-pin
male D-shell

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.





Application Specific Automation Processor

A quick-turn, custom single board computer for high-volume, embedded applications that require low cost and an exact complement of I/O

The Application Specific Automation Processor (ASAP™) program is intended for high volume applications requiring an exact mix of I/O or peripheral functions on a low cost, single board computer. ASAP computers are developed by integrating existing processor modules with existing Peripheral I/O Modules using an on-board interface specification and CAD (Computer Aided Design) development tools. ASAP computers are ideal for applications where low cost, high reliability, and a quick time-to-market are priorities.

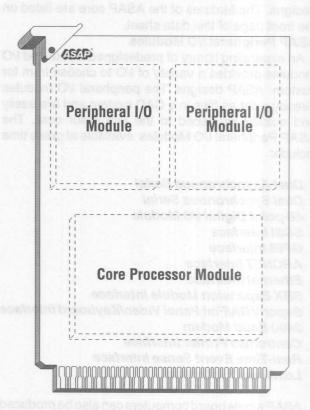
ASAP Peripheral I/O Modules are chosen by the user from an established library of modules and then interfaced directly to the ASAP Core Processor

Module. Because all ASAP computers utilize Core Processor Modules, they all feature STD 32® and STD-80 Series bus-compatibility, ample on-board memory capacity, and stand-alone operation. A wide range of functions such as counter/timers, interrupt controllers, RS-232 serial ports, and watchdog timers is also found on the Core Processor Modules.

ASAP product development includes a complete hardware prototyping platform utilizing STD cards in an STD card cage. Software development tools include Ziatech's STD Device Driver Package (STD DDP), supporting the various I/O modules, and the choice of STD ROM or STD DOS software development tools for ROM-based or DOS-based ASAP computers.

ASAP Core Processor Modules feature:

- Choice of processor
- 8088/8086 code-compatible
- 64 Kbyte I/O address range
- STD 32 and STD-80 compatible
- STD 32 multiple bus-master operation
- One RS-232 serial port
- One interrupt controller
- 16-bit counter/timers
- DMA controller
- Real-time clock, optional battery
- AC/DC power-fail detection
- Single stage watchdog timer
- Push-button reset
- Dynamic 8- and 16-bit bus sizing
- Low power CMOS with sleep mode
- Software-programmable LED
- Burned in at 55° C and tested to guarantee reliability





Functional Considerations The ASAP Program

An ASAP (Application Specific Automation ProcessorTM) single board computer (SBC) can be custom tailored to fit many embedded applications exactly. The ASAP program is intended for high volume (400 boards or more per year) applications where a low cost, highly-integrated single board computer is required. The prototyping cost, payable in three installments during the development process, includes the first 25 ASAP boards and the development tools. For this reason, potential ASAP users should be sure of their system requirements and production quantities before entering the ASAP program.

ASAP Core Processor Modules

The core processor module provides the processor, memory, and numerous functions useful in most embedded applications. Because the ASAP Core Processor Module is a proven circuit and is the primary component of all ASAP products, an ASAP SBC can be created without a lengthy design effort. The core module typically contains over 1,260 circuit interconnections, all of which remain unchanged in all ASAP designs. The features of the ASAP core are listed on the front page of this data sheet.

ASAP Peripheral I/O Modules

An expanding library of predesigned and tested I/O modules provides a variety of I/O to choose from for custom ASAP designs. The peripheral I/O modules already exist as files in a CAD system and are easily and quickly interfaced to the processor core. The ASAP Peripheral I/O Modules available at press time include:

Dual Asynchronous Serial
Dual Synchronous Serial
48-point Digital I/O Module
SCSI Interface
GPIB Interface
ARCNET Interface
Ethernet Interface
SBX Expansion Module Interface
Super VGA/Flat Panel Video/Keyboard Interface
2400 Baud Modem
Centronics Printer Interface
Real-Time Event Sense Interface
LonWorks™ Interface

ASAP single board computers can also be produced with custom I/O functions not found in the standard library of ASAP Peripheral I/O Modules. The development time and prototyping charge will be slightly higher for an ASAP design incorporating custom I/O functions. Some custom I/O functions may become standard ASAP Peripheral I/O Modules in the future; in this way, the library of standard modules continues to

grow. Contact Ziatech's ASAP product manager if you have questions about an I/O function not yet listed as standard.

Development Tools

Users who benefit most from the ASAP program are those with a product that must get to market quickly. However, receiving 25 pre-production ASAP prototypes in a short period of time has little value if the application software is not ready to run at that time also. To assist the user in developing software for his ASAP computer in parallel with prototype production, Ziatech offers four development tools for accelerating the software development process.

1. ASAP Hardware Prototyping Platform

A multiple board system that functionally duplicates the desired ASAP SBC may be quickly assembled using an STD card cage, a few STD cards, and/or SBX expansion modules. This ASAP Hardware Prototyping Platform, while not matching the finished ASAP board in physical size, does provide a functional equivalent. It can run the software and can interface to real world I/O. The core processor module is available on one of Ziatech's standard single board computers (ZT 8801, ZT 8901, ZT 8902). The functional blocks of the ASAP Peripheral I/O Modules are found on individual STD cards, or, in some cases, on SBX expansion modules which may be plugged onto the SBC.

2. STD ROM Software Development System

STD ROM is a software tool for developing code for ROM-based systems. STD ROM, which provides user-friendly programming and debugging tools, is available for any ASAP computer. Please refer to the STD ROM data sheet for a detailed description of this development tool for ROM-based systems.

3. STD DOS Development and Operating System

All ASAP boards are capable of running the STD DOS operating system and associated development tools and utilities. STD DOS is simply MS-DOS (Version 5.0) and Ziatech's AT-compatible BIOS in EPROM or flash EPROM, with the addition of several features useful in embedded control environments. PROM and RAM disks are supported, as well as host communication with a PC over a serial port.

Ziatech's Virtual System Console (VSC) utility allows a host PC to act as development tool for the target ASAP computer. The STD DOS data sheet provides a more detailed description of the STD DOS Development and Operating System.

4. STD Device Driver Package (STD DDP)

To aid ASAP users in writing code for the various ASAP Peripheral I/O Modules and peripherals found on the ASAP Core Processor Module itself, a device driver package called STD DDP is provided at the beginning of the ASAP development cycle. The STD DDP drivers are written in C and can be linked to the user's application program. C libraries can be linked to

3

C, C++, Assembly language, and QuickBASIC. The driver modules found in STD DDP can be used with both STD ROM and STD DOS ASAP computers. Some drivers not found in Ziatech's standard STD DDP package may require four weeks for delivery after the start of the ASAP development process. For a more detailed description of this device driver package, please refer to the STD DDP data sheet.

If the Application Specific Automation Processor sounds like a solution for an application, contact Ziatech's ASAP product manager or a local sales representative for quote and delivery schedule.



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4

STD Bus I/O Control Processors

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STD Bus I/O Control Processors Product Feature Guide

Product	Processor	CPU Speed MHz	RAM Capacity	EPROM/ Flash Capacity	Max. Memory Address	Serial Port(s)	Parallel lines	Other I/O	Counter/ Timers	Bus Data Width	Real-Time Clock	Interrupts	-40° to +85° C
ZT 8830 Intelligent I/O Control Processor	8088-2	8	32 KB	32 KB	64 KB	(1) RS-232/422	16	SBX	5 16-bit	8	1	8	
ZT 8832 Intelligent I/O Control Processor	NEC V40	8	544 KB	480 KB	1 MB*	(1) RS-232 (1) RS-232/ 485	24	SBX	3 16-bit	8		8	
ZT 89CT30 Integer DSP Control Processor	M56001	27	384 KB	128 KB	192 KB	(1) RS-485 (1) RS-232/ 485	24	SBX		8		8	٠
ZT 8932 Intelligent, Multi-Channel Serial Controller	V53	16	1 MB	1 MB	16 MB	(6) RS-232 (2) RS-232/ 485 (1) RS-232 (3-wire)	8		3 16-bit	16	1	8	

[◆] Feature included or available ▲ On-board memory addressing only

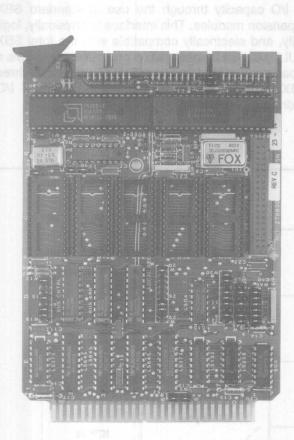
ZT 8830

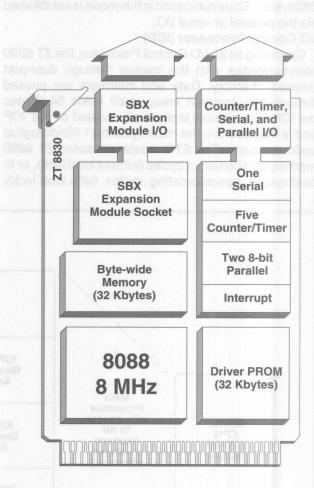
A single board 8088 computer that operates as an Intelligent I/O Control Processor

The ZT 8830 is designed for data acquisition, communication, and robotics applications where real-time performance and high-speed programmable I/O are requirements. This 8088-based STD Bus computer can function as an intelligent I/O Control Processor (ICP) or as a single board computer, depending on the user's application.

As an ICP, the ZT 8830 "teams up" with the STD processor to form a multiprocessing STD Bus system.

The ZT 8830 can be used as a single board computer in situations that require low-cost, compact computer power. Operation in the single board (non-STD Bus) mode requires only the addition of electrical power.





- 8 MHz 8088 processor
- Eight-level, vectored interrupt controller
- · On-board and external interrupt capability
- One 28-pin EPROM socket (32K capacity)
- Four 28-pin RAM sockets (32K capacity)
- Two 8-bit parallel I/O ports
- Eight control registers

- Serial port with option for RS-232 or RS-485
- Optional DOS Multiprocessing Extension (DOS MPX) software
- Five 8-bit counter/timers
- SBX Expansion Module socket
- Burned-in at 55° C and tested to guarantee reliability



Functional Considerations

Central Processor

The ZT 8830 has an 8.192 MHz 8088 central processor. The CPU accesses local on-board memory and I/O, but cannot access off-board memory, or I/O, or interact with an 8087 Math Coprocessor. Interrupts can be sent to the STD Bus backplane.

Single Board Computer Mode

The ZT 8830 can operate as a stand-alone single board computer with on-board memory and I/O.

Free Mode

The ZT 8830 can operate as a loosely coupled parallel processor in an STD Bus system. The STD Bus master can be any STD processor (8085, 8088, Z80, 6809, etc.). Communication in this mode is established via the parallel or serial I/O.

I/O Control Processor (ICP)

Operating as an I/O Control Processor, the ZT 8830 communicates with the master through dual-port (shared) memory. Data and interrupts are passed through this common area, which holds 64 Kbytes per ICP. The memory is physically located on the ICP and is mapped into the main system's 1 Mbyte logical address space. The STD master accesses ZT 8830 memory on alternating cycles (without local lock), or in continuous, non-alternating cycles (with local lock).

Memory System

The ZT 8830 supports 32 Kbyte of EPROM and four 8 Kbyte static RAMs for a total of 32 Kbytes of RAM. **Serial I/O**

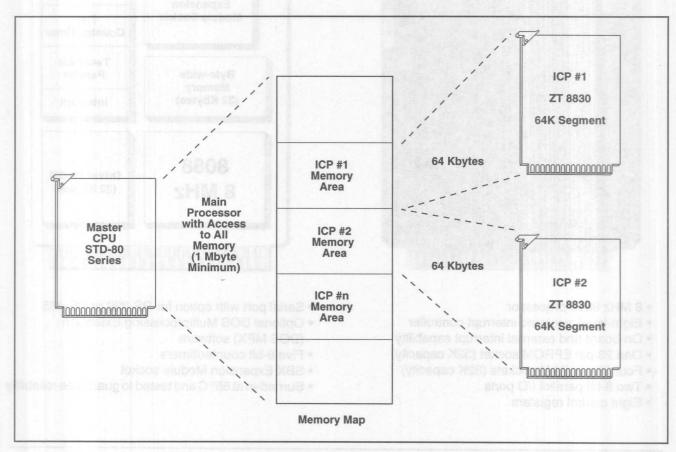
The ZT 8830 has one asynchronous serial I/O port with an on-board programmable baud rate generator. Serial line drivers can be added with optional Ziatech off-board interface adapters for RS-232 or RS-485 compatibility.

Parallel I/O

Two 8-bit, parallel I/O ports are provided. Port 1 is bidirectional and bit-programmable. Port 2 is bidirectional and nibble (4 bits) programmable. Both ports are combined for bidirectional, asynchronous, and parallel communication with handshake.

SBX Expansion Interface

One of the most powerful aspects of the ZT 8830 is its I/O capacity through the use of standard SBX expansion modules. This interface is physically, logically, and electrically compatible with the Intel SBX MULTIMODULE specification and makes available a broad array of I/O functions. The ZT 8830 uses three SBX address modes for up to 64 bytes of I/O address capability.



The ZT 8830 ICP and the STD Bus master processor communicate through 64 Kbytes of dual-port RAM on the ICP.

Counter/Timers

The ZT 8830 features five 8-bit programmable counter/timers and a programmable pre-scaler to give the ZT 8830 the capability to accurately measure time and count off-board events. Four counter/timers can be programmably cascaded into two 16-bit timers; one of the 8-bit counter/timers can be reset to its initial value by an external signal.

Interrupt Controller

The interrupt controller vectors eight priority levels. Vectored interrupts can be generated from external TTL signals, serial or parallel I/O activity, counter/timer activity, SBX module interrupts, or STD master/ICP interaction.

Software Development Considerations DOS MPX

Ziatech's DOS Multiprocessing Extension (DOS MPX[™]) is a development and an operating environment that provides high-level support for designers developing STD DOS (MS-DOS on STD Bus) applications with the ZT 8830.

DOS MPX is comprised of a boot ROM for the ICP, an installable device driver for the system's master processor, and a utility for downloading programs to ICPs. The Virtual Processor Console (VPC) program provides a flexible user interface to the ICPs.

Software development for the ZT 8830 ICP is simplified by the use of DOS MPX, which allows programmers to develop applications with a high-level language such as "C." Any or all of the components of DOS MPX can also be used in the run-time environment. (See the DOS MPX data sheet for more details.) STD ROM

The ZT 8830 I/O Control Processor is also supported by STD ROM. The STD ROM development environment is designed for users who want to develop ROM-based applications using high-level languages like "C," but don't want the cost and overhead of an operating system in their final application.

The STD ROM package includes Paradigm DEBUG/RTTM, Ziatech PDREMOTE/ROM EPROM and Paradigm LOCATE, and startup libraries. This allows the developer to write programs in Microsoft or Turbo C®, debug these programs at the source level on the actual hardware, and make a final target EPROM of the application (see the STD ROM data sheet).

Specifications

Electrical

Compatible with STD-80 Series Bus, up to 8 MHz.

Power Output	r Output Min.			
Supply Voltage, V _{CC}	4.75V	5.00V	5.25V	
Supply Current, V _{CC} = 5.0V		0.85A	1.7A	
Aux Voltage, V _{aux+}	11.4V	12.0V	12.6V	
Aux Current, V _{aux+} = 12.0V	-	0.15A	0.25A	
Aux Voltage, V _{aux} -	-12.6V	-12.0V	-11.4V	
Aux Current, Vaux- = -12.0V	-	0.15A	0.25A	

Note: Vaux+ and Vaux- are needed only if the RS 232 interface adapter is installed.

Data Rates
 Serial I/O:

 1.024 Mbaud maximum with external baud clock, 29.3 Kbaud maximum with on-board baud rate generator

Parallel I/O:

- 228 Kbytes/second maximum STD master block transfer
- 380 Kbytes/second maximum STD master block transfer
- 380 Kbytes/second maximum at 5 MHz, 600 Kbytes/second maximum at 8 MHz, in lock configuration

Mechanical

- Size- and pin-compatible with the STD Bus and SBX MULTIMODULE specifications
- Measures 4.5" x 6.5" (11.4cm x 16.5cm)
- Occupies two 0.625" (1.6cm) spacing card slots with SBX module installed
- Connectors

P1:	56-pin card edge-connector on 0.125"
	(3.2mm) spacing for the STD Bus
J1:	16-pin parallel channel 2
J2:	16-pin parallel channel 1
J3:	16-pin serial channel
J4:	36-pin SBX expansion module

Environmental	Misia Rushing , a reshiri
Operating Temperature	0° to 65° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

Reliability

MTBF: 59 years

MTTR: five minutes (based on board replacement)



The minimum configuration of the ZT 8830 does not include RAM, PROM, or software and is ordered as: ZT 8830-P0R0S0.

ZT 8830

I/O Control Processor

ZT M8830

I/O Control Processor manual

Must choose one option from each category: PROM Options

PO No EPROM

P1 32 Kbyte EPROM, 170ns

RAM Options

RO No RAM

R1 32 Kbytes RAM

Software Options

SO No software installed on board

S1 DOS MPX boot software

(Requires Options P1R1 or greater)

Accessories

Cables (see Data Book cable section for details):

ZT 90011 RS-232 adapter board with 40" (1m)

cable and 25-pin female D-shell

ZT 90012 RS-422 adapter board with 40" (1m)

cable and 25-pin female D-shell

ZT 90021 10' (3m), 50-pin to 50-pin card edge

ZT 90072 10' (3m), 50-pin both ends ZT 90137 2' (0.6m), 50-pin both ends

Boards (see separate data sheets for details):

ZT 2224 24-Line Termination Assembly

ZT 2225 Industrial I/O Cable Adapter

ZT 2226 24-Channel I/O Mounting Rack

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.

ZT 8832

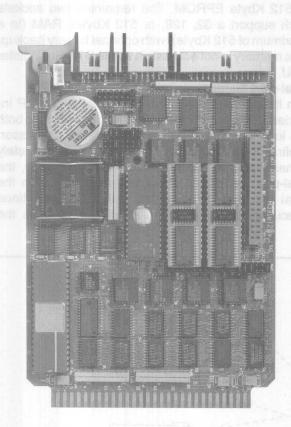
I/O Control Processor

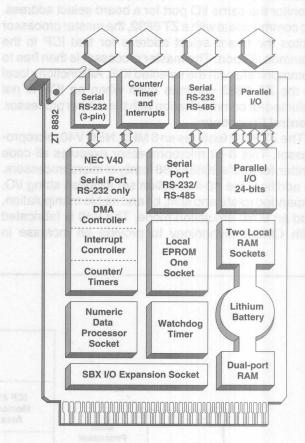
A single board V40 computer with a large I/O complement for intellegent I/O functions

The ZT 8832 I/O Control Processor (ICP) is an 8 MHz, V40-based single board computer designed to operate by itself or as an intelligent control processor in an STD Bus system. It increases system throughput by managing time-critical operations and includes a large complement of on-board I/O and expansion capability. Use of the ZT 8832 simplifies complex systems because it allows them to be partitioned into a series of tasks assigned to one or more ICPs.

The ZT 8832 and the STD master processor communicate through 32 Kbytes of dual-port RAM and I/O-mapped control and status registers located on the ZT 8832. The ZT 8832 does not directly access other STD I/O or memory cards, and therefore does not restrict STD backplane throughput.

The ZT 8832 is supported by Ziatech's DOS Multiprocessing Extention (DOS MPX), which integrates multiprocessing into the DOS environment.





- 8 MHz, V40 microprocessor
- 512K ROM/512K RAM capacity
- 32 Kbyte dual-port RAM (populated)
- Optional battery backup on all RAM
- Two serial ports (V40, 82050) RS-232/485
- Three 8-bit parallel ports, Opto 22 compatibility
- SBX expansion interface with DMA support
- Three 16-bit counter/timers (V40)

- Interrupt controller (V40)
- Push-button reset
- Two-stage watchdog timer
- 8087 Numeric Data Processor socket
- 20-/24-bit STD memory decoding
- Optional DOS Multiprocessing Extension (DOS MPX)
- Optional PROM-based debugger



Functional Considerations I/O Control Processor (ICP)

The ZT 8832 can operate as a stand-alone single board computer or as an I/O control processor (ICP), communicating with a master processor through 32 Kbytes of dual-port memory. The memory is physically located on the ICP and is mapped into the main system's address space.

Board Select Option

One ZT 8832 ICP occupies 32 Kbytes of STD addressing space. For applications using multiple ICPs, each ICP can be mapped into a unique 32 Kbyte space or, by using the board select option, up to seven can be mapped into a common 32 Kbyte space. This option is enabled by mapping each ZT 8832 to the same memory address range and to a unique board select address. In operation, all commonly mapped ZT 8832 ICPs monitor the same I/O port for a board select address. To communicate with a ZT 8832, the master processor writes the board select address for that ICP to the common I/O port. The master processor is then free to communicate with the selected ICP. All functions local to the ZT 8832 continue even when an ICP is not selected for communication with the master processor. **Central Processor**

The ZT 8832 features an 8 MHz, NEC V40 microprocessor. This 8-bit microprocessor executes all code written for Intel's 8088/8086 family of microprocessors. In addition, the 40-instruction set includes string I/O, expanded rotate and shift, bit and nibble manipulation, and an 8080 emulation mode. The V40 is fabricated with CMOS technology to provide an increase in

operating temperature range and noise immunity, with a reduction in power consumption.

Extended Math Performance

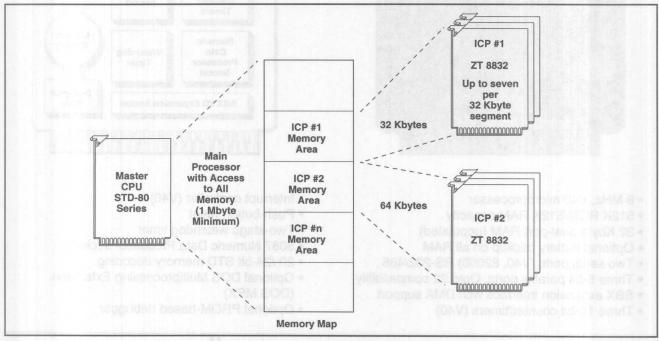
The Intel 8087 Numeric Data Processor (NDP) can be added to the ZT 8832 ICP for applications that require additional math capability. Plugging the NDP into the socket on the ZT 8832 provides 68 added instructions for extended arithmetic, trigonometric, exponential, and logarithmic functions. These added instructions are supported by seven additional data types, including integers (16-, 32-, and 64-bit), floating-point (32-, 64-, and 80-bit), and BCD (18-digit). Using the NDP increases performance up to 100 times that of equivalent routines implemented in software.

Local Memory

The ZT 8832 ICP is populated with three 32-pin memory sockets dedicated for use by the V40 microprocessor. One socket supports an 8, 16, 32, 64, 128, or 512 Kbyte EPROM. The remaining two sockets each support a 32, 128, or 512 Kbytes RAM (to a maximum of 512 Kbyte), with optional battery backup. This memory is not accessible by the STD Bus master CPU.

Dual-port Memory

In its standard configuration, the ZT 8832 ICP includes 32 Kbytes of RAM that are accessible from both the local ICP processor and the master processor. Arbitration for simultaneous access is done completely in hardware. To increase system performance, the dual-port memory is physically separated from the local memory. This permits the ICP to continue executing local operations at full speed while the



The ZT 8832 ICP and the STD Bus master processor communicate through 32 Kbytes of dual-port RAM on the ICP.

master processor is accessing the shared memory. The master processor can also continue operations while the ICP processor accesses dual-port memory. Only when both processors attempt a dual-port memory access is the operation of one suspended until the other is completed. Repetitive accesses from both processors are interleaved on a machine cycle basis. The dual-port memory also supports software-programmable interrupts, a locking mechanism, and battery backup. The locking mechanism allows either the master processor or the local ICP processor to keep the other from accessing the dual-port memory until the lock is removed.

Serial I/O

The ZT 8832 includes two asynchronous serial communication channels, each with a programmable baud rate generator. The NEC V40 provides one serial channel (a subset of the 8251A) configured as RS-232 DTE. This serial channel supports the transmit data (TXD) and receive data (RXD) signals only, and is available through a 3-pin frontplane connector. An optional one-meter cable (ZT 90069) joins the 3-pin connector to a male 25-pin, D-shell connector.

The second serial channel (Intel 82050 or equivalent) is functionally equivalent to the serial controller used in the IBM PC. This channel supports all handshaking and modem control signals and can be jumper-programmed for RS-232 or RS-422A/485. Other features include loopback diagnostics, maskable interrupt generation, and jumper-selectable DCE or DTE configuration. The 82050 serial channel is accessed through a 14-pin frontplane connector. Optional one-meter cables (ZT 90014 and ZT 90027) connect the 14-pin connector to a male or female 25-pin, D-shell connector, respectively.

Parallel I/O

There are three, 8-bit parallel ports on the ZT 8832, for a total of 24 I/O lines. Each I/O line can be programmed as input, or output with readback. The I/O signals and fused power are accessible through a 26-pin, frontplane connector. An optional one-meter cable (ZT 90068) connects the 26-pin connector directly to an 8-, 16-, or 24-position I/O module mounting rack, such as those manufactured by Ziatech and Opto 22.

Interrupt Controller

The ZT 8832 includes one programmable interrupt controller (8259A architecture) with eight inputs. Features of the interrupt controller include level- and edge-triggered sensing, fixed and rotating priorities, and the ability to mask individual inputs. Two of the interrupt request inputs are available through a frontplane connector to be used as needed by the application. The remaining inputs are dedicated to interrupt sources to support interrupt-driven data transfers from the master processor through

dual-port memory. These interrupt sources include serial controllers (for interrupt-driven data transfers), SBX modules (for interrupt-driven I/O), and the STD Bus.

Counter/Timers

The ZT 8832 has three independent 16-bit counter/ timers (8254 architecture) that can be used as timers or event counters. There are six programmable counter/ timer modes: interrupt on end-of-count, frequency divider, square wave generator, software-triggered, hardware-triggered, and retriggerable one-shot. One of the counter/timers is available for application use through a frontplane connector. The other two counter/timers are dedicated for uses such as baud rate generation for the NEC V40 serial channel, and interrupt generation for timed and periodic interrupts.

Watchdog Timer

The ZT 8832 includes a selectable, two-stage watch-dog timer. If the application fails to strobe the watchdog timer, the ZT 8832 sends a non-maskable interrupt to the V40. The non-maskable interrupt service routine must take corrective action that includes strobing the watchdog timer within a certain time period or the ZT 8832 is reset. The watchdog timer is enabled through jumper selection.

DMA Controller

Direct Memory Access (DMA) provides high-speed data transfer between ZT 8832 memory and SBX expansion module I/O. The DMA controller performs the memory and I/O operation in a single machine cycle for a data transfer rate of up to 2 Mbytes per second. The following transfers are supported: SBX I/O to and from the local memory sockets, and SBX I/O to and from the dual-port RAM.

SBX Expansion Interface

An on-board SBX expansion socket allows users to customize the I/O capabilities of the ZT 8832 to the needs of the application. The SBX interface is electrically, mechanically, and functionally equivalent to the Intel SBX MULTIMODULE standard, including DMA support for high-speed data transfers. This makes it compatible with hundreds of off-the-shelf I/O modules.

Battery Backup

An optional battery can be installed to support the RAM during system downtime. The battery will support the 32 Kbyte dual-port RAM and can be configured to support all the RAM.

Software DOS MPX

Ziatech's DOS Multiprocessing Extension (DOS MPX) is a development and an operating environment that provides high-level support for designers developing STD DOS (MS-DOS on STD Bus) applications with the ZT 8832.



installable device driver for the system's master processor, and a utility for downloading programs to ICPs. The Virtual Processor Console (VPC) program provides a flexible user interface for the ICPs. (See the DOS MPX data sheet for more details.)

STD ROM

The ZT 8832 I/O Control Processor is also supported by Ziatech's STD ROM Development package. STD ROM is designed for users who want to develop a ROM-based application using high-level languages like C, but don't want the cost and overhead of an operating system in their final application (see STD ROM data sheet).

Specifications

Electrical

- Size- and backplane-compatible with the STD 32 and STD-80 specifications
- RAM data retention for optional battery backup:
 5 yrs. typical, 2 yrs. minimum for dual-port RAM

Power Output	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00A	5.25A
Supply Voltage, Vcc = 5.0V	-	1.0A	1.8A
Aux Voltage, Vaux+	11.4V	12.0V	12.6V
Aux Current, Vaux+ = 12.0V	#C +fT .C	4mA	8mA
Aux Voltage, Vaux-	-12.6V	-12.0V	-11.4V
Aux Current, Vaux- = -12.0V	telement p	4mA	8mA

Mechanical

- Size- and backplane-compatible with the STD 32 and STD-80 mechanical specifications
- SBX MULTIMODULE-compatible
- Measures 4.5" (11.4cm) by 6.5" (16.5cm)
- Height measured from component surface:
 Without battery = 0.38" (9.7mm)
 With battery = 0.43" (10.9mm)
- Weight = 4 oz. (113.4g)
- Connectors

P1: 56-pin card edge-connector on 0.125" (3.2mm) spacing for the STD Bus

J1: 26-pin parallel channel

J2: 14-pin serial channel

J3: 10-pin interrupt and counter/timer

J4: 36-pin SBX expansion module

J5: 3-pin serial channel

Environmental		
Operating Temperature	0° to 65° Celsius	
Storage Temperature	-40° to +85° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

• MTBF: 20 years

• MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8832 I/O Control Processor

ZT M8832 I/O Control Processor manual

Must choose one option from each category: PROM Options:

P0 No PROM installed P1 128 Kbytes PROM P2 512 Kbytes PROM

RAM Options:

RO No RAM

R1 128 Kbytes static RAM, 120ns

(extended temperature)

R2 512 Kbytes static RAM, 120ns

(extended temperature)

Software Options:

S0 No software

S1 DOS MPX Boot Software

(Requires Options P1R1 or greater)

Choose Miscellaneous options as needed:

Miscellaneous Options:

B 1 amp-hour lithium battery (extended temperature)

M 10 MHz 8087 Numeric Coprocessor

and 8087-2 math coprocessor (extended temperature)

(Oxtorided to

Accessories

Cables (see Data Book cable section for details):

ZT 90014 40" (1m), 14-pin to 25-pin female
ZT 90021 10' (3m), 50-pin on both ends
ZT 90027 40" (1m), 14-pin to 25-pin male
ZT 90068 40" (1m), 26-pin to 50-pin header
and 50-pin edge
ZT 90069 39" (1m), 3-pin to 25-pin female
ZT 90090 40" (1m), 26-pin on both ends

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix. Batteries are not covered by Ziatech's warranty.



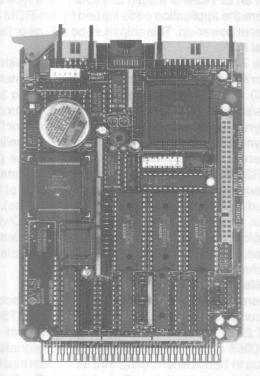


ZT 89CT30

Integer DSP Control Processor

Digital Signal Processor provides high-speed, real-time signal processing

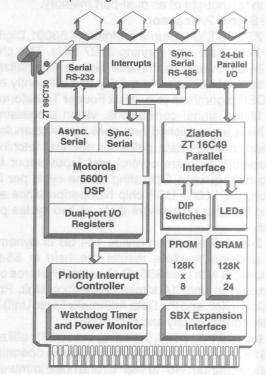
The ZT 89CT30 Integer DSP Control Processor is a single board computer based on the 27 MHz Motorola 56001. Designed to operate alone or as an I/O Control Processor (ICP) for STD Bus systems, it performs specialized signal processing operations as well as I/O management of a high-speed serial interface. The DSP Control Processor has a large complement of onboard I/O and expansion capability through an SBX connector and a high-speed serial channel. One or more ZT 89CT30 boards can be used to simplify complex tasks such as audio filtering, Fast Fourier Transforms (FFT), vibration analysis, or vision processing.



- 27 MHz Motorola 56001 24-bit integer DSP
- Three 32-pin static RAM (SRAM) sockets
- One 32-pin PLCC EPROM/flash memory socket
- Optional battery backup on all RAM
- SBX expansion interface
- High-speed interrupt/DMA I/O interface
- Dual-ported I/O register interface to STD Bus
- Priority Interrupt Controller for STD Bus (82C59)
- 2 Kbyte EEPROM for parameter storage

The ZT 89CT30 and the STD Bus master processor communicate through 16 dual-port I/O registers and an on-board Priority Interrupt Controller (PIC). STD backplane throughput is not restricted since the board does not directly access other STD Bus I/O or memory cards. Similarly, the dual-port I/O accesses by the master processor do not affect the DSP's execution performance.

A broad selection of software tools and application programs supports the 56001 DSP chip on the ZT 89CT30. These include a debugger, an assembler, a linker and simulator, a "C" compiler, and numerous FFT and filter packages.



- CMOS/wide temperature operation (-40° to +85° C)
- RS-232/485 (4-wire) asynchronous serial port
- RS-485 synchronous serial port
- Watchdog timer
- 24 bits of digital I/O (12mA sink current), compatible with Ziatech's ZT 2226 and Opto 22, etc.
- Push-button reset for local processor
- Burned-in at 55° C and tested to guarantee reliability

Note: CT denotes CMOS, TTL backplane-compatible and extended temperature operation of -40 $^\circ$ to +85 $^\circ$ C. (Users should make adjustments for temperature rise in enclosures.)



Functional Considerations Integer DSP I/O Control Processor

The ZT 89CT30 can operate as a stand-alone single board Digital Signal Processor, or as an I/O Control Processor (ICP) communicating with a master processor on the STD 32® or STD Bus. This communication occurs through eight I/O-addressed registers which are physically located in the DSP chip and are mapped into a jumper-selectable location in the main system's I/O address space.

Board Select Option

Multiple ZT 89CT30 boards can be used in a single system for added processing power. This is accomplished by jumpering each board at a different I/O address. The DSP chip occupies the first eight addresses, and the on-board slave Priority Interrupt Controller (PIC) redundantly occupies the second eight.

The DSP's processing is not impaired by the master CPU's access to these addresses, nor is it put on hold during these accesses. The registers inside the DSP chip can be thought of as dual-port memory.

Digital Signal Processor

The ZT 89CT30 features a Motorola 56001 Digital Signal Processor chip running at 27 MHz. This chip uses 24-bit integer arithmetic with a specialized instruction set designed to quickly and efficiently execute DSP algorithms (e.g., Fast Fourier Transforms, digital filters, signal correlations, vision processing, etc.). This is accomplished through Multiply Accumulate operation, multiple data paths for operand fetching, and versatile program control and input/output for moving data quickly. Operating at one cycle per instruction, the 56001 DSP chip has performance exceeding 50 MHz processors that use two cycles per instruction.

The 24-bit data paths provide 144 dB of dynamic range and intermediate results are held in 56-bit accumulators with over 336 dB of range. The three onchip execution units (Address Generation Unit, Program Controller, and the Data Arithmetic Logic Unit) all operate independently and in parallel.

The entire ZT 89CT30, including the 56001, utilizes CMOS technology to provide an increase in operating temperature range (-40° to +85° C) and noise immunity, and a simultaneous reduction in power consumption. The 56001 has a WAIT instruction that shuts off the central processor clock, and a HALT instruction to minimize power consumption when processing is not required.

Local Memory

The 56001 has a 32-word (all references to "word" imply 24 bits) bootstrap ROM for loading the user's application from either the on-board PROM or the master CPU on the STD Bus. The DSP chip also has a 512-word program memory, and preprogrammed ROMs containing the Mu-law and A-law to linear

expansion tables and a full four-quadrant sine-wave table. In addition, there are 256 words each of X and Y memory on the chip for zero-wait data accesses.

The ZT 89CT30 has three JEDEC 32-pin sockets for Static RAM which will accept either 32 or 128 Kbyte SRAMs for data and program storage. With the 128 Kwords of SRAM, the user may store up to 32 Kwords of program instructions and 48 Kwords each of X-address data memory and Y-address data memory. The following table gives the required memory speed for 0, 1, or 2 wait state operation of the 27 MHz DSP:

# Wait States	32 Kbyte parts	128 Kbyte parts
0	25ns *	35ns
vera 1 december	55ns *	70ns
2	100ns	100ns
2		100ns

* for non-battery-backed use, the 32 Kbyte parts can have the same speed as 128 Kbyte parts

There is one 32-pin, rectangular PLCC socket for either an EPROM or a flash EPROM (5 volt type only) to store the application code loaded by the ROM boot loader at power-up. This chip must be 200 ns or faster. **Serial I/O**

The ZT 89CT30 includes a serial channel with RS-232 or RS-485 levels (Serial Communication Interface – SCI). The channel supports baud rates up to 3.375 Mbits/second. This channel can be either synchronous or asynchronous and jumpered as either DCE or DTE. In async mode there is a Clear To Send input available.

There is also a Synchronous Serial Interface (SSI) with RS-485 levels set-up for 2-wire multidrop data with four additional RS-485 general purpose pairs of lines (including the clock and three serial control lines). The SSI is double buffered and supports Time Division Multiplexed networks as well as normal and on-demand modes. Many DSP analog-to-digital peripherals use this channel.

Parallel I/O

There is an on-board 24-bit parallel I/O interface that can connect to an Opto 22 rack to the ZT 89CT30 via a ZT 2225 Industrial I/O Cable Adapter card or a ZT 90068 cable. These bidirectional I/O signals can sink up to 12 mA when configured as outputs and have 100k ohm pullup resistors. Fused, 1 amp +5 volt power is also available on the connector.

Interrupts

Several on-board actions, and four software-initiated actions, can generate individually vectored interrupts to the STD Bus master processor. Four of the parallel lines can detect a change in signal level and cause an interrupt to the 56001. The DSP can also be interrupted by signals from the SBX and the watchdog timer.

Watchdog Timer

The ZT 89CT30 includes a two-stage watchdog timer that, when enabled, must be strobed at a periodic rate

4

of less than 45ms, or an interrupt to the 56001 DSP will result. After 100ms, the system is permanently reset and can be restarted only by an STD Bus SYSRESET or by pushing switch PB1 on the ZT 89CT30.

SBX Expansion Interface

An on-board SBX expansion socket allows users to customize the I/O capabilities of the ZT 89CT30 according to the needs of a specific application. This IEEE 959 interface uses 8- or 16-bit data and has limited DMA support. The SBX can be interrupt/DMA driven and can execute much faster than other SBX interfaces if the software programs fewer DSP wait states. This socket supports hundreds of off-the-shelf I/O modules. For specialized applications, many users design and build their own I/O interfaces that utilize the SBX socket on the ZT 89CT30. Contact Ziatech for a list of available SBX modules or for information on prototyping cards in the SBX format.

Battery Backup

An optional battery can be installed to supply the SRAMs with power during system downtime. The battery supports SRAMs of any speed, but the life of the battery is a strong function of the standby current (faster memory chips have very high currents). For longest battery life, use 100ns SRAMs.

Specifications

Benchmarks

20-tap FIR filter	500 kHz
64-tap FIR filter	190 kHz
• 3x3 matrix multiply by 3x1	1.259 µsec
• 1024-point complex FFT	2.453 ms

Electrical

· Power Supply:

Power Req. *	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, V _{CC} =5.0V		0.6A	1.0A
Aux Voltage, V _{aux+}	11.4V	12.0V	12.6V
Aux Current, Vaux+=12.0V		-	1.0A
Aux Voltage, V _{aux} -	-12.6V	-12.0V	-11.4V
Aux Current Vaux-=-12.0V	- 1	-	1.0A

- * Aux voltage is not required by ZT 89CT30, but is available for use by an optional SBX module.
 - STD 32- and STD Bus-compatible
 - STD I/O Address range: 16 ports located anywhere in 64 Kbyte address space on a 16-byte boundary
 - SBX interface is compatible with Intel Spec. and IEEE 959

Environmental		
Operating Temperature	-40° to +85° Celsius	
Storage Temperature (with battery)	-40° to +85° Celsius	
Storage Temperature (without battery)	-55° to +105° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

Mechanical

- Size- and backplane-compatible with the STD 32 and STD-80 mechanical specifications
- Requires one STD slot without SBX installed
- · Requires two STD slots with SBX
- Height measured from board component mounting surface:

0.38" (0.96cm) without battery 0.48" (1.2cm) including battery 1.15" (2.9cm) including SBX

- Board measures 4.5" (11.4cm) by 6.5" (16.5cm)
- Weight 6 oz. (170g)
- Connectors

P1:	114-pin STD Bus card edge connector with 0.0625" (0.16cm) spacing
J1:	5-pin latching RS-232/485 serial I/O
J2:	10-pin latching interrupt request
J3:	20-pin latching RS-485 sync. serial
J4:	26-pin latching parallel I/O interface
J5:	44-pin latching SBX connector
	(8- or 16-bit)

Data Rates

- J1: Synchronous serial, 3.375 Mbit/sec. maximum
- J1: Asynchronous serial, 422 Kbit/sec. maximum
- J2: Synchronous serial, 6.75 Mbit/sec. maximum

STD 32 Compliance

 I/O Slave: SA8, I, IXP, IXL, ICA
 Note: SA8 is equivalent to STD-80 Series Rev 2.3 (5 and 8 MHz).

Reliability

- MTBF: 20 years
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 89CT30 Integer DSP Control Processor ZT M89CT30 ZT 89CT30 manual

RAM Options (must choose one):

R0 No RAM
R1 96 Kbytes Static RAM, 35ns
R2 384 Kbytes Static RAM, 120ns
R3 384 Kbytes Static RAM, 35ns

Miscellaneous Options:

B 1 amp-hour lithium battery

Accessories

Cables (see Data Book cable section for more details): ZT 90068 40" (1m), flat digital I/O, 26-pin to 50-pin ZT 90090 40" (1m), flat digital I/O, 26-pin both ends ZT 90099 40" (1m), RS-232 serial, 5-pin to 25-pin



of less than 45ms, or an interrupt tothe 56001 DSP will result. After 100ms, the evatem is permanently reset and can be restarted only by an STO Bus SYSRESET or by pushing swings PR1 on the ZT 890T80.

An on-board SRX expension socket allows users to customize the VO capabilities of the ZT 69CT39 according to the meets of a specific application. This conding to the meets of a specific application. This IEEE 959 interface uses 8- or 16-bit data and has limited DMA support. The SBX can be interrupt/DMA driven and data execute much faster than other SBX interfaces if the software programs fewer DSP wait interfaces. This accide septents mundreds of off-the-shelf VO medules. For specialized applications, many users design and build their own VO interfaces that utilize the SBX seeket on the ZF 89CT30. Contact Zeatech for a controtycling cards in the SBX modules or for information on prototycling cards in the SBX format.

An optional battery can be installed to supply the SFAMs with or war during system downtime. The battery supports SFAMs of any speed, but the life of the battery is a strong function of the standby current fester memory chips have very high currents). For langest battery ife, use 100ns SFAMs.

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-Management

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- Aux voltage is not required by ZT 89CT30, but is evailable for use by an optional SBX module.
 - * STD 32- and STD Bus-compatible
- STD VC Address range: 16 ports located anywherein 6+ Kbyte address space on a 16-byte houndary
 - SBX Interface is compatible with Intel Specient IEEE 1989.

Ispinsdooli

- Size- and backplane-compatible with r = 3 to 32
 - * Paquires one STD slot with our SEX in culted
 - Requires two STO state with SID
 - Height measured from board component mounting surface;
 - vialted fundiliw (mo38.0) "88.0"
 - 0.45" (1,2cm) including battery
 - 1.15° (2.8cm) Including SBX
- * Board measures 4.5" (11 Adm) by 6.5 . 15.5cm)
 - * Weight 6 oz. (176g)
 - Consectors
- P1: 114-pinSTD Bascarded connector
- Uti 5-pin istoring RS-232/46 sedai3/O
- teem injuried in painfale iniq-01 ISL
- ishee a 664-169 grindel nid 999 all.
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 - tions which believes the second

Data Rates

- Fundamental se vidivi & E.S. Ishes sucremient B. 14.
- * 31: Asynchronous serial, 422 (Stit/sec. naximum
- - STD 32 Compliance
 - * NO Shive: SAS I, DCP, IXL, ICA
 - Note: SA6 is equivalent to STD-69 Series Tav 2.3 (5 and 8 A8Hz)

Wildelish

- * WEIGH, 25 years
- MTTH: five minutes (based on board includement)
 - r defing internation
 2T ASCT30 Interes DSP Control Processor
 - ZT MBBCT20 ZT 69CT30 marrial
 - AM Opdose (must choose one):
 - RO NORAM
 - R1 96 Kbytes Static RAM, 35m
 - RS 384 Kbytes Static RAM, 36
 - (discellaneous Options)
 - 8 tamp-hour lithaum battery
- Cables (see Data Book cable section for condetails):
- ZT 90088 40" (1m), flat digital VO, 28 ... 10'50 pin ZT 90090 40" (1m), flat digital VO, 28 ... both ends

STO32°

ZT 8932

Intelligent, Multi-Channel Serial Controller

High-density, high-performance, eight-channel serial controller with 16 MHz V53 processor

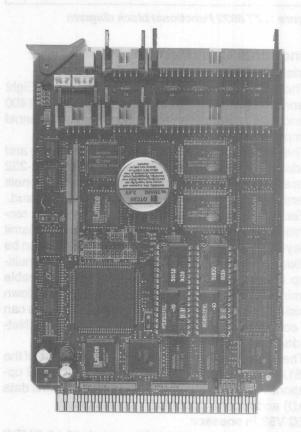
The ZT 8932 is an Intelligent Serial Controller for STD 32® Bus or stand-alone applications. Its on-board 16 MHz V53 (286 class) processor manages eight asynchronous serial channels with a ninth channel available for development and debugging. The eight serial channels include 12 byte FIFOs and full modem handshake capability. Two channels are configurable for RS-485 operation. Communication rates up to 115 Kbaud are supported.

The ZT 8932 and the host processor communicate through 16 Kbytes of dual-port RAM located in the ZT 8932. The RAM is selectable by the host processor so that up to eight ZT 8932 controllers can occupy the same memory space in a system. The dual-port interface supports interrupt driven and locked transfers to reduce bus traffic and increase performance.

Up to 1 Mbyte of on-board RAM and 1 Mbyte of flash EPROM provide ample space for user-written communication applications and offer enough flexibility for stand-alone applications. A version of the board is available without the dual-port logic (ZT 89132).

The ZT 8932 can be ordered with an on-board communications executive and host software driver for DOS (other operating environments will follow). This driver provides extended COM support. Alternatively, users can develop their own communications front-end software using Ziatech's powerful development environment, STD ROM. STD ROM can also be used to develop stand-alone communications applications for the ZT 89132.

- Eight asynchronous RS-232 channels with modem control (CD-CL1400)
- Individual transfer rates to 115 Kbaud
- Combined transfer rates to 19.2 Kbaud
- 16 MHz, V53 (286 class) microprocessor
- 12 byte FIFO support per channel
- Up to 1 Mbyte flash/ROM
- Up to 1 Mbyte total, optional battery backup
- 32 Kbyte dual-port RAM
- Two channels configurable for 2- or 4-wire RS-422/485 operation
- Host interface-compatible with Star Gate[™]
 Avanstar 100 Series software
- Additional RS-232 channel for development and debug
- +5V operation (±12V not required)
- Three 16-bit timers (8254)
- Eight bidirectional digital I/O lines with event sense
- Real-time clock, optional battery backup
- •AC/DC power-fail detection
- Single-stage watchdog timer
- Push-button reset
- User-written applications supported





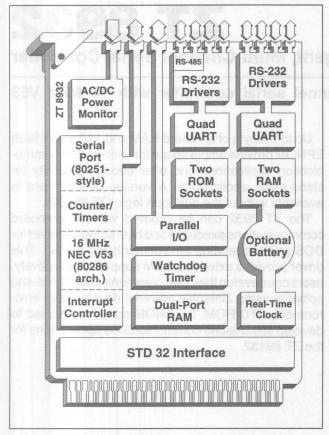


Figure 1. ZT 8932 Functional block diagram

Serial Interface

The ZT 8932 provides nine serial channels. Eight channels are available via the Cirrus Logic CD-CL1400 asynchronous serial controller, and the ninth channel is implemented via the V53 microprocessor.

The CD-CL1400 chip supports all handshaking and modem control signals configured as DTE for RS-232 operation. The overall throughput with all channels operating continuously is approximately 19.2 Kbaud.

Each serial channel features special character recognition/generation and the ability to insert transmit delays in the data stream. One or two channels can be software selected for RS-422/485 operation. For multidrop applications, the ZT 8932 features jumperable termination resistors and socketed pull-up/pull-down resistor SIPs. One or two of the RS-485 channels can be configured for SAE-J1708 for Vehicle Area Networks (VAN).

The V53 provides one serial channel (a subset of the 8251A) optionally configured as DTE for RS-232 operation. This serial channel supports the transmit data (TxD) and receive data (RxD) signals only.

NEC V53 Processor

The NEC V53 is a highly integrated, 16-bit CMOS microprocessor. The V53 includes several standard

peripherals, and has an architecture similar to that of the 80286 CPU. The processor has been optimized to execute instructions up to 20% faster than an 80286 operating at the same clock frequency. The primary difference between the V53 CPU and the 80286 is in the method used to address memory between the 1 Mbyte and 16 Mbyte address range.

The V53 uses an extended addressing scheme to software bank select from the 16 Mbyte physical address range. It does not support the protected address mode available on the 80286.

Memory Addressing

Local memory consists of two pairs of sockets for use by the V53 microprocessor. One pair of 32-pin memory sockets accepts RAM devices (32, 128, 256, and 512 Kbyte) with standard 0.6-inch DIP package. The other pair accepts ROM/EPROM devices (32, 128, 256, and 512 Kbyte) and flash devices (128, 256, and 512 Kbyte) with a standard 32-pin PLCC package. Flash devices requiring +12V for programming can use the ZT 8932's on-board voltage generator with software shutdown capability.

The ZT 8932 does not allow an STD Bus host CPU to access its local memory.

Bus Interface

The ZT 8932 (not the ZT 89132) includes 16 Kbytes of software-selectable RAM that can be accessed by both the V53 microprocessor and the STD 32 host processor. The hardware handles all arbitration for simultaneous access. To increase system performance, the dual-port memory is physically separated from the local memory. This permits the V53 to continue executing local instructions at full speed while a host processor accesses the shared memory. The host processor can also continue to execute instructions while the V53 is accessing dual-port memory. Only when both processors attempt a dual-port access is the operation of one suspended until the other is completed. Repetitive accesses from both processors are interleaved on an instruction basis. The dual-port memory also supports software mechanisms to facilitate software communication. A locking mechanism allows either the master processor or the V53 to keep the other from accessing the dual-port memory until the lock is removed. The host processor can enable one of eight ZT 8932s on the bus via a memory port. This saves valuable BIOS extension memory space in large systems.

Digital I/O Interface

Eight buffered parallel I/O lines can be programmed for input or output with read back operation. The open collector outputs sink 12mA (suitable for driving LEDs, low current lamps, etc.) and do not glitch during power-up or power-down. Event sense capability can optionally generate an interrupt on a negative or positive edge.

ZT 8932 Intelligent, Multi-Channel Serial Controller

Interrupts

The interrupt controller (8259) within the V53 supports eight maskable inputs. Features of the interrupt controller include level- and edge-triggered sensing, fixed and rotating priorities, and the ability to mask individual inputs. There are eight interrupt sources, timer 0, serial I/O, V53 serial I/O, real-time clock, parallel I/O event sense, and STD Bus.

The serial interrupts provide a versatile and efficient mechanism for servicing modem, transmit data, receive data, and error condition service requests. Each service request is "daisy-chained" between the two CL-CD1400 devices. This allows them to arbitrate and set priorities between themselves regarding which type of service request is asserted. Once the request is asserted, the V53 can read a "vector" register and serial channel register within the CL-CD1400 to determine a response. Once executed (load transmit FIFO, read receive FIFO, etc.), it issues an "end-of-service."

Counter/Timers

The V53 includes three independent, 16-bit timers (8254). An interrupt can be generated on the end-of-count for timer 0.

Watchdog Timer

The ZT 8932's watchdog timer monitors system operation. If enabled, the watchdog timer must be strobed at a periodic rate of 100ms by the application software. Failure to strobe the watchdog timer will result in an on-board reset 100 to 600ms later.

Real-Time Clock

The real-time clock uses the National Semiconductor 8572A to perform time keeping functions and includes 44 bytes of RAM. Time keeping features include resolution down to 0.01 seconds, 12- or 24-hour operation, leap year adjustment, rollover status, time comparison and periodic interrupts, and automatic time logging in the event of power failure. With the optional battery installed, these features continue to operate when power is removed.

AC Power-Fail Protection

With the addition of an optional AC transformer, AC power can be monitored to permit an orderly shutdown during a power failure. When AC power falls below an acceptable operating range, a non-maskable interrupt is generated to notify the V53 microprocessor of the impending AC power failure. The application software can then save critical data before the processor is reset by the precision on-board reset circuitry.

Software Support

Intelligent Serial Controller (ISC) Software

The ZT 8932 can be ordered with the Intelligent Serial Controller (ISC) executive software and drivers. The host interface is compatible with the Star Gate Avanstar 100 Series of PC-based controllers. This

includes a software executive on the ZT 8932 that handles all the communication channels and exchanges data with the host processor via buffers in the dual-port RAM. Device drivers on the host processor provide operating system support for the eight serial channels on the ZT 8932. Microsoft® MS-DOS® support is now available with other operating environments under development.

User Written Applications

Users requiring specialized processing of serial data may want to develop their own applications for the ZT 8932's on-board processor. Developing code for the ZT 8932 is relatively simple because the controller is based on PC architecture. Ziatech's STD ROM package supports standard Borland and Microsoft "C" compilers for both source level debugging and embedding in flash EPROM. Additionally, the device driver package includes linkable library routines for buffered, interrupt driven communications over the serial channels. Full "C" source code for these routines lets the user customize them for specific requirements. STD ROM also includes utilities for on-board programming of the flash EPROM, downloading new applications, and communicating through the dual-port RAM. An onboard jumper selects whether to boot a user application or the debugger.

Specifications

Electrical

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, V _{CC} =5.0V	coel Tacillo	0.5A	1.0A

Mechanical

Measures: 4.5" (11.3cm) by 6.5" (16.5cm)

Height: 0.5" (1.3cm)Weight: 6.5oz (184g)

Connectors

P1: 136-pin STD 32 Bus card edge connector on 0.0625" (0.16cm)

spacing

J1, J2: 40-pin latching four channel RS-232

serial I/O

J3: 10-pin latching interrupt

J4: 10-pin latching 8-bit parallel I/O

J5: 3-pin V53 RS-232 serial I/O

J6: 2-pin latching A/C interrupt

J7: 10-pin latching two channel RS-422/ 485 serial I/O

2-position power connector

(ZT 89132 only) STD 32 Compliance

J8:

· Memory Slave: SAI6, SA8-I, IXL

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz)



Environmental		
Operating Temperature	0° to +70° Celsius	
Storage Temperature	-40° to +85° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

Reliability

MTBF: 28 years

MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8932

Intelligent, Multi-Channel

Serial Controller

ZT M8932

ZT 8932 manual

ZT 8932-ISC-DR1

Intelligent, Multi-Channel Serial Controller with on-board executive and installable device drivers for DOS. Includes 256 Kbytes of Boot Block flash memory and 256 Kbytes of RAM.

ZT 8932-ISC-DRx

Support for other operating environments. Contact Ziatech

for more information.

Ordering example for OEM applications: A ZT 8932 Intelligent, Multi-Channel Serial Controller with 256 Kbytes of flash memory, 256 Kbytes of static RAM, and boot loader and flash reprogrammer installed is ordered as: ZT 8932-P1R1S1.

Must choose one option from each category: Flash Options

P1 256 Kbytes flash (boot block), 150ns

RAM Options

R1 256 Kbytes static RAM, 100ns

R2 256 Kbytes static RAM, 55ns

R3 1 Mbyte static RAM, 120ns

R4 1 Mbyte static RAM, 55ns

(option R4 cannot be battery backed)

Software Options

S1 Boot loader, and flash reprogrammer installed

Development Software

ZT 94031

STD ROM Development Environment; STD ROM development system for PROM-based target systems. Includes Virtual Terminal Interface (VTI) installed on PROM, Paradigm LOCATE and startup modules, STD DDP, Paradigm DEBUG/RT, one serial cable, and a PLCC extractor tool.

Accessories

Cables (see Data Book cable section for details):

ZT 90069 39" (1m), 3-pin to 25-pin female

D-shell

ZT 90182 10" (25cm), 40-pin to four 9-pin

male D-shells

ZT 90183 10" (25cm), 40-pin to four 10-pin

headers

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

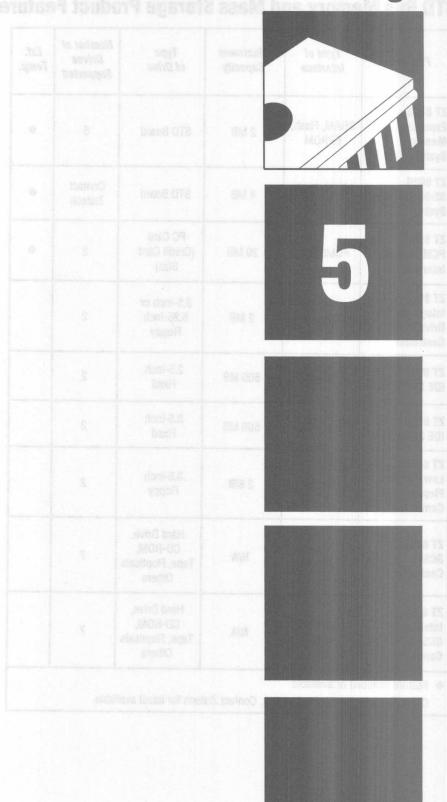
Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.

STD 32 is a registered trademark of Ziatech Corporation. Star Gate is a trademark of Star Gate Technologies, Inc.



5

STD Bus Memory and Mass Storage



STD Bus Memory and Mass Storage Product Feature Guide

Product	Type of Interface	Maximum Capacity	Type of Drive	Number of Drives Supported	Ext. Temp.
ZT 8825 Expanded Memory System	BRAM, Flash, EPROM	2 MB	STD Board	5	*
ZT 8920 32-bit Memory System	SRAM, Flash, EPROM	4 MB	STD Board	Contact Ziatech	+
ZT 8921 PCMCIA 2.0 Interface	PCMCIA 2.0	20 MB	PC Card (Credit Card Size)	2	*
ZT 8950 Integrated Disk Drive/DMA Controller	Floppy	2 MB	3.5-inch or 5.25-inch Floppy	2	
ZT 8952 IDE Subsystem	Fixed IDE	500 MB	2.5-inch Fixed	2	
ZT 8953 IDE Subsystem	Fixed IDE	500 MB	3.5-inch Fixed	2	
ZT 8954 Low Profile Floppy Controller	Floppy	2 MB	3.5-inch Floppy	2	
ZT 8955 SCSI-2 Controller	Fast SCSI-2	N/A	Hard Drive, CD-ROM, Tape, Flopticals Others	7	
ZT 8956 Intelligent SCSI-2 Controller	Fast-Wide SCSI-2	N/A	Hard Drive, CD-ROM, Tape, Flopticals Others	7	

Feature included or available
 Capacities are constantly changing. Contact Ziatech for latest available.

Expanded/Extended Memory System

Byte-wide memory board expands memory of STD Bus systems with the Expanded Memory Specification (EMS 3.2)

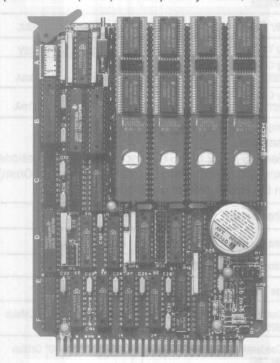
The ZT 8825 Expanded Memory System is a bytewide memory board that provides expanded memory capabilities to STD Bus systems. For DOS applications, the ZT 8825 can be used as PROM and/or battery-backed RAM disk, as main memory, as extended memory, or as expanded main memory. In any of these modes, it can accommodate up to 2 Mbytes of memory with eight JEDEC sockets.

Several ZT 8825 memory units can be used in a single system, allowing DOS computers to operate with several megabytes of solid state disk or expanded memory. The ZT 8825 utilizes the Expanded Memory Specification (EMS) developed by Lotus, Intel, and

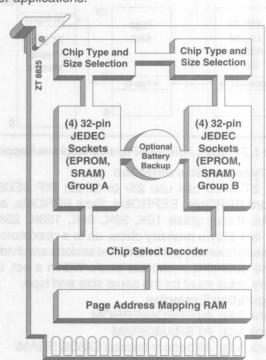
Microsoft. Originally developed to expand the 640 Kbyte conventional memory capacity of the PC DOS environment, this EMS technique has been adopted by Ziatech for its DOS computers.

The ZT 8825 can be used as a standard 24-bit addressable memory board (up to 2 Mbytes) for applications not using DOS.

The ZT 88CT25 is designed and tested for -40° to +85° Celsius operation in harsh environments. This product is designed for use in conjunction with Ziatech's other LT (low temperature) and CT (CMOS, TTL backplane-compatible) products for mobile and outdoor applications.



- Direct 20- and 24-bit addressing (STD-compatible)
- Two sets (four sockets each) of independently configured 32-pin JEDEC sockets
- Supports Expanded Memory Specification (EMS) for paged memory
- Supports various combinations of SRAM (32,128, 512 Kbyte chip size)
 and EPROM (16K to 1 Mbyte chip size)
- · Software support package included
- Supports flash EPROMs (+5V-only)



- Low power, extended temperature operation version available
- No wait states required at 5 or 8 MHz for fast memory device types
- Optional 1 amp-hour lithium battery backup for SRAMs (including RAM disks)
- 2 Mbyte maximum on-board storage, mappable in 16K pages
- Supports PROM, Flash EPROM, and RAM disk configurations in DOS

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40° to +85° C. (Users should make adjustments for temperature rise in enclosures.)



The ZT 8825 provides complete compatibility with the STD Bus specification. The ZT 8825 can operate at 5 and 8 MHz without wait states using properly chosen chips (see Wait States section).

Address Selection

The ZT 8825 is software-compatible with the Expanded Memory Specification (EMS), developed by Lotus, Intel, and Microsoft. EMS is a well-known memory mapping technique in the personal computer industry. It has been adopted by Ziatech for use with STD Bus computers in a DOS environment. Each 16 Kbyte block of ZT 8825 memory can be mapped into any of the 64 possible 16 Kbyte windows in the logical address space (24-bit addressing has 1024 possible windows).

This EMS implementation allows the ZT 8825 to fulfill various roles ranging from expanded main memory to PROM and RAM disk.

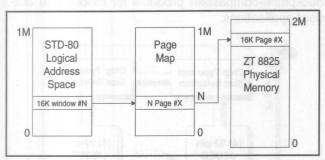


Figure 1. ZT 8825 Logical-to-Physical Address Mapping

Chip Type and Size Selection

The ZT 8825 can use 28- or 32-pin DIP JEDEC standard EPROMs, EEPROMs, flash EPROMs, and SRAMs. It can utilize 16K, 32K, 64K, 128K, 256K, 512K, or 1 Mbyte memory chips, up to a maximum of 2 Mbytes of memory per board. The sockets are divided into two sets of four sockets each. Within a set, the memory chips must be the same size and type.

Configuration Examples

Bank A/B: All EPROM/EPROM

Bank A/B: All SRAM/SRAM

 Bank A/B: All battery-backed CMOS SRAM/ battery-backed SRAM

Bank A/B: PROM/SRAM

Software

Ziatech provides an IBM PC format 3.5" disk with Expanded Memory Manager software (EMS-compatible) and RAM, PROM, and battery-backed RAM disk software drivers for DOS 3.x and newer systems. This software support is provided free of charge.

Battery Backup

To maximize the battery backup duration, very low power CMOS SRAMs must be used. Approved types are Toshiba TC55256 PL-12, NEC µPD44256-12L, and Sony CXK58255P-12L. Each of these has a 1µA data retention current which will have an estimated two-year life on a fully loaded ZT 8825. Higher current devices will reduce the life proportionately.

Either or both sets of four sockets may be battery-backed. An on-board DC voltage comparator isolates the RAMs when V_{CC} drops below 4.5V on power-fail. When V_{CC} reaches 3.0, the ZT 8825 enters data retention mode for battery backup of the SRAMs.

Wait States

The ZT 8825 may optionally generate one wait state on each access.

Write Protect

Hardware and software write protection is available.

Specifications Electrical

Power Req.*	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, V _{CC} =5.0V (ZT 8825)	-	500mA	670mA
Supply Current, V _{CC} =5.0V (ZT 88CT25)	50mA	100mA	220mA

^{*} Memory chips not included

Mechanical

 Meets STD 32 and STD mechanical specifications except for lead protrusion of 0.115 inches (2.90mm) on the circuit side of the board.

Environmental		
Operating Temperature (ZT 8825)	0° to 65° Celsius	
Operating Temperature (ZT 88CT25)	-40° to +85° Celsius	
Storage Temperature	-55° to +105° Celsius*	
Non-Condensing Relative Humidity (ZT 8825)	less than 95% at 40° Celsius	
Non-Condensing Relative Humidity (ZT 88CT25)	15% to 90% at 40° Celsius	

^{*} Note: Battery cannot be stored in temperatures above 110° C

STD 32 Compliance Level

Memory Slave: SA-8

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz).

Reliability

MTBF: 45 years

MTTR: five minutes (based on board replacement)

5

Ordering Information

ZT 8825 Expanded /Extended memory

system

ZT 88CT25 Expanded /Extended memory

system, extended temperature

ZT M8825 Expanded /Extended memory

system manual

The ZT 8825 (or ZT 88CT25) has two banks of separately configured memory. Orders must include a configuration for each bank (specify zero memory, if required), with a maximum of 2 Mbytes per board.

Ordering example: A ZT 8825 Expanded/Extended Memory System with 1 Mbyte of SRAM in bank A, 128 Kbytes of flash, and 1 amp-hour lithium battery would be ordered as: ZT 8825- (or ZT 88CT25) AM3BM4B.

Must choose one memory option for memory banks A and B (Contact Ziatech for other configurations):

Memory Options

M0 No memory

M1 128 Kbyte static RAM chip, 100ns

M2 Four 128 Kbyte static RAM chips, 100ns

M3 Two 512 Kbyte static RAM chips, 120ns,

1 Mbyte total

M4 32 Kbytes flash Memory (5V), 200ns

M5 128 Kbytes flash Memory (5V), 200ns

M6 2 Mbytes static RAM, 120ns (Bank A only, Bank B unpopulated)

Miscellaneous Option

B 1 amp-hour lithium battery, extended temperature

Choose accessories as needed:

Accessories

ZT 96009 Memory kit with 64 Kbyte

EPROM, 200ns

ZT 96013 Memory kit with 128 Kbyte

EPROM, 200ns

ZT 96033 Memory kit with 256 Kbyte

EPROM, 200ns

ZT 97047 Software package with EMS

driver for DOS

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix. Batteries are not covered by Ziatech's warranty.



dering in formation

1 8825 Expanded /Extended memory
system, extended temperature
system, extended temperature
f M8825 Expanded /Extended memory
system manual

10 2T 8825 (or 2T 880725) has two banks are left configured memory. Orders must include
liguration for each bank (specify zero memory, liguration for each bank (specify zero memory, liguration for each bank (specify zero memory, liguration and each bank (specify zero memory, light), with a maximum of 2 Mbytes per board.

Indering era inplet: IA 21 932b Expandeduxienada lemory System with 1 Moyte of SRAM in bank A, 128 ayles of liash, and 1 amp-hour lithium battery would be ordered as 21 8626- (or ZT 880125) AMSBMAB. Itset classes one memory option for memory banks land 8 (Cor Inct Zlatech for other configurations). Authory Options

Nom arrory
128 kbyte static RAM chip, 100ns
A2 Four 123 Kbyte static RAM chips, 100ns
A3 Two 5 to Kbyte static RAM chips, 120ns,
A 32 Kbytes total
A5 22 Kbytes theb Memory (5V), 200ns
A5 128 Kbytes flesh Memory (5V), 200ns
A6 2 Millytes static RAM, 120ns (Bank A chips
Beans 3 unpopulated)

extended temperature
ose apacs sortes as needed:
ZT 9c009 Memory fit with 64 Kbyte
EPROM, 200ns
ZT 9c013 Mamory kit with 128 Kbyte
EPROM, 200ns
ZT 9c023 Mamory kit with 256 Kbyte
EPROM, 200ns
ZT 9c047 Software package with EMS
driver for DOS

shases. Contest Zietech for additional information.

Warranty—Five years with an optional five-year extension. See the rull warranty statement in the Technical Cata Book appendix. Batteries are not covered by Zatach's warranty.





32-Bit Memory System

32-bit memory board provides SRAM, flash, shared RAM to STD 32 computers

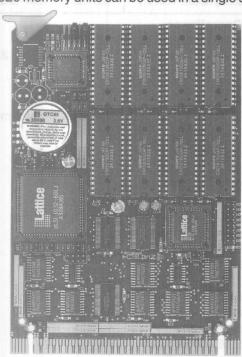
The ZT 8920 is a 32-bit Extended Architecture (EA) and 16-/8-bit Standard Architecture (SA) memory board that provides extended memory capabilities to STD 32® computers. The ZT 8920 is designed to operate with high-end processors that can perform 16-bit SA and 32-bit EA memory transfers across the STD 32 backplane. Ziatech processors with this capability include the ZT 8901 Single Board V53 Computer, ZT 8902 Single Board 486 Computer, and ZT 8911 Scalable Processor Board. The ZT 8920 can be used as extended memory, shared RAM for STD 32 STAR SYSTEMs™, battery-backed RAM, or as a flash disk. In any of these modes, it can accommodate up to 4 Mbytes of memory with eight JEDEC sockets. Several ZT 8920 memory units can be used in a single system,

allowing DOS computers to operate with several megabytes of solid state disk or extended memory.

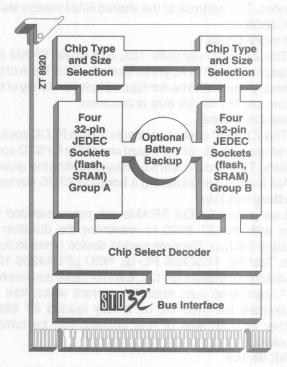
The ZT 8920 doubles backplane performance in 16-bit SA mode, and increases it by 16 times in 32-bit EA single mode over traditional STD-80 specifications.

Other features include a boot-off-board socket for booting single board computers which have not been programmed.

The ZT 89CT20 model is designed and tested for -40° to +85° Celsius operation in harsh environments. This product is designed for use in conjunction with Ziatech's other LT (low temperature) and CT (CMOS, TTL backplane-compatible) products for mobile and outdoor applications.



- · 24-bit addressing only
- 32-bit EA transfers
- · 8- or 16-bit SA transfers
- · Auto EA/SA detect, jumper selectable
- Two sets (four sockets each) of independently configured 32-pin JEDEC sockets
- 0 to128 Kbyte shared RAM, jumper selectable using bank B



- 1, 2, or 4 Mbyte of RAM, flash (5V-only)
- Boot-off-board EA or SA modes, jumper selectable
- Optional 1 amp-hour lithium battery backup for SRAMs (including RAM disks)
- 5V-only board
- Board is mapped on 1, 2, or 4 Mbyte boundaries

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40 $^{\circ}$ to +85 $^{\circ}$ C. (Users should make adjustments for temperature rise in enclosures.)



The ZT 8920 is compatible with STD 32 Bus specifications. The board extensions prevent it from fitting into the STD-80 backplane connector.

Address Selection

The ZT 8920 supports extended memory and can be mapped at 1, 2, or 4 Mbyte boundaries. In SA mode, the board can be mapped anywhere in the 16 Mbyte address range, and in EA mode anywhere in the 4 Gigabyte address range. The address is set by 12 jumpers which control A20 to A31.

Memory Banks

There are two memory banks on the ZT 8920. These banks can be independently configured for different device types but are mapped contiguously to each other. For example, if the ZT 8920 is mapped at 1 Mbyte, RAM bank A is mapped at 100000h to 17FFFFh and RAM bank B is mapped at 180000h to 1FFFFFh. Shared RAM

The ZT 8920 supports 0 to 128 Kbytes of shared RAM for STD 32 STAR SYSTEMs. The RAM size is configured by three jumpers on the ZT 8920. The available options are 0, 16, 32, 48, 64, 96, and 128 Kbytes. The address of the shared RAM always starts at C8000h.

Memory Types

The ZT 8920 supports 128, 512 Kbyte SRAM devices, or 128 or 512 Kbyte 5V flash devices. Each of the memory banks can be configured independently of the other, but the device size is common.

Boot-Off-Board

The ZT 8920 contains a single 32-pin PLCC socket, which provides boot-off-board capability for STD computers. This feature is enabled by disabling the shared RAM feature and installing a bootable BIOS device.

Battery Backup

Low-power CMOS SRAMs are recommended for use with the ZT 8920 to maximize the duration of battery backup. Recommended device types include the Toshiba TC55256 PL-12, NEC µPD44256-12L, and Sony CXK58255P-12L. Each of these devices has a 1 microamp data retention current which has an estimated two-year life on a fully loaded ZT 8920. Either or both sets of four sockets can be battery backed.

Wait States

The ZT 8920 generates wait states for EA cycles only, when enabled on the ZT 8920. Wait states on each memory bank are controlled independently.

Low Power/Extended Temperature

The ZT 89CT20 version is designed and tested for -40° to +85° Celsius operation in harsh environments. This product is designed for use in conjunction with Ziatech's other LT (low temperature) and CT (CMOS, TTL backplane-compatible) products for mobile and outdoor applications.

Specifications Electrical

Power Req. *	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, V _{CC} =5.0V	orq-bra	200mA	250mA

^{*} Not including memory chips

Mechanical

- Size- and backplane-compatible with STD 32 mechanical specifications (can only be used in an STD 32 system)
- Measures: 4.5"W by 6.5"L by 0.46"H (11.4cm by 16.5cm by 11.5mm)
- Weight: 4.6oz. (130g)
- Occupies one 0.625" (1.6026cm) STD slot

Environmental		
Operating Temperature (ZT 8920)	0° to 65° Celsius	
Operating Temperature (ZT 89CT20)	-40° to +85° Celsius	
Storage Temperature	-55° to +105° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

STD 32 Compliance

· Memory Slave: SA-8, SA-16, EA-32

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz)

Reliability

- MTBF: 40 years
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8920 32-Bit Memory System ZT 89CT20 32-Bit Memory System,

extended temperature

ZT M8920 32-Bit Memory System manual

Must choose one memory option:

Memory choices

M0 No memory

M1 128 Kbytes RAM, 70ns

M2 512 Kbytes static RAM, 120ns

M3 2 Mbytes static RAM, 120ns

M4 512 Kbytes 5V flash memory, 150ns

M5 2 Mbyte 5V flash, 150ns

Optional accessories:

B 1 amp-hour lithium battery, extended temperature

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information. *Warranty* – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix. Batteries are not covered by Ziatech's warranty.





PCMCIA 2.0 Interface for STD Bus Computers

PCMCIA interface provides fixed media and I/O PC Card™ support for STD 32® and STD Bus computers

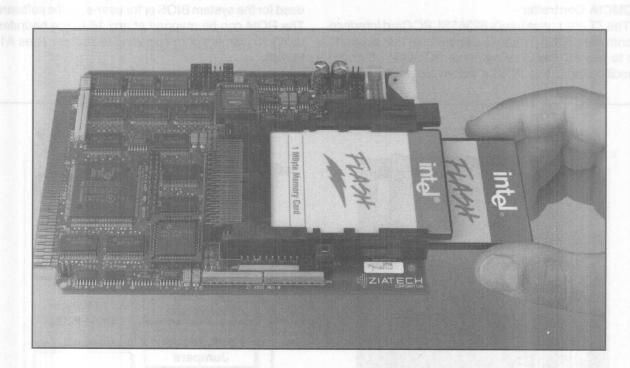
The ZT 8921 provides STD 32 and STD Bus computer systems with fixed media storage and I/O interface options via plug-in, credit card-sized modules (PC Cards). The interface is fully compatible with the Personal Computer Memory Card International Association (PCMCIA) 2.0 standard. Features include dual PC Card support, hardware and software resets, a 16 Kbyte PROM socket for BIOS extensions or other code, and support for multiple ZT 8921 interfaces in a single STD system.

In harsh environments, less reliable rotating media can be replaced with a ZT 8921 interface equipped

with PC Card-based memory. This solid state memory is available in flash, SRAM, OTP, EPROM, EEPROM, and masked ROM formats.

The ZT 8921 also supports PC Cards containing I/O functions that adhere to the PCMCIA 2.0 standard. Peripherals such as modems, Local Area Network interfaces, and hard drives can be added to a system by plugging the desired I/O PC Card into the ZT 8921.

The ZT 89LT21 version combines low power and low temperature operation (-40 $^{\circ}$ to +70 $^{\circ}$ C).



- PCMCIA 1.0, 2.0, and JEIDA 4.0 compatible
- Supports two memory or two I/O PC Cards
- Supports LIM/EMS, XIP, or PCMCIA 2.0 Metaformats
- Supports flash, SRAM, OTP, masked ROM, and EEPROM memory cards
- Support for PC Card-based I/O (modems, LAN interfaces, hard drives, etc.)
- STD 32- and STD-compatible
- 16-bit I/O port addressing
- · 20- or 24-bit memory addressing
- On-board DC to DC converter for Flash Card programming
- ZT 89LT21 is available for low power/ low temperature operation

Note: LT (low temperature) denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40 $^{\circ}$ to +70 $^{\circ}$ C. (Users should make adjustments for temperature rise in enclosures.)



PCMCIA Overview

The Personal Computer Memory Card International Association (PCMCIA) developed a standard architecture for the credit card-sized expansion modules known as PC Cards. These cards plug into computers via a 68-pin external PC Card "slot."

Originally limited to flash, SRAM, ROM, OTP, and EEPROM memory card designs, the PCMCIA 2.0 standard now includes support for PC Card-based I/O such as modem and LAN interfaces. Now memory and I/O devices can be added to an STD 32 system simply by plugging the appropriate PC Card into one of the slots on the ZT 8921 interface.

PC Card technology, with its compact, low power characteristics, is well suited to the harsh environments in which STD systems frequently operate. Natural to their design, PC Card-based memory and I/O modules are resistant to the shock, vibration, and temperature extremes that hamper standard peripherals in such environments.

PCMCIA Controller

The ZT 8921 uses Intel's 82365SL PC Card Interface Controller (PCIC), a high-level controller that supports up to two PC Cards using either PCMCIA 1.0 or 2.0 specifications. The PCIC's automatic power control,

combined with the hardware design of the ZT 8921, allow individual PC Cards to be added or removed during power-up conditions. A PC Card resident in one ZT 8921 slot is unaffected by the addition or removal of a card in the other slot.

The PCIC address is set by 13 jumpers corresponding to address lines A3 to A15, allowing for an 8-byte resolution in the I/O addressing.

Memory Addressing

PCIC software controls five memory windows that support the Lotus-Intel-Microsoft/EMS, XIP interface. The PC Card Metaformat is also supported. PC Cards configured with up to 64 Mbytes of memory can be used in the ZT 8921.

I/O Addressing

Two I/O windows, also controlled by software, provide I/O addressing for I/O peripherals that conform to the PCMCIA 2.0 specification. The I/O address range for these devices is zero to 64 Kbytes.

PCIC BIOS ROM

The PCIC BIOS ROM, a 16 Kbyte EPROM, can be used for the system BIOS or for user-specific software. The ROM can be mapped at any 16 Kbyte boundary using 10 jumpers corresponding to address lines A14 to A23.

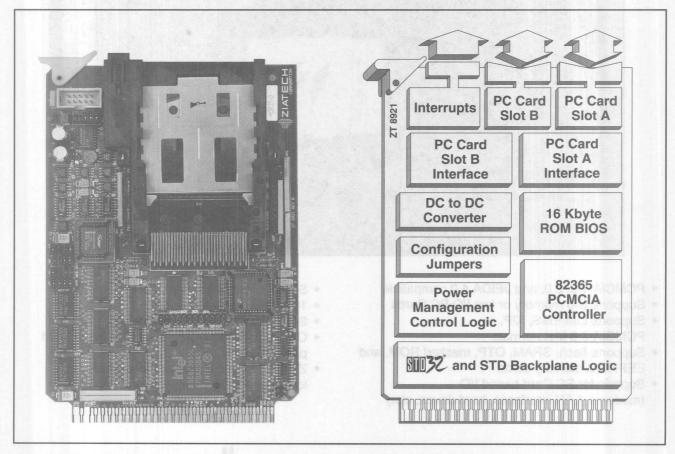


Figure 1. The ZT 8921 PCMCIA 2.0 Interface for STD Bus Computers offers easy expansion for STD Bus systems.

STD Bus Interface

The ZT 8921 performs 8- and 16-bit data transfers over STD 32 backplanes and 8-bit data transfers over STD-80 Series backplanes. The ZT 8921 decodes all 16 I/O address bits and either 20- or 24-bit memory address bits.

Software

The ZT 8921 comes equipped with Microsoft's Flash File System Version 2.0 (FF2) device drivers, which are supported by Ziatech's industrial BIOS. FF2 supports memory PC Cards with individual capacities of up to 64 Mbytes.

PC Card Support

The ZT 8921 supports most PC Cards that adhere to the PCMCIA 2.0 standard. **See Table 1** on the back page for a list of the current card types supported. Contact Ziatech for information about support for other types of PC Cards.

Low Power/Extended Temperature

The ZT 89LT21 is designed and tested for -40° to +70° Celsius operation in harsh environments. These products are designed for use in conjunction with Ziatech's other LT (low temperature) and CT (CMOS, TTL-compatible) products for mobile and outdoor applications.

Specifications

Electrical

- PCMCIA 1.0 or 2.0 and JEIDA compatible
- Backplane-compatible with STD 32 and STD-80 specifications



PC Card modules include I/O (modems, etc.) as well as memory cards.



This Type I PC Card (pictured at actual size) measures 2.13" (5.41cm) by 3.37" (8.56cm) by 0.13" (0.33cm) and provides 20 Mbytes of removable storage.

Power Req. *	Min.	Тур.	Max.
Supply Voltage, V _{CC}	4.75V	5.00V	5.25V
Supply Voltage, V _{CC} = 5.0V	100mA	180mA	220mA

^{*} Does not include PC Card

Mechanical

- Size- and backplane-compatible with the STD 32 and STD-80 mechanical specifications
- Measures 4.5" (11.4cm) by 6.5" (16.5cm)
- Height measured from component surface: 0.55" (1.40cm)
- Weight: 5.6 oz. (159g)
- Occupies two 0.625" (1.581cm) STD slots
- Connectors

P/E: 114-pin STD 32 Bus

P1/P2: Dual 68-pin PCMCIA 2.0 interface

JEIDA 4.0 standard

J1: 10-pin connector for external

interrupts

J2: 2-pin external speaker connector

Environmental *		
Operating Temperature (ZT 8921)	0° to 65° Celsius	
Operating Temperature (ZT 89LT21)	-40° to +70° Celsius	
Storage Temperature	-55° to +105° Celsius	
Non-Condensing Relative Humidity	10% to 95% at 40° Celsius	

^{*} Check PC Card specifications for deviations

Reliability

• MTBF: 27 years

MTTR: five minutes (based on board replacement)

STD 32 Compliance Level

• I/O Slave:

SA8-I, ICA, IXP, IXL SA16-I, ICA, IXP, IXL

· Memory Slave: SA8-I, ICA, IXP, IXL

SA16-I, ICA, IXP, IXL

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz).

Ordering Information

ZT 8921-M0

Dual PCMCIA 2.0 Interface for STD Bus Computers and Microsoft

Flash File Software

ZT 8921-M1

Same as ZT 8921-M0 above with an extended PCMCIA card connector for industrial computer enclosures (for ZT 250 and ZT 300, also order ZT 2521)

ZT M8921

PCMCIA 2.0 Interface manual

ZT 2521

Face plate for industrial computer

enclosures (e.g. ZT 250

and ZT 300)

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty - Five years with an optional five-year extension. See the full warranty statement in the Technical Data Book appendix.

For additional information, contact: PCMCIA at 1030G East Duane Avenue, Sunnyvale, CA, 94086. Telephone (408) 720-0107; FAX (408) 720-9416; BBS (408) 720-9388

PC Card™ is a trademark of the Personal Computer Memory Card International Association. Microsoft® is a registered trademark of Microsoft Corporation. STD 32 is a registered trademark of Ziatech Corporation. Other product names may be trademarks of their respective companies.

ZT 8921 Compatibility with Various PC Cards

PC Card Type	Thickness	Description	ZT 8921 Compatibility
Type I	3.3mm (0.13")	Standard memory card	Slots 1 and 2
Type II	5.5mm (0.22")	Intel iNC modem	Slots 1 and 2
Type III	10.5mm (0.41")	Hard drives (e.g. 32 Mbytes)	Contact Ziatech
Type IV	13.5mm (0.53")	Hard drives (ie.g. 64 Mbytes)	Contact Ziatech
Type I Extended	Unannounced	Unannounced	Contact Ziatech
Type II Extended	Unannounced	Unannounced	Contact Ziatech

Table 1. Several types of PC Cards are available that work with the ZT 8921.

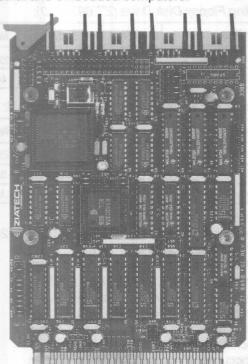




Floppy Disk Drive/DMA Controller

Modular microfloppy disk drive provides compact mass storage and DMA support for STD 32® and STD Bus industrial computer systems

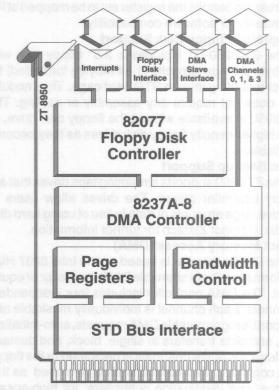
The ZT 8950 provides mass storage support for STD 32 and STD Bus systems. It provides PC-compatibile floppy support for CPUs that lack on-board PC DMA controllers, such as Ziatech's ZT 8801 Single Board V40 Computer and ZT 8901 Single Board V53 Computer. For the ZT 8902 Single Board 486 Computer and ZT 8911 Scalable Processor Board (Rev. A), the ZT 8954 Low Profile Floppy Disk Controller is used. The ZT 8950 Floppy Disk Drive/DMA Controller board is available separately or integrated with a floppy disk drive into a single unit. Its modular design provides easy installation, removability, and maintenance for industrial and embedded computers.



- STD 32- and STD-compatible
- Supports 3.5" and 5.25" disk drive formats
- Utilizes Intel 82077 Floppy Disk Controller
- IBM PC/AT-compatible in software and hardware design
- Interrupt capability
- On-board Direct Memory Access (DMA) controller (82C37-8)
- Off-board DMA capability

The IBM PC/AT®-compatible controller supports floppy disk drives with 1 Mbyte (720 Kbyte*) and 2 Mbyte (1.44 Mbyte*) storage capacity (*formatted capacities). The ZT 8950 also includes a Direct Memory Access (DMA) controller to support floppy disk data transfers as well as high-speed memory-to-memory, memory-to-I/O, and I/O-to-memory transfers across the STD Bus.

The ZT 8950 operates with 8-bit data transfers in an STD system and supports dynamic bus sizing for both 8-bit and 16-bit data transfers over the STD 32 backplane.



- Memory-to-memory DMA transfer capability
- Supports block mode DMA transfers
- DMA controller provides 24-bit addressing for memory transfer
- Disk controller supports up to two disk drives
- Programmable bandwidth registers
- Burned in at 55° C and tested to guarantee reliability



STD Bus Interface

The ZT 8950 is compatible with the STD 32 Bus Specification and the STD-80 Series specification. This compatibility enables the ZT 8950 to provide floppy disk and DMA support between 8-bit devices designed to operate in an STD backplane and between 8-bit and 16-bit devices designed to operate in an STD 32 backplane. The I/O devices local to the ZT 8950 are mapped into a 16-bit address space and the ZT 8950 provides a 24-bit memory address during DMA operations.

Floppy Disk Interface

The floppy disk interface is based on the Intel 82077 Floppy Disk Controller or equivalent. Features of the floppy disk interface include support for both 3.5" and 5.25" disk drives with unformatted storage capacities up to 2 Mbytes. The NEC 765 and PS/2 register sets are supported for compatibility with IBM PC/AT and PS/2 personal computers. Jumper-selectable I/O addressing permits the register set to be mapped at PC addresses for software compatibility.

Integrated Floppy Disk Support

The ZT 8950-D1 includes a 3.5" floppy disk with 2 Mbyte storage capacity (1.44 Mbytes formatted) for direct mounting into an STD card cage. This modular unit does not require any assembly or cabling. The ZT 8950 is available without the floppy disk drive, or with higher density floppy disk drives as they become available.

Tape Backup Support

The ZT 8950 supports streaming tape drives that are floppy controller driven. The drives allow users to archive large amounts of data in lieu of using hard disk media. Contact Ziatech for further information.

Direct Memory Access (DMA)

The DMA controller is based on the Intel 8237 High Performance Programmable DMA Controller or equivalent. The DMA controller includes four independent channels. Each channel is individually maskable and supports programmable DMA requests, auto-initialization, and data transfers in single, block, and demand modes. One of the channels is dedicated to the floppy disk controller. Two other channels, are used as the source and destination controllers, for high-speed, memory-to-memory transfers. These two channels and the one remaining channel are also available through frontplane connectors to allow DMA devices to request service.

Page Registers

There are four programmable registers, one for each DMA channel, that extend the number of memory address lines driven during a DMA transfer. The 8-bit registers add eight address lines to the 16 already provided by the DMA controller, for a total of 24.

Bandwidth Control

The bandwidth control manages the frequency of DMA operations and the maximum number of transfers for each DMA operation. This "throttling" mechanism protects the integrity of systems having critical interrupt latencies, DMA latencies, asynchronous data transfers, or dynamic RAM that must be refreshed by the STD CPU.

Software

The ZT 8950 is fully supported by MS-DOS using Ziatech's BIOS version 3.0 or later for Ziatech CPUs without on-board PC-type DMA controllers. For the ZT 8902 and ZT 8911 Rev. A, use the ZT 8954. (See the separate data sheet for the ZT 8954.)

Specifications Specification Specificat

Specifications that include rotating media are based on the Teac FD-235 HF 1.44 Mbyte, 3.5" drive. Other compatible drives may be used. (The specifications given vary for other drives)

Electrical

Excluding Floppy Disk Drive (ZT 8950-D0):

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.0 V	5.25V
Supply Current, Vcc = 5.0V	-	0.7A	1.4A

Integrated TTL Floppy Disk Drive (ZT 8950-D1):

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.0 V	5.25V
Supply Current, Vcc = 5.0V	0.7A	1.1A	2.0A
Start-up peak			2.1A

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 specifications
- PC/AT-compatible floppy disk interface
- Measures 4.5" (11.3cm) by 6.5" (16.5cm)
- Height measured from component surface: Excluding drive = 0.375" (9.5mm), occupies one 0.625" (15.9mm) slot Including drive = 1.600"(40.6mm), occupies three 0.625" (15.9mm) slots

· Weight:

Excluding drive = 7.0 oz (198.4g) Including drive = 22.0 oz (623.7g)

Connectors

PE: 114-pin card edge connector on 0.0625" (15.9mm) centers (backplane interface)

J1: 10-pin DMA request input (channel 0 or 3)

J2: 10-pin DMA request input (channel 1)

J3: 10-pin Floppy DMA request output J4: 10-pin interrupt input/output

J5A: 34-pin PC/AT floppy disk interface

Mechanical

Connectors

J5B:

34-pin PC/AT floppy disk interface

(reverse orientation)

J6:

4-pin floppy disk power location

J7:

4-pin floppy disk power location

Environmental

Excluding drive:

Environmental	
Operating Temperature	0° to 65° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

Including drive (typical):

Environmental	
Operating Temperature	5° to 45° Celsius
Storage Temperature	-20° to +60° Celsius
Non-Condensing Relative Humidity	20% to 80% at 40° Celsius

Shock: 6G (10ms)

• Vibration: 0.5G (55Hz) or 0.25G (55 to 150Hz)

STD 32 Compliance

• Temporary Master: SA16, SA8 - SDMA, MB

• I/O Slave:

SA8 - SDMA8, I, IXL, IXP

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz).

Reliability

· MTBF: three years

MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8950

Floppy Disk Drive/DMA Controller

ZT M8950

Floppy Disk Drive/DMA Controller

manual

Must choose one drive option

Drive Options:

D0

No drive installed

D1

1.44 Mbyte 3.5" integrated drive

installed

Accessories

Cable (see Data Book cable section for details):

ZT 90077

20" (50.8cm) dual floppy disk cable

ZT 90172

20" (50.8cm) floppy power cable

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Drive manufacturer's two-year warranty. See the full warranty statement in the *Technical Data Book* appendix.







ZT 8952/8953

Integrated Drive Electronics (IDE) Subsystems

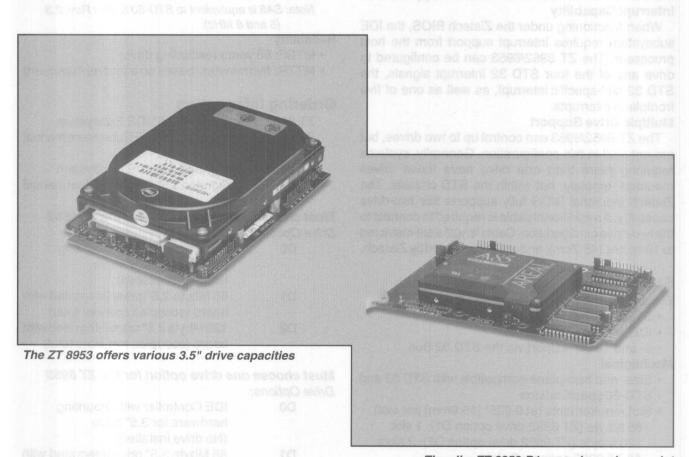
Multi-unit IDE disk drive controller supports 8- and 16-bit STD 32°/STD Bus systems

The ZT 8952 and ZT 8953 provide Integrated Drive Electronics (IDE) disk drive support to STD 32 and STD Bus industrial computers.

The ZT 8952 and ZT 8953 are fully integrated, IDE controller and disk drive units intended for STD 32 and STD Bus systems that lack built-in IDE support. The ZT 8952 features an integrated 2.5-inch disk drive, while the ZT 8953 features an integrated 3.5-inch hard

disk drive. Various drive capacities are supported on both the ZT 8952 and ZT 8953.

The IDE concept is used in many laptop computers because of its low cost and modularity. The demands of the laptop environment require IDE drives to have high resistance to shock and vibration. The reliability of this IDE technology also benefits STD 32 and STD computers that operate in harsh environments.



The slim ZT 8952-D1 occupies only one slot

- STD 32- and STD-compatible
- Supports 3.5" and 2.5" IDE drives
- On-board 8- and 16-bit byte lane control/FIFO capability
- Requires only 5 volts power for 2.5" drives
- · Controls up to two IDE drives

- · Optional IDE drive mounted on controller
- Fully supported by the Ziatech BIOS and STAR multiprocessing BIOS
- · Interrupt capability
- Single slot capability (ZT 8952-D1)



Integrated Drive Electronics (IDE) Controller

The ZT 8952 and the ZT 8953 both interface the IDE electronics to the STD Bus, supporting CPUs that do not directly support the IDE protocol. This CPU-independent approach allows modular sharing of data between systems for data acquisition as well as embedded applications.

Data Transfer

Although the IDE interface is a 16-bit interface, the ZT 8952/8953 operate with 8- and 16-bit CPU systems via the STD 32 and STD Buses. For 8-bit CPU systems, data is packed and unpacked dynamically by the bus interface logic. In 16-bit systems, the bus interface logic performs full 16-bit transfers. All disk transfers are performed with programmed I/O cycles. The IDE interface is not a Direct Memory Access (DMA) system, and therefore, the host processor need not support DMA. Interrupt Capability

When functioning under the Ziatech BIOS, the IDE subsystem requires interrupt support from the host processor. The ZT 8952/8953 can be configured to drive any of the four STD 32 interrupt signals, the STD 32 slot-specific interrupt, as well as one of five frontplane interrupts.

Multiple Drive Support

The ZT 8952/8953 can control up to two drives, but are not sold in this configuration. Generally, systems requiring more than one drive have those drives mounted remotely, not within the STD chassis. The Ziatech industrial BIOS fully supports this two-drive capability. An additional cable is required to connect to the two-drive configuration. Cable lengths are restricted to 18 inches (45.7cm), and are not provided by Ziatech.

Specifications

Electrical

- STD 32 and STD-80 compatible
- IDE interface-compatible
- 8- and 16-bit support via the STD 32 Bus

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 specifications
- Slot requirements (at 0.625" [15.9mm] per slot)
 85 Mbyte (ZT 8952 drive option D1): 1 slot
 120 Mbyte (ZT 8952 drive option D2): 2 slots
 All ZT 8953 options: 3 slots
- Vibration: 5 to 500Hz sine wave (p-p), 0.5G
- Shock: 1/2 sine wave of 11ms duration, 20G Vibration and shock specifications will vary with drive used.

Connectors

- One 40-pin 0.1" (2.5mm) IDE interface
- One 44-pin 2mm IDE interface position for 2.5" integration (ZT 8952 only)

Environmental	
Operating Temperature	5° to 55° Celsius
Storage Temperature	-40° to +60° Celsius
Non-Condensing Relative Humidity	8% to 80% at 40° Celsius
Operating Altitude	10,000 feet (3047.9m) or less

Parameters change with different drives installed. These environmental specifications refer to the 85 Mbyte 2.5" disk drive (ZT 8952-D1).

STD 32 Compliance

• I/O Slave: SA16, SA8 - I, IXL, IXP Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz).

Reliability

- MTBF: 86 years (excluding drive)
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8952 ZT M8952	Integrated 2.5" IDE Subsystem Integrated 2.5" IDE Subsystem manual
ZT 8953 ZT M8953	Integrated 3.5" IDE Subsystem Integrated 3.5" IDE Subsystem manual

Must choose one drive option for the ZT 8952 Drive Options:

D0	IDE Controller with mounting
	hardware for 2.5" drive
	(No drive installed)
D1	85 Mbyte 2.5" drive integrated with
	board (occupies one slot total)
D2	120 Mbyte 2.5" drive integrated with
	board (occupies two slots total)

Must choose one drive option for the ZT 8953Drive Options:

D0	IDE Controller with mounting
	hardware for 3.5" drive
	(No drive installed)
D1	85 Mbyte 3.5" drive integrated with
	board (occupies three slots total)
D2	170 Mbyte drive integrated with
	board (occupies three slots total)
D3	340 Mbyte drive integrated with
	board (occupies three slots total)
D4	530 Mbyte drive integrated with
	board (occupies three slots total)
antant Tin	took for other diels drive configurations

Contact Ziatech for other disk drive configurations.





Low Profile Floppy Disk Controller

Low profile, low-power, integrated floppy disk interface for STD 32® industrial computer systems

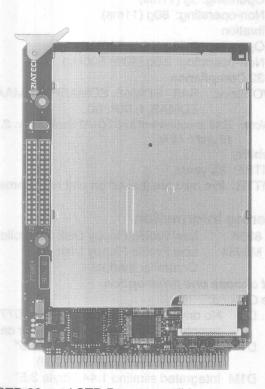
The ZT 8954 is an integrated floppy disk drive and controller for the STD 32 Bus. The entire assembly occupies a single slot through the use of highly integrated surface mount control logic and a low profile floppy disk drive. The ZT 8954 is intended for use with STD 32 CPU boards that have Direct Memory Access (DMA) capability (like the ZT 8902 Single Board 486 Computer and the ZT 8911 Scalable Processor Board).

The floppy disk drive does not use +12V, freeing the system of that requirement.

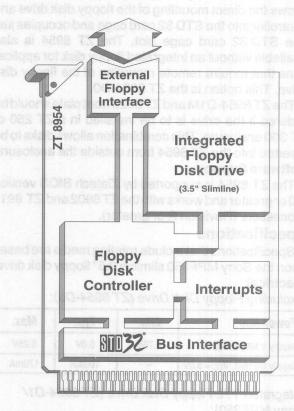
The IBM PC/AT®-compatible floppy disk controller used in the design of the ZT 8954 supports all floppy

disk formats, including 360 and 720 Kbyte and 1.2 formatted densities. Interface connectors are provided for 3.5" and 5.25" floppy drives. A remote mounting option allows the floppy disk drive to be located up to 21 inches from the STD 32 chassis.

The ZT 8954 is fully compatible with the STD 32 and STD Bus specifications. STD 32 is a superset of the original STD Bus that allows higher speed transfers as well as backplane DMA. The ZT 8954 takes advantage of the capabilities of the STD 32 Bus to provide maximum flexibility and performance.



- STD 32- and STD Bus-compatible
- Low profile one-slot integrated 3.5" option
- 3.5" and 5.25" floppy disk drive support
- High performance Intel 82078-1 floppy disk controller
- PC-compatible design supporting DOS/Windows and other operating systems



- · Direct Memory Access capability
- Integrated 16-byte FIFO
- · Support for up to two disk drives
- ZT 250/300 Industrial Enclosure mounting option
- Burned in at +55° Celsius and tested to guarantee reliability



STD 32 Bus Interface

The ZT 8954 is compatible with Revision 1.2 of the STD 32 Specification and with the original STD-80 Specification, which is a subset of STD 32. The ZT 8954 is designed to work without any frontplane connections in STD 32 systems. When used in STD Bus card cages a frontplane DMA cable is required. All accesses to the ZT 8954 are 8 bits wide for programming and for DMA. The peripherals on board the ZT 8954 are I/O mapped, with full 16-bit address decoding. There are no memory peripherals on board.

Floppy Disk Interface

The Floppy Disk Controller (FDC) used on the ZT 8954 is register-compatible with the original controller used in the IBM PC. The floppy disk interface supports both 3.5" and 5.25" disk drives in formatted capacities of 360 and 720 Kbytes and 1.2 and 1.44 Mbytes.

The ZT 8954-D1 includes a slimline 3.5" floppy disk drive with 1.44 Mbyte capacity support. This option allows the direct mounting of the floppy disk drive and controller into the STD 32 card cage and occupies just one STD 32 card cage slot. The ZT 8954 is also available without an integrated floppy disk for applications that require remote mounting of the floppy disk drive. This option is the ZT 8954-D0.

The ZT 8954-D1M and ZT 2523 front plate should be ordered if the drive is to be installed in a ZT 250 or ZT 300 enclosure. This combination allows disks to be inserted into the ZT 8954 from outside the enclosure. **Software Support**

The ZT 8954 is supported by Ziatech BIOS version 4.0 or greater and works with the ZT 8902 and ZT 8911 processors (Revision A or greater).

Specifications

Specifications that include rotating media are based upon the Sony MPF350 slimline 3.5" floppy disk drive. **Electrical**

Excluding Floppy Disk Drive (ZT 8954-D0):

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.0V	5.25V
Supply Current, Vcc = 5.0V		100mA	170mA

Integrated TTL Floppy Disk Drive (ZT 8954-D1/ Sony MPF350):

Power Req. (5V)	Min.	Тур.	Max.
Supply Voltage, V _{CC}	4.75V	5.0V	5.25V
Idle		105mA	WON IN
Start-up peak	-	Elisto Tak as	720mA
Read/Write	-	320mA	320mA
Motor Start	-	-	720mA
Motor Step	_	_	720mA

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 specifications
- STD 32 Slot Usage: 1 slot (0.5" maximum component height)
- Weight

ZT 8954-D0: 3 oz. (85g) ZT 8954-D1: 9 oz. (255.1g) ZT 8954-D1M: TBD

Connectors

J1: 10-pin latching frontplane DMA
J2,J3,J4,J6: Floppy disk drive interface
J5: Floppy disk drive power
connector

Environmental	without drive	with drive (typ.)
Operating Temperature	0° to 65° Celsius	5° to 45° Celsius
Storage Temperature	-40° to +85° Celsius	-20° to +60° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° C	20% to 80% at 40° C

· Shock

Operating: 5g (11ms) Non-operating: 80g (11ms)

Vibration

Operating: 0.56g (10 to 500Hz) Non-operating: 2.0g (10 to 500Hz)

STD 32 Compliance

 I/O Slave: SA8 - SDMA8, SDMABP, EDMAA, EDMAB, I, IXP, IXL

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz).

Reliability

MTBF: 25 years

MTTR: five minutes (based on unit replacement)

Ordering Information

ZT 8954 Low Profile Floppy Disk Controller ZT M8954 Low Profile Floppy Disk

Controller manual

Must choose one drive option

Drive Options:

D0 No drive installed. Includes ZT 90077 remote mounting cable and power cable.

D1 Integrated slimline 1.44 Mbyte 3.5" floppy disk drive (one slot total)

D1M Integrated slimline 1.44 Mbyte 3.5" floppy disk drive for ZT 250 and ZT 300 card rack systems

Accessories

Cable (see Data Book cable section for details):

ZT 90077 20" (50.8cm) dual floppy disk cable
for use with ZT 8954-D0 only

Warranty – Drive manufacturer's two-year warranty. See the full warranty statement in the *Technical Data Book* appendix.





SCSI-2 Controller

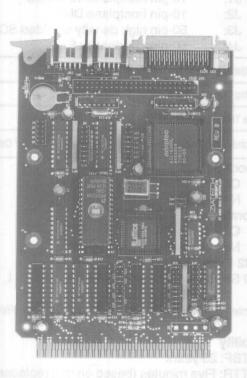
SCSI-2 interface card is Adaptec 1520A-compatible, supporting up to seven devices with 10 Mbytes per second transfer rates

The ZT 8955 brings SCSI-2 interface capabilities to the STD 32 Bus. It supports both 8- and 16-bit backplane transfers with off-board DMA or programmed I/O (PIO) transfers on the STD 32 bus. The ZT 8955 is software-compatible with the Adaptec 1520A and takes advantage of the many software packages written to support SCSI peripherals. The ZT 8955 is compatible with both SCSI-1 and SCSI-2 devices (including Fast-SCSI). The ZT 8955 also supports 32-bit double-word transfers which are buffered through a 128-byte FIFO for increased efficiency and higher transfer rates.

Up to seven SCSI devices are supported by the ZT 8955. DMA communication can be routed across the backplane or frontplane, or can use the slot-specific DMA channels provided by STD 32 systems.

The ZT 8955 features active terminations and singleended operation, allowing cable lengths of up to 19.7 feet (6 meters).

Sustained data transfer rates of up to 10 Mbytes per second are supported across the SCSI interface. The ZT 8955 meets all of the requirements outlined in the Small Computer Systems Interface (SCSI-2) standards.



DMA Low High Interrupts Density Densit

- STD 32- and STD-compatible
- On-board 8- and 16-bit data control/FIFO capability
- DMA slave operation
- · BIOS extension socket with software
- SCSI-2 operation supporting up to 10 Mbytes per second transfer rates (Fast-SCSI)
- 19.7 feet (6m) maximum cable length
- Support for simultaneous operation of seven separate SCSI devices

- 50-contact low-density connector and shielded high-density connector for external SCSI devices
- Active terminators on the SCSI interface for improved noise immunity
- Boot and multiple disk/tape drive software included
- Burned in at 55° C and tested to guarantee reliability



Functional Considerations STD 32 Bus Interface

The ZT 8955 is compatible with Revision 1.2 of the STD 32 Specification and with the original STD-80 Specification, which is a subset of STD 32. It supports both 8- and 16-bit backplane transfers with off-board DMA or programmed I/O transfers on the STD 32 bus. The ZT 8955 is designed to work without any frontplane connections in STD 32 systems. When using DMA transfers in an STD-80 card cage a frontplane DMA cable is required. The peripherals on board the ZT 8955 are I/O mapped with 16-bit address decoding. There is a memory peripheral (BIOS extension) on board.

SCSI Bus Interface

The ZT 8955 provides a fully compliant SCSI-2 interface and is software compatible with the Adaptec 1520A, taking advantage of the many software packages written to support the 1520A and SCSI peripherals. The ZT 8955 is compatible with both SCSI-1 and SCSI-2 devices (including Fast-SCSI). The ZT 8955 also supports 32-bit double-word transfers which are buffered through a 128-byte FIFO for increased efficiency and higher transfer rates.

The ZT 8955 supports a host of SCSI-compatible peripheral devices, including fixed disk drives, highcapacity floppy drives, tape drives, CD-ROM drives, and other removable media drives.

Multiple boards can share the backplane. However, most commercially available software checks only two different I/O locations, limiting commercial software support to only two ZT 8955 interfaces per system. These two ZT 8955 I/O addresses are 0340h-035Fh (standard SCSI control/read back registers) and 0140h-015Fh (optional SCSI control/read back registers). The ZT 8955 supports up to seven different hardware jumperable locations.

Software Support

Software support for the ZT 8955 is supplied in two different forms: as a BIOS extension and as a DOS installable device driver.

Both are licensed by Ziatech from Adaptec and are software-compatible with the drivers used on the Adaptec 1520A.

Booting from a SCSI device requires a BIOS extension PROM on the ZT 8955, but limits device support to only two fixed disks. However, the BIOS extension does not use any system RAM.

The ASPI2DOS Installable DOS Device Driver for the ZT 8955 supports two or more fixed disks or nondisk devices. This driver is required for non-disk devices such as tape drives. The ASPI2DOS Installable Driver also supports multitasking and greater configuration options such as port address, bus on/off time, and expansion through additional device driver modules.

The device driver is fully compatible with the Advanced SCSI Programming Interface (ASPI), an industry standard programming interface for SCSI controllers.

Specifications

Electrical

Power Req.	Min.	Тур.	Max.
Supply Voltage, V _{CC}	4.75V	5.0V	5.25V
Supply Current, Vcc=5.0V	ind elange	TBD	1.3A

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 specifications
- STD 32 Slot Usage: One slot (0.5" [12.2mm] maximum component height)
- Weight: 3oz. (85g)
- Connectors

OHITICOLO	
PE:	STD 32-compatible backplane
	interface
J1:	10-pin frontplane interrupts
J2:	10-pin frontplane DMA
J3:	50-pin high density shielded SCSI

50-pin low density SCSI

Environmental	
Operating Temperature	0° to 65° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

Shock

Operating: 5g (11ms) Non-operating: 80g (11ms)

Vibration

Operating: 0.56g (10-500Hz) Non-operating: 2.0g (10-500Hz)

STD 32 Compliance

• I/O Slave: SA16, SA8-D16, D8, A24, I, IXP, SDMA8, SDMA16

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8MHz).

Reliability

• MTBF: 25 years

MTTR: Five minutes (based on unit replacement)

Ordering Information

SCSI-2 Controller with ZT 8955

BIOS extension

ZT M8955 SCSI-2 Controller manual

Must choose drive option:

No drive installed

D₁ 340 Mbyte SCSI-2 hard disk drive

Accessories

ZT 97105

DOS Installable ASPI driver and Software manual

Cable (see data book cable section for details):

ZT 90137 2' (61cm) low density SCSI cable





Intelligent SCSI-2 Controller

High-performance, RISC-based 32-bit SCSI-2 controller

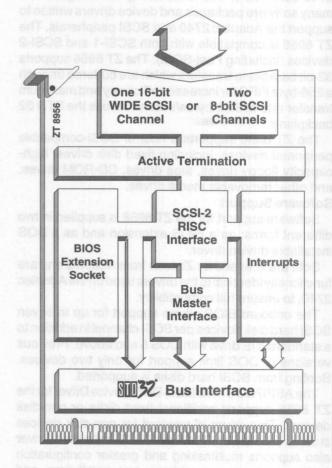
The ZT 8956 is a high-performance SCSI-2 (Small Computer Systems Interface) controller for the STD 32® Bus structure. The SCSI interface can be configured for one or two 8-bit interfaces or one 16-bit interface. The ZT 8956 is an Extended Architecture Bus Master on the STD 32 Bus, supporting 16- and 32-bit transfers. The design is software-compatible with the Adaptec AHA-2740 EISA SCSI interface and takes advantage of software and device drivers written for the 2740. The ZT 8956 is compatible with the SCSI-2 specification, including Fast SCSI.

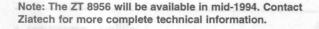
Up to seven SCSI devices are supported per SCSI interface on the ZT 8956, for a maximum of 14 devices. The slot-specific capability of STD 32 allows up to 14 ZT 8956 interfaces in the system, although most

system arbiters, such as the ZT 8911 Scalable Processor Board, limit support to six ZT 8956's. System boot services are supported by an onboard BIOS interface.

The ZT 8956 is configurable for either one 16-bit WIDE SCSI-2 Channel or two 8-bit SCSI-2 Channels. Sustained data transfer rates of up to 10 Mbytes per second are supported across both 8-bit SCSI-2 channels. Sustained data transfer rates of up to 20 Mbytes per second are supported across the 16-bit SCSI-2 channel. A 256-byte FIFO on the ZT 8956 allows the board to maintain a top data rate of up to 32 Mbytes per second across the STD 32 backplane. The ZT 8956 meets all of the requirements outlined in the Small Computer Systems Interface (SCSI) standard.

- RISC-based SCSI controller
- BIOS extension socket with software
- Two 8-bit or one 16-bit Fast SCSI-2 channel
- 8-bit SCSI-2 channels supports up to 10 Mbytes per second transfer rates (Fast-SCSI)
- 16-bit WIDE SCSI-2 operation supports up to 20 Mbytes per second transfer rates (Fast-SCSI)
- · 32 Mbytes per second STD 32 operation
- Supports simultaneous operation of fourteen separate SCSI devices
- Two 50-contact low-density connectors for 8-bit SCSI channels (A cable-compatible)
- Shielded high-density connector for 16-bit WIDE
 SCSI-2 channel (P cable-compatible)







The 218956 provides compatibility with the STD 32 Bus specification. The ZT 8956 requires an STD 32 system arbiter with MRFQ*/MAKx* capability.

The ZT 8956 features a RISC-based SCSI-2 controller, the Adaptec AIC-7770. The ZT 8956 provides either two 8-bit Fast SCSI-2 channels, or one 16-bit WIDE, Fast SCSI-2 channel, with respective peak transfer rates of 10 and 20 Mbytes per second.

The ZT 8956 supports both 16- and 32-bit backplane transfers on the STD 32 bus. The peripherals on board the ZT 8956 are I/O mapped with 16-bit address decoding. There is a memory peripheral (BIOS extension) on board, which provides system boot capability. The ZT 8956 is an Extended Architecture Bus Master. This means that the board can drive control cycles on the backplane independently of the host processor(s). SCSI Bus Interface

The ZT 8956 provides a fully compliant SCSI-2 interface and is software-compatible with the Adaptec 2740 EISA SCSI interface, taking advantage of the many software packages and device drivers written to support the Adaptec 2740 and SCSI peripherals. The ZT 8956 is compatible with both SCSI-1 and SCSI-2 devices (including Fast-SCSI). The ZT 8956 supports 32-bit backplane transfers which are buffered through a 256-byte FIFO for increased efficiency and maximum transfer rate of 32 Mbytes/second across the STD 32 backplane.

The ZT 8956 supports a host of SCSI-compatible peripheral devices, including fixed disk drives, high-capacity floppy drives, tape drives, CD-ROM drives, and other removable media drives.

Software Support

Software support for the ZT 8956 is supplied in two different forms: as a BIOS extension and as a DOS installable device driver.

Both are licensed by Ziatech from Adaptec and are functionally identical to the drivers used on the Adaptec 2740, to ensure full compatibility.

The onboard BIOS allows support for up to seven SCSI hard disk devices per SCSI channel in addition to a standard IDE drive with DOS 5 and above. Previous versions of DOS limit support for only two devices. Booting from SCSI hard disks is supported.

The ASPI7DOS Installable DOS Device Driver for the ZT 8956 supports additional fixed disks or non-disk devices. This driver is required for non-disk devices such as tape drives. The ASPI7DOS Installable Driver also supports multitasking and greater configuration options such as port address, bus on/off time, and expansion through additional device driver modules.

industry standard programming interface for SCSI controllers.

Specifications

Electrical The analysis of the second second

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.0V	5.25V
Supply Current, Vcc=5.0V	is: Interfa	TBD	2A

Mechanical management and a second a second and a second

- The ZT 8956 is size- and backplane-compatible with STD 32 specifications
- The ZT 8956 occupies one STD slot (0.625" or 1.6026cm spacing).
- Connectors

PE: STD 32-compatible backplane interface

- J1: 68-pin high-density shielded SCSI (P-cable)
- J2: 68-pin high density integrated drive connector
- J3: 50-pin low-density SCSI (A-cable)
- J4: 50-pin low-density SCSI (A-cable)
- J5: 4-pin power connector

Environmental	
Operating Temperature	0° to 65° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

STD 32 Compliance Level

- Temporary Master: EA32, EA16-{MX}, EBURST
- I/O Slave: EA8-{GAX}, I, IXP, IXL, NOWS
- Memory Slave: SA8

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz).

Reliability

MTBF: 20 years

MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8956-D0 Intelligent SCSI Controller and

software

ZT M8956 Intelligent SCSI Controller and

software manuals

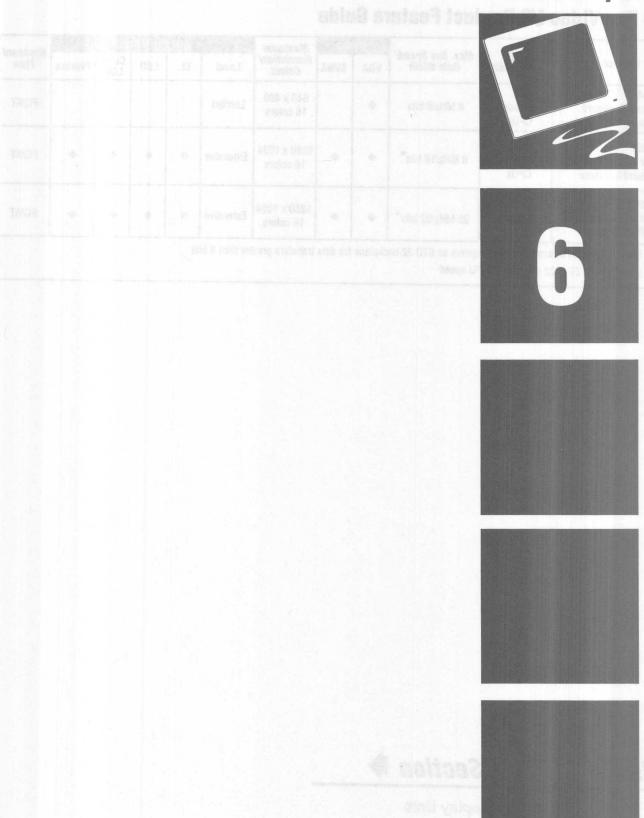
Accessories

Cables (see data book cable section for details): ZT 90137 2' (61cm) low-density SCSI cable

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.



STD Bus Video I/O



6

STD Bus Video I/O Product Feature Guide

	ODU	May Buo Consod/	Mo	odes	Maximum		Flat	Panel S	upport		
Product	CPU Compatibility	Max. Bus Speed/ Data Width	VGA	SVGA	Resolution/ Colors	Level	EL	LCD	Color	Plasma	Keyboard Type
ZT 8842 VGA and Keyboard Interface	All Ziatech CPUs	8 MHz/8 bits	*		640 x 480 16 colors	Limited					PC/AT
ZT 8982 Super VGA/FPD and Keyboard Interface	All Ziatech CPUs	8 MHz/16 bits	+	•	1280 x 1024 16 colors	Extensive	٠		*	•	PC/AT
zVID2 Local Bus Super VGA/FPD Adapter	ZT 8902	33 MHz/32 bits		•	1280 x 1024 16 colors	Extensive	•	+	*	•	PC/AT

- ◆ Feature included or available ◆ Requires an STD 32 backplane for data transfers greater than 8 bits
- ▲ Local bus on ZT 8902 operates at CPU speed

Also Inside This Section

- ZT 1502 Industrial Display Unit
- ELVGA and LCDVGA Rugged VGA Displays

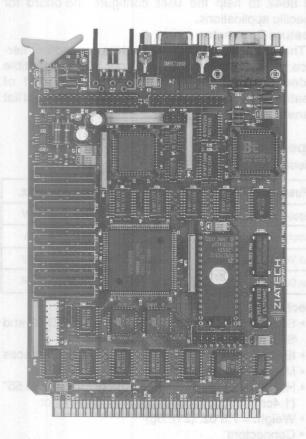


VGA and Keyboard Interface

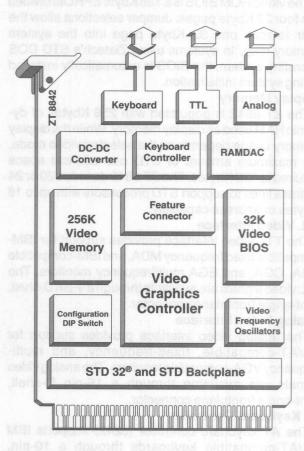
Video interface provides analog, and TTL display support in VGA and other resolutions, as well as keyboard control for STD 32® and STD Bus systems

The ZT 8842 drives analog and digital Cathode Ray Tube (CRT) displays, plus an IBM PC/AT-compatible keyboard via the on-board keyboard controller. For software developed for the IBM PC/AT, PS/2, and compatibles, the ZT 8842 provides VGA, EGA, CGA, and MDA video output.

The ZT 8842 is designed for industrial applications requiring a robust user interface with high-resolution graphics capabilities.



- STD 32- and STD-compatible
- · Register-level compatibility with VGA and BIOS-level compatibility with EGA, CGA, and MDA
- Support of IBM-compatible, fixed frequency digital MDA monitors
- Support of IBM-compatible, multifrequency digital monitors
- · Support of IBM VGA-, EGA-, MDA-, and MCGAcompatible fixed and multifrequency analog



- Palette of 262,144 available colors
- IBM PC/AT-compatible keyboard interface
- 256 Kbytes of display memory
- 32 Kbyte video BIOS
- · Support for four video boards in one STD card cage
- · Software utilities and drivers included
- Feature connector



Versatile Panel Display Controller

The ZT 8842 uses the Yamaha 6388 Versatile Panel Display Controller (VPDC), a high-level display controller with functions for driving high-resolution raster scanning CRT displays. The VPDC is completely compatible with IBM PS/2 video graphics array (VGA). When a VGA CRT is used, compatibility extends to the register level.

The ZT 8842 supports graphic resolutions up to 640 x 480 (16 colors) and 320 x 200 (256 colors) for CRTs. Text resolutions up to 132 columns with 25, 43, or 50 rows are also supported.

Video ROM BIOS

The video ROM BIOS is a 128 Kbyte EPROM divided into four 32 Kbyte pages. Jumper selections allow the user to map one 32 Kbyte page into the system memory map. In systems using Ziatech's STD DOS operating system, the BIOS is automatically installed during system initialization.

Display Memory

The ZT 8842 is populated with 256 Kbytes of dynamic RAM used as display memory. While the display memory usage depends on the selected video mode, the maximum amount of STD bus address space required is 128 Kbytes. The ZT 8842 decodes 20 or 24 address lines to support STD processors with up to 16 Mbytes of address capability.

TTL Video Interface

The TTL video interface provides support for IBMcompatible fixed frequency MDA, and IBM-compatible MDA, CGA, and EGA multifrequency monitors. The TTL video signals are available through a 9-pin D-shell, right-angle frontplane connector.

Analog Video Interface

The analog video interface provides support for PC/AT-compatible, fixed-frequency, and multifrequency VGA-compatible monitors. The analog video signals are available through a 15-pin D-shell, right-angle frontplane connector.

AT Keyboard Controller

The AT keyboard controller (8242) supports IBM PC/AT-compatible keyboards through a 10-pin, right-angle frontplane header. When used with STD DOS-based computers, all aspects of communication with the keyboard controller are initialized and managed by the operating system software. The keyboard controller can be disabled for systems already including a keyboard controller. An optional cable is required for direct connection to an IBM AT-compatible keyboard.

STD Bus Interface

The ZT 8842 performs 8-bit data transfers over STD 32 and STD backplanes. Memory addressing is

jumper-selectable as either 20-bit or 24-bit. The video memory is mapped from 0A0000 to 0BFFFF hex, and the video BIOS is mapped from 0C0000 to 0C7FFF hex. For I/O requirements, 16 address lines are decoded for all on-board registers. The video registers are mapped from 3B0 to 3DF hex. The keyboard controller is mapped at 60, 64, and 67 hex.

Software

The ZT 8842 VGA and Keyboard Interface is fully supported by Ziatech's STD DOS operating system in BIOS (version 3.0 or later), and by Ziatech's STAR BIOS (version 3.2 or later) for STD 32 STAR SYSTEMs. (For a list of supported operating modes, refer to Table 1 on the back page.)

A set of software utilities are also included with the ZT 8842 to help the user configure the board for specific applications.

Feature Connector

The ZT 8842 supports the feature connector interface found on most VGA and Super VGA-compatible video cards. This connector allows support of "feature"-style devices, including several classes of flat panel displays.

Specifications Electrical

Power Req. *	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V		0.6A	1.2A
Aux Voltage, V _{aux+}	11.4V	12.0V	12.6V
Aux Current, V _{aux+} = 12.0V		50mA	125mA

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 mechanical specifications
- IBM PC-compatible video and keyboard interfaces
- Measures 4.5" (11.4cm) by 6.5" (16.5cm)
- Height measured from component surface = 0.55" (1.4cm), occupies one 0.625" (1.58cm) slot
- Weight = 7.5 oz. (212.6g)

J6:

•	Connectors	
	E/P:	114-pin card edge connector on
		0.0625" (1.588mm) centers
	J1/J2:	10-pin, dual-row, right-angle header
		for AT keyboard
	J3:	34-pin, dual-row, vertical header for
		flat panel display
	J4:	9-pin, dual-row, D-shell, right-angle
		TTL video connector
	J5:	26-pin, dual-row, vertical header for

feature connector 15-pin, triple-row, D-shell, right-angle

analog video connector

nical Data Book appendix.

Environmental		All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity
Operating Temperature	0° to 65° Celsius	purchases. Contact Ziatech for additional information.
Storage Temperature	-40° to +85° Celsius	Warranty - Five years with an optional five-year
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	extension. See the full warranty statement in the Tech-

STD 32 Compliance Levels

 Memory slave: SA8 • I/O slave: SA8-I

Note: SA8 is equivalent to STD-80 Series Rev. 2.3

(5 and 8 MHz).

Reliability

• MTBF: 20 years

• MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8842 ZT M8842 VGA and Keyboard Interface

VGA and Keyboard Interface manual

Accessories

Cables (see Data Book cable section for details):

ZT 90076

32" (81.3cm) keyboard cable,

10-pin dual-row header to desktopstyle DIN keyboard connector

panel display

Mode	Type	Resolution	Colors	Displays	Address	Mode	Type	Resolution	Colors	Displays	Address
0,1	Text	40 x 25 8 x 8 Characters	16	CD, ED, VGA, MS	B8000	7	Text	80 x 25 9 x 14 Characters	-	MDA	B0000
0*, 1*	Text	40 x 25 8 x 14 Characters	16	ED, VGA, MS	B8000	D	Graphics	320 x 200	16	CD, ED, VGA, MS	A0000
0+,1+	Text	40 x 25 8 x 16 Characters	16	VGA, MS	B8000	Е	Graphics	640 x 200	16	CD, ED, VGA, MS	A0000
2,3	Text	80 x 25 8 x 8 Characters	16	CD, ED, VGA, MS	B8000	F	Graphics	80 x 25	2	MDA	A0000
2*,3*	Text	40 x 25 8 x 14 Characters	16	ED, VGA, MS	B8000	10	Graphics	640 x 350	16	ED, VGA, MS	A0000
2+,3+	Text	40 x 25 8 x 16 Characters	16	VGA, MS	B8000	11	Graphics	640 x 480	2	VGA, MS	A0000
4,5	Graphics	320 x 200	4	CD, ED, VGA, MS	B8000	12	Graphics	640 x 480	16	VGA, MS	A0000
6	Graphics	640 x 200	2	CD, ED, VGA, MS	B8000	13	Graphics	320 x 200	256	VGA, MS	A0000

Table 1. Software operating modes for the ZT 8842



All products are shipped FOB San Luis Claspo, CA
USA OEM discounts are available for quantity
purchases. Contact Zietech for additional programments.

Warranty — Five years with an optional five year extension. See the full warranty statement in the Tachnical Data Book appendix.

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- 1-8A8 sevela ON •
- Note: SA8 is equivalent to STD-80 Series Rev. 2.3

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Ordering Information
ZT 8842 VGA and Keyboard Interface
TT 8842 VGA and Keyboard Interface

	40 × 25 5 ± 18 (Supporters					
				005 x 040		

Pable 1. Software operating modes for the 27 8842





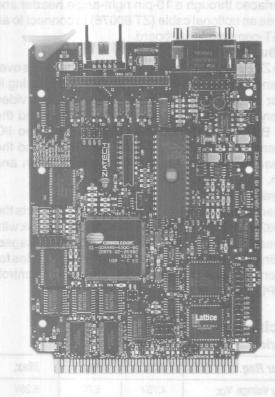
Super VGA/FPD and Keyboard Interface

Video interface provides keyboard control plus monitor and flat panel support for STD 32® and STD bus systems

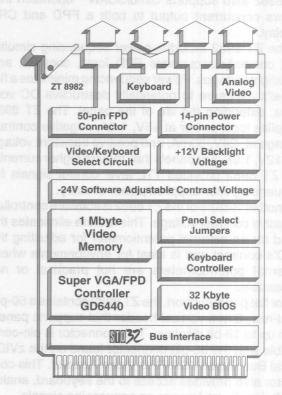
The ZT 8982 Super VGA/FPD and Keyboard Interface is an 8- or 16-bit STD 32 video card that supports both analog CRTs and Flat Panel Displays (FPDs). The ZT 8982 supports most monochrome and color FPDs on the market, including 8- and 16-bit single- and dual-scan color super twisted nematic (STN) panels and 9-, 12-, and 18-bit thin film transistor (TFT) color panels. The ZT 8982 contains 1 Mbyte of video memory and supports CRT resolutions up to 1024 x 768 x 256

colors non-interlaced and 1280 x 1024 x 16 colors interlaced.

The ZT 8982 also features video select circuitry, which allows multiple boards to share a common keyboard and monitor in Ziatech's STD 32 STAR SYSTEM™. Flat panel power-on sequencing circuitry is also included on the ZT 8982 to minimize a flat panel's exposure to harmful DC voltages.



- STD 32®- and STD-compatible
- Hardware-compatible with IBM Super VGA standard
- 1 Mbyte high-speed video memory
- Built-in Microsoft® Windows™ performance enhancements
- Built-in video select circuitry for up to eight video boards in same backplane
- 1024 x 768 x 256 colors non-interlaced



- 1280 x 1024 x 16 colors interlaced
- Supports 8- and 16-bit dual- and single-scan color STN panels
- Supports 9-, 12-,18-bit color TFT panels
- Simultaneous display on CRT and LCD panels (SimulSCAN™) with resolutions up to 1024 x 768 x 256 colors
- Power sequencing circuitry for FPDs
- · Software adjustable flat panel contrast voltage



Super VGA Controller

The ZT 8982 design is based on the Cirrus GD6440 VGA controller. The GD6440 is a second-generation, fully integrated single-chip solution that contains an internal RAMDAC and frequency synthesizer.

The GD6440 is fully hardware register-compatible with the IBM Super VGA standard and features several Windows performance enhancements such as color expansion and packed pixel memory addressing.

Flat Panel Support

The ZT 8982 supports most types of monochrome and color flat panels, including 8- and 16-bit dual- and single-scan color STN panels and 9-, 12-, and 18-bit color TFT panels. The GD6440 supports12 different classes of FPDs. The user selects specific panel types through configuration jumpers on the ZT 8982. The ZT 8982 also supports SimulSCAN™ operation that allows concurrent output to both a FPD and CRT display.

The ZT 8982 includes power sequencing circuitry that correctly sequences FPD logic, contrast, and backlight voltages. Power sequencing minimizes a flat panel's exposure to potentially destructive DC voltages, extending the life of the panel. The ZT 8982 supplies logic power at +5V, 1.0A, negative contrast voltage at -24V, 30mA, and positive backlight voltage at +12V, 1.0A. For panels that require higher currents, the ZT 8982 provides TTL level control signals for sequencing user-supplied power circuitry.

Another feature of the ZT 8982 is software controlled negative contrast voltage. This feature eliminates the need for an external potentiometer for adjusting the FPD's contrast and is ideal for environments where external potentiometers are not practical or not accessible.

For flat panel support, the ZT 8982 contains a 50-pin dual-row, 2 mm vertical header that supports panels with up to 18-bit displays. This connector is pin-compatible with the 50-pin connector found on the zVID2 Local Bus Super VGA/FPD Video Adapter. This connector also provides access to the keyboard, analog CRT signals, and power-on sequencing signals.

Analog Video Interface

The analog video interface supports IBM-compatible fixed and multi-frequency VGA monitors. A 15-pin right-angle D-shell connector is provided to allow direct connection to VGA monitors.

Video Memory

The ZT 8982 contains 1 Mbyte of high-speed fast page mode DRAM, allowing it to support high-resolution color graphics modes such as 1024 x 768 x 256 colors non-interlaced and 1280 x 1024 x 16 colors interlaced. The video memory is mapped to the standard 0A000 to 0BFFFh VGA memory space.

Video ROM BIOS

The video ROM BIOS is a 128 Kbyte EPROM divided into four 32 Kbyte pages. Jumpers on the upper address lines allow the user to select different BIOS versions. The BIOS is automatically installed during system initialization. The BIOS is mapped to the standard 0C000 to 0C7FFh VGA BIOS memory space.

Video Select Circuitry

The ZT 8982's video select circuitry allows it to work in multi-video configuration. The ZT 8982 contains a video select bit mapped to the STD I/O interface that allows each board (up to eight) in the backplane to be enabled or disabled via software.

AT Keyboard Controller

The ZT 8982 contains an AT keyboard controller (8242) that supports IBM PC/AT-compatible keyboards. The keyboard controller can be disabled for systems that already have a keyboard controller. The keyboard is interfaced through a 10-pin right-angle header and requires an optional cable (ZT 90076) to connect to an IBM AT-compatible keyboard.

STD Bus Interface

The ZT 8982 performs 8- or 16-bit data transfers over STD and STD 32 backplanes. Memory addressing is jumper selectable as either 20- or 24-bit. The video memory is mapped from 0A000 to 0BFFFh and the video BIOS from 0C000 to 0C7FFh. The video I/O registers are mapped from 03B0 to 03DFh, and the keyboard controller is mapped at 0060, 0064h and 0067h.

Software

Ziatech's BIOS (Version 4 or later) fully supports the ZT 8982. The ZT 8982 includes a driver/utility disk with high-resolution drivers for various software packages, including Microsoft Windows 3.x, as well as utilities for functions such as changing video modes and controlling FPD attributes.

Specifications

Electrical

Power Req.	Min.	Тур.	Max.
Supply Voltage, V _{CC}	4.75V	5.0V	5.25V
Supply Current, Vcc=5.0V	570mA	630mA	820mA

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 mechanical specifications
- IBM PC/AT-compatible video and keyboard interfaces
- Height: 0.570"(14.5mm), occupies one card slot
- Weight: 4.5 oz (127.6g)

6

Connectors

E/P: 114-pin card edge connector on

0.0625" (1.588mm) centers

J1: 10-pin, dual-row, right-angle header

for AT keyboard

J2: 50-pin, 2mm header, FPD interface J3: 15-pin D-shell analog video connector J4: 14-pin, dual-row, vertical header,

auxiliary power connector

Environmental		
Operating Temperature	0° to 65° Celsius	
Storage Temperature	-40° to +85° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

Reliability

MTBF: 21 years

MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8982 Super VGA/FPD and Keyboard

Interface

ZT 97104 ZT 8982/zVID2 software utilities and

manual

Accessories

Cable (See Data Book cable section for details):

ZT 90076 32" (81cm) keyboard cable, 10-pin

header to desktop-style DIN

ZT 90166 10" (25.4cm) video/keyboard to

panel mount connector

ZT 90167 10" (25.4cm) video/keyboard to

desktop-style connector

ZT 90168 10" (25.4cm) multi-video/keyboard,

converts seven ZT 8982s to desktop-style connector

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.



STD32°

zVID2

Local Bus Super VGA/FPD Adapter

High-speed Super VGA/Flat Panel Display Adapter brings local bus video performance and flat panel support to Ziatech's ZT 8902 Single Board 486 Computer

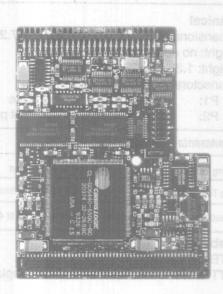
The zVID2 is a 32-bit, high-performance, local bus Super VGA and flat panel display (FPD) adapter for the ZT 8902 Single Board 486 Computer (SBC). The zVID2 operates at the full speed of the CPU, using a 32-bit data path. This allows it to substantially outperform interfaces that use the system backplane or a motherboard's ISA chipset for graphics.

The zVID2 supports most monochrome and color FPDs on the market, including 8- and 16-bit single- and dual-scan color Super Twisted Nematic (STN) panels, and 9-, 12-, and 18-bit Thin Film Transistor (TFT) color panels. The zVID2 contains 1 Mbyte of video memory

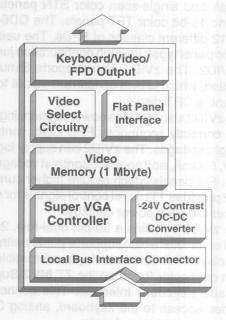
and supports CRT resolutions up to $1024 \times 768 \times 256$ colors, non-interlaced, and $1280 \times 1024 \times 16$ colors, interlaced.

Users can also access the ZT 8902 SBC's keyboard interface, making the zVID2 a space efficient video/keyboard solution. The low-profile zVID2 and ZT 8902 together fit in a single card cage slot.

The zVID2 allows each ZT 8902 SBC in a multiprocessing STD 32 STAR SYSTEM™ to have a separate video display, or to be "daisy-chain" connected in a multiprocessing system, allowing multiple zVID2-equipped processors to share a monitor and keyboard.



- 32-bit high-performance local bus interface
- Supports CPU bus speeds up to 33 MHz
- Up to 10 times the graphics performance of busbased video solutions
- Eliminates backplane bus traffic for video operations
- Microsoft[®] Windows[™] hardware performance features
- One slot for zVID2 and ZT 8902 SBC
- Supports shared or separate video displays in multiprocessing STAR SYSTEMs



- 1 Mbyte high-speed video memory
- Hardware-compatible with IBM Super VGA standard
- 1024 x 768 x 256 colors non-interlaced
- 1280 x 1024 x 16 colors interlaced
- Supports 8- and 16-bit dual- and single-scan color STN panels
- Supports 9-, 12-, and 18-bit color TFT panels
- Simultaneous display of CRT and LCD panels with resolutions up to 1024 x 768 x 256 colors
- · Power sequencing circuitry for FPDs



Local Bus Interface

The zVID2 connects directly to the ZT 8902 Single Board 486 Computer through a 100-pin board-to-board local bus connector.

The local bus interface intercepts 486 CPU read and write cycles sent to video memory or I/O addresses, preventing the ZT 8902's chipset from performing STD Bus transactions. The local interface uses all 32 data bits and operates at the full speed of the 486 CPU's external data bus (up to 33 MHz).

VGA Controller

The zVID2 design incorporates the Cirrus GD6440 VGA controller. The GD6440 is fully hardware register-compatible with the IBM Super VGA standard and features several Windows performance enhancements such as color expansion and packed pixel memory addressing.

Flat Panel Support

The zVID2 supports most types of monochrome and color Flat Panel Displays (FPDs), including 8- and 16-bit dual- and single-scan color STN panels and 9-, 12-, and 18-bit color TFT panels. The GD6440 supports 12 different classes of FPDs. The user selects specific panel types through configuration jumpers on the zVID2. The zVID2 also supports SimulSCAN™ operation, which allows concurrent output to both an FPD and a CRT display.

The zVID2 also includes power sequencing circuitry, which correctly sequences FPD logic, contrast, and backlight voltages. The zVID2 can supply logic power at +5V, 500mA, and negative contrast voltage at -24V, 30mA. For panels which require higher currents, the zVID2 provides TTL level control signals for sequencing user-supplied power circuitry.

The zVID2 contains a 50-pin dual-row, 2mm horizontal connector which supports panels with up to 18-bit displays. This connector is pin-compatible with the 50-pin connector found on the ZT 8982 Super VGA/FPD and Keyboard Interface. This connector also provides access to the keyboard, analog CRT, and power-on sequencing signals.

Video Memory

The zVID2 contains a full 1 Mbyte of high-speed fast page mode DRAM, allowing it to support high resolution color graphics modes such as $1024 \times 768 \times 256$ colors non-interlaced and $1280 \times 1024 \times 16$ colors interlaced. The video memory is mapped to the standard A0000h to BFFFFh VGA memory space.

Video ROM BIOS

The video BIOS for the zVID2 has been combined with the system BIOS and occupies 32 Kbytes in the CPU's memory. On power-up, the BIOS is automatically installed during system initialization.

Video Select Circuitry

The zVID2 is capable of sharing monitors and

keyboards with other zVID2 modules. This feature is controlled by the zVID2's on-board video/keyboard select circuitry, which consists of a video switch and a software controlled video/keyboard select signal. Up to seven ZT 8902/zVID2 pairs can be daisy-chain connected in a Ziatech STD 32 STAR SYSTEM™ to share a common display and keyboard. Using software control, the user can "hot key" to any of the single board computers with a simple key stroke.

Software

The zVID2 is fully supported by Ziatech's BIOS (Version 4.12 or later). The zVID2 includes a driver/ utility disk with high-resolution drivers for various software packages such as Microsoft Windows 3.x, and various utilities for performing functions such as changing video modes.

Specifications

Electrical

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	175mA	196mA	260mA

Mechanical

- Dimensions: 3.75" (9.50cm) x 2.860" (7.26cm)
- Height: no additional slots
- Weight: 1.38 oz. (39.1g)
- Connectors

P1: 100-pin local bus interface
P2: 50-pin video/keyboard/flat panel

Environmental		
Operating Temperature	0° to 65° Celsius	
Storage Temperature	-40° to +85° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

Reliability

- MTBF: 49 years
- MTTR: five minutes (based on board replacement)

Ordering Information

zVID2 Local Bus Super VGA/Flat Panel Display Adapter

ZT 97104 ZT 8982/zVID2 software utilities and

manual

Accessories

Cable (See Data Book cable section for details):

ZT 90166 10" (25.4cm) video/keyboard to panel mount connector

10" (OF App) vides/keyb

ZT 90167 10" (25.4cm) video/keyboard to

desktop-style connector

ZT 90168 10" (25.4cm) multi-video/keyboard,

converts seven zVID2s to desktop-

style connector



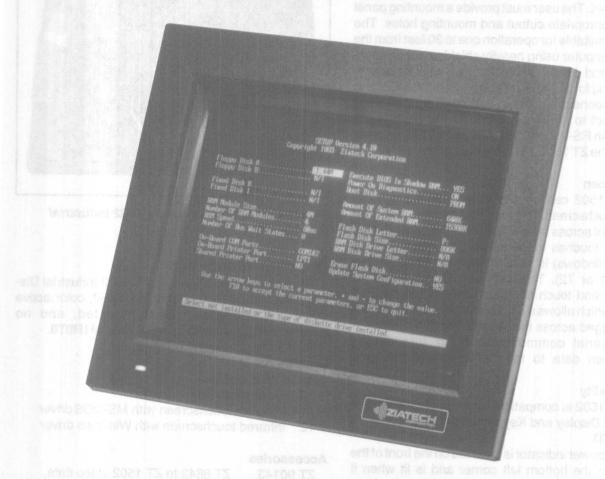
ZT 1502

Industrial Display Unit

A NEMA-rated color VGA flat panel monitor for panel mounting with optional touchscreen

The ZT 1502 Industrial Display Unit (IDU) offers a rugged, space saving alternative to bulky CRT monitors in STD 32® systems requiring a PC-compatible display. The ZT 1502 offers a VGA resolution (640x480) backlit color TFT-LCD display and is NEMA 4- and 12-rated when panel mounted in custom enclosures. The

ZT 1502 may be mounted within 30 feet of the STD 32 computer, using shielded ribbon cable for video data. Power for the display is provided by the computer, so no power supply is required at the display. An infrared touchscreen option is available for applications requiring touch capability on the display surface.



- 640x480 active matrix color TFT-LCD with HCFT backlight
- PC software-compatible flat panel display system
- · Power provided to display by computer
- Low-cost mounting possible up to 30 feet from computer
- · Panel mount (open back, gasket seal)

- Infrared touchscreen option with Microsoft® MS-DOS® or Windows™ software driver
- NEMA 4/12-rated front bezel
- . Shock 15G, 11ms and vibration 1G, 10 to 500 Hz
- Operating temperature range: 0° to 40°C
- FCC Part 15, Class A device approval (pending)
- U. L. rated (pending)



The ZT 1502 uses a 640 column by 480 row active matrix color TFT (Thin Film Transistor) LCD (Liquid Crystal Display) module. This flat panel display incorporates amorphous silicon TFT technology and can display 16 colors. The display incorporates a bright HCFT-backlight unit so the overall display appearance resembles a VGA CRT monitor. This display supports CGA, EGA, and 640 x 480 VGA graphics formats.

Mounting

The ZT 1502 is open-backed and the display unit mounts in a panel cutout. A gasket on the back of the bezel surrounds the LCD display creating a NEMA 4/12-rated seal. The user must provide a mounting panel with the appropriate cutout and mounting holes. The ZT 1502 is suitable for operation one to 30 feet from the STD 32 computer using heavily shielded ribbon cable for video and touchscreen data, as well as heavy-gauge wiring for power. Power signals (+5V, +12V and GND) are connected at the STD 32 card cage terminals and connect to screw terminals on the back of the ZT 1502. An RS-232 ribbon cable carries touchscreen data from the ZT 1502 unit to the host computer's COM serial port.

Touchscreen

The ZT 1502 can be configured with an optional infrared touchscreen. The touchscreen uses beams of infrared light across the surface of the flat panel display to register touches to the screen. A software driver (DOS or Windows) is included with the Touchscreen Option (T1 or T2). This option includes utilities for calibration and touch functions, as well as a mouse emulator which allows a finger to act as a mouse cursor when dragged across the screen. The ZT 1502 uses RS-232 serial communications for transmitting touchscreen data to the COM port of the host computer.

Compatibility

The ZT 1502 is compatible with the ZT 8842 VGA/ Flat Panel Display and Keyboard Interface.

Power LED

An LED power indicator is included on the front of the ZT 1502 in the bottom left corner and is lit when it receives power from the host computer.

Specifications

Electrical

- FCC Part 15, Class A device approval pending
- U.L. 1950 approval pending

Mechanical

- *See attached mechanical drawings for external physical dimensions of ZT 1502.
 - Connectors
 - J3: RS-232 touchscreen data (for 14-pin COM ports), 14-pin header

- J9: Parallel video data (for ZT 1502), 34-pin header
- J11: RS-232 touchscreen data (for 10-pin COM ports), 10-pin header
- J12: Power (+5V, +12V, GND), 3-pin screw terminal, 13 AWG

Reliability

MTBF: 2 years

MTTR: ten minutes (based on replacement of entire unit)

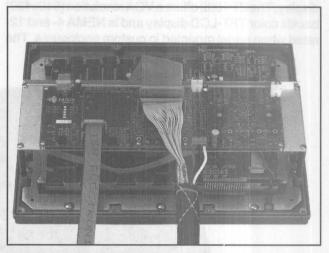


Figure 1. Rear view of the ZT 1502 Industrial Display Unit.

Ordering Information

The base configuration of a ZT 1502 Industrial Display Unit with VGA resolution 640x480, color active matrix LCD display, panel mounted, and no touchscreen, is ordered as a ZT 1502-M1R0T0.

Options

Touchscreen choices

- TO No touchscreen
- T1 Infrared touchscreen with MS-DOS driver
- T2 Infrared touchscreen with Windows driver

Accessories

ZT 90143

ZT 8842 to ZT 1502 video data, touchscreen, and power cable, 10' (3.05m)

The ZT 1502 Industrial Display Unit carries a twoyear warranty, with the exception of the flat panel display (LCD) and touchscreen components, which are warranted for nine months.

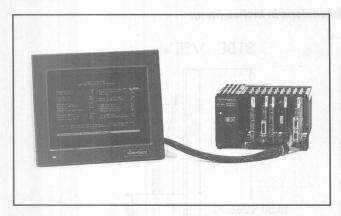


Figure 2. The ZT 1502 operates up to 30 feet away from an STD 32 Computer.

Power Req.	Min.	Тур.	Max.
Supply Voltage, V _{CC}	4.75V	5.0V	5.25V
Supply Current, V _{CC} =5.0V	- 1	0.03A	-
Aux Voltage, V _{aux+}	11.4V	12.0V	12.6V
Aux Current, V _{aux+} =12.0V	-	1.60A*	PK

^{*}Touchscreen option (T1 or T2) adds 0.20A typical @ 12.0V

Display Parameters	
Active Pixel Area	6.496" H x 8.574" W (158.4mm H x 211.2mm W)
Pixel Organization	640 horiz. by 480 vert.
Display Viewing Angle	± 45° horiz., +10°, -30° vert
Display Color	16 colors
Touchscreen	Infrared, 69 x 51

Environmental	
Operating Temperature	0° to 40° Celsius
Storage Temperature	-25° to +60° Celsius
Non-Condensing Relative Humidity*	0% to 95% at 40° Celsius

^{*}Backside of display (front is NEMA 4/12-rated)

• Operating shock: 15G, 11ms

• Operating vibration: 10 to 500 Hz (1G)

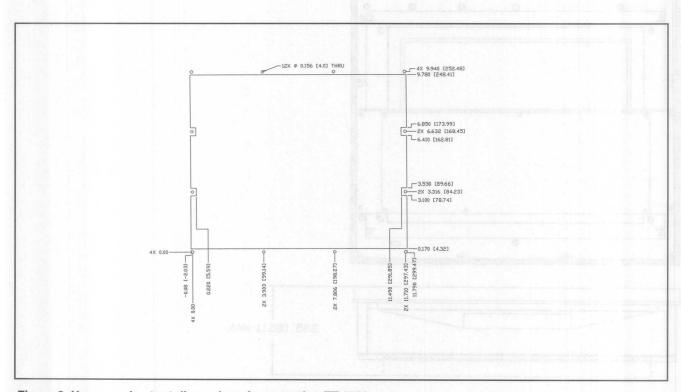
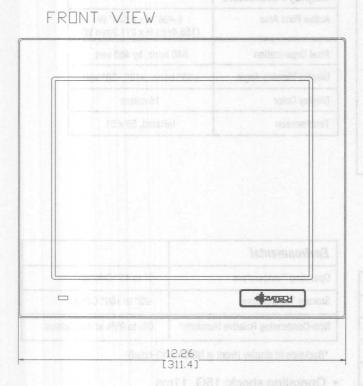
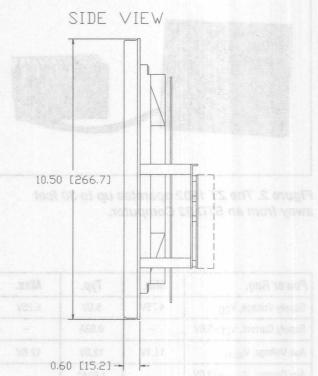


Figure 3. User panel cutout dimensions for mounting ZT 1502

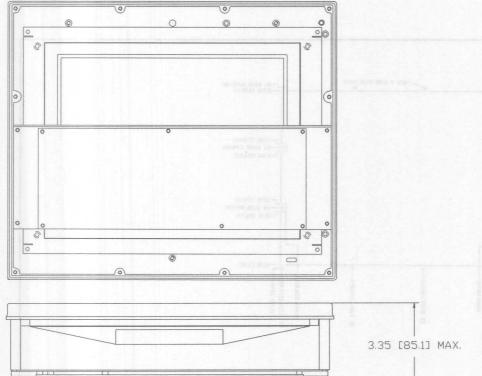


Figure 4. ZT 1502 Industrial Display Unit's mechanical dimensions in inches (mm).





REAR VIEW molterally onlined of





BOTTOM VIEW



STD32°

ELVGA & LCDVGA

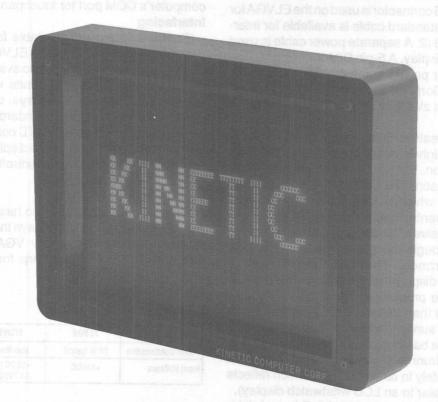
Rugged VGA Displays

Rugged, high resolution flat panel displays for use in exposed and high shock and vibration environments with two display choices and an IR touchpanel option

The Kinetic Computer Corp. ELVGA and LCDVGA are completely sealed display units rated to NEMA 4/12 standards. The ELVGA provides an Electroluminescent (EL) flat panel display with 640x480 resolution that is viewable under most lighting conditions at wide viewing angles. The LCDVGA uses a Liquid Crystal Display (LCD), also in 640x480 resolution, with a choice of transmissive or transflective monochrome LCD display panels.

Both displays provide 307,200 pixels for high resolu-

tion graphics or text and can be easily driven from Ziatech's ZT 8842 VGA/Flat Panel Display and Keyboard Interface as well as the zVID2 Local Bus Super VGA/Flat Panel Display Adapter and the ZT 8982 Super VGA/Flat Panel and Keyboard Interface. This combination provides PC-software compatibility in a rugged package ideal for mobile vehicle, factory, military and outdoor data entry applications. Both the ELVGA and LCDVGA displays are available with an optional 69x51 infrared (IR) touchpanel for user input.



- Rugged, sealed to NEMA 4/12 standards
- Compact 11.5" x 8.6" x 2.5" maximum
- High resolution 640x480 displays
- EL or LCD display types
- 69x51 touch points with IR touchpanel option
- Software for integrating touch input into Windows
- Extended temperature versions available
- 50G shock
- Extended distance interface available
- One-year parts and labor warranty



KINETIC COMPUTER CORP.

TEL>617.547.2424 FAX>617.547.7266



Both the ELVGA and LCDVGA Rugged VGA Displays are housed in black, anodized aluminum enclosures sealed for a NEMA 4/12 rating. They can be mounted using mounting locations on the back side. Electroluminescent (EL) and LCD displays each have their own characteristics depending on the environment they will be used in.

ELVGA

EL displays feature high contrast (100:1), bright amber displays on a black background which yield very wide viewing angles (exceeding 160° C). EL displays are also very rugged, capable of handling high levels of shock and vibration. The ELVGA display supports all standard VGA modes and employs a 16-level gray scale technique utilizing a combination of true levels and pixel patterning.

The ELVGA interfaces to any standard IBM feature connector such as the one on Ziatech's ZT 8842 video controller. A DB-25 connector is used on the ELVGA for video data and a standard cable is available for interfacing to the ZT 8842. A separate power cable is used for powering the display. A 5-pin DIN connector on the display is used for powering the display. Contact Kinetic Computer Corp. or Ziatech for cable requirements to Ziatech's zVID2 or ZT 8982 video cards.

LCDVGA

LCD displays feature crisp, black-on-white backgrounds and a high-contrast appearance, with low power consumption. They are popular in laptop computers for this reason. The LCDVGA-T is a transmissive LCD display which is ideal for a wide range of ambient environments, from completely dark to bright lighting. Transmissive LCD displays use a backlight to transmit light through the glass, producing a high contrast appearance. The LCDVGA-F uses a transflective LCD display that provides both transmissive and reflective properties. Transflective displays are lower contrast than transmissive displays but can be used in direct sunlight with excellent results. The LCDVGA-F uses a backlight as a light source in low to medium light environments, and the backlight can be turned off completely in direct sunlight, which reflects ambient light (similar to an LCD wristwatch display).

Both the LCDVGA-T and LCDVGA-F have brightness and contrast knobs for controlling the display's appearance under different lighting conditions. A special anti-reflective filter is used with the LCDVGA-F to enhance the display appearance in direct sunlight conditions. Extended temperature versions are available providing operation down to -30° C.

Both the LCDVGA-T and LCDVGA-F interface to Ziatech's ZT 8842 video controller using a 25-pin cable that provides both display data and power from the

computer. An additional 5-pin DIN connector is provided for power input if the extended temperature option (Opt ET) for powering an internal heater. Contact Kinetic Computer Corp. for cable requirements for interfacing to the zVID2 and ZT 8982 video controllers.

Touchpanel
A 69x51 infrared (IR) touchpanel is available as an option for both the ELVGA and LCDVGA displays. Infrared light beams just above the surface of the display detect a screen touch point and identify whether it is an initial contact or a final contact (the user removes his finger from the screen). This functionality is handled by an MS-DOS or Windows driver available as an option.

The rugged IR touchpanel does not compromise the NEMA 4/12 seal of the display, yet enables user input to be added to the application. Both the ELVGA and LCDVGA include NEMA-rated DB-9 connectors which provide a standard RS-232 serial connection to the computer's COM port for touchpanel data.

Interfacing

Standard cables are available for flat panel video data from the ZT 8842 to the ELVGA and LCDVGA. Separate power cables are also available for powering the ELVGA and LCDVGA units with the extended temperature option. Displays ordered with the touchpanel option can use standard RS-232 cables for the connection between the STD computer's COM port and the DB-9 connector on the display. Custom cables for interfacing to other video controllers can be ordered by Kinetic Computer Corp.

Analog VGA Interface

Kinetic Computer Corp. also has rugged, color and monochrome LCD VGA displays that accept standard analog VGA input from any VGA video controller. Contact Kinetic Computer Corp. for more information.

Specifications Electrical

Power Req.	ELVGA	LCDVGA-T	LCDVGA-F
Power Consumption	18 W typical	less than 3 W	less than 3 W
Input Voltages	+12VDC	+5VDC (logic), -18.7VDC (LCD)	+5VDC (logic), 18.7VDC (LCD)

Mechanica

• ELVGA meets SAE specification J1455 for operation on heavy-duty trucks and buses, ARINC specification ATCS 110 for operation on train locomotives, in addition to NEMA 4/12.

ELVGA and LCDVGA Rugged VGA Displays

Physical Characteristics	ELVGA	LCDVGA-T	LCDVGA-F
Dimensions	11.5"W x 6.6"H x 2.25"D	11.5"W x 6.6"H x 2.25"D	11.5"W x 6.6"H x 2.25"D
Weight	10 lbs.	10 lbs.	10 lbs.

Environmental	ELVGA	LCDVGA-T	LCDVGA-F
Operating Temperature	0° to 55° Celsius *	0° to 45° Celsius *	0° to 45° Celsius *
Storage Temperature	-40° to +75° Celsius	-40° to +45° Celsius	-40° to +45° Celsius
Relative Humidity	0 to 100%	0 to 100%	0 to 100%
Vibration	5 to 55 Hz (.030° p-p) 55 to 500 Hz 1G peak	10 to 75 Hz (.003" p-p) 58 to 500 Hz 1G peak	10 to 57 Hz (.003" p-p) 58 to 500 Hz 1G peak
Shock	50G	50G	50G

^{*} Optional operating temperature of -20° to +70° C available

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ELVGA Electroluminescent VGA display LCDVGA-T Monochrome LCD VGA display

(transmissive)

LCDVGA-F Monochrome LCD VGA display

(transflective)

Options

Opt TP IR touchpanel option

Opt TB MS-DOS touch software option
Opt TW Windows touch software option

Opt ET -30° C extended temperature option

(LCDVGA only)

Accessories

Cables

Opt EL-CAB 6' shielded VGA video data

cable - ZT 8842 to ELVGA

Opt POW-CAB 6' power cable for ELVGA or

LCDVGA with Opt ET

Opt LCD-CAB 10' shielded VGA video data

and power - ZT 8842 to

LCDVGA

Custom cables can be ordered to meet customer specifications. Contact Kinetic Computer for details.

Display Information	ELVGA	LCDVGA-T	LCDVGA-F
Technology	Electroluminescent	Transmissive LCD	Transflective LCD
Resolution	640 x 480 pixels	640 x 480 pixels	640 x 480 pixels
Active Viewing Area	8.13" x 6.19"	7.72" x 5.81"	7.72" x 5.81"
Diagonal	10.2"	9.7"	9.7"
Viewing Angle	160° cone	50° cone	55° cone
Contrast Ratio	100:1	18:1	10:1
Pixel Brightness	35 fL (typical)	19 fL	12 fL
Backlight	None	CCFT (edge-lit)	CCFT (edge-lit)
Color	585nm (yellow-orange)	Black dot on white background	Black dot on white background
Touchpanel	69 x 51 IR	69 x 51 IR	69 x 51 IR





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STD Bus Serial I/O

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STD Bus Serial I/O Product Feature Guide

Product*	Special Features	Type and Quantity of Channels	Interrupt Controller	Maximum Data Rate	-40° to +85 Celsius
ZT 88CT41 Quad Serial Interface	Optional Opto Isolation Optional FIFO	(2) RS-232 (2) RS-232/422/485	*	56K	•
ZT 8843 Modem for STD Bus	Speaker, LEDs	RJ-11 Phone RJ-11 Line		2400 bps	
ZT 88CT75 Centronics and Serial Interface	8 lines of parallel I/O, [*] Watchdog timer	(2) RS-232/422/485		56K	•
ZT 8932 Intelligent, Multi-Channel Serial Controller	On-board CPU with dual-port RAM, 8 lines of digital I/O	(6) RS-232 (2) RS-232/485 (1) 3-wire RS-232	•	115K	

Also Inside This Section

• UE9002 Interbus-S Interface

Four-channel serial data communications board combines low power consumption and extended temperature operation

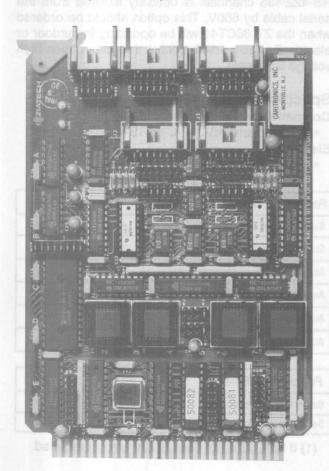
The ZT 88CT41 is a four-channel serial interface board for STD Bus systems. This interface features four 82050 UARTs (8250-compatible) that operate at speeds up to 56K baud in DTE or DCE configurations.

For easier programming, each 82050 UART features directly addressable registers, direct hardware interrupt capability, and individual baud rate generators.

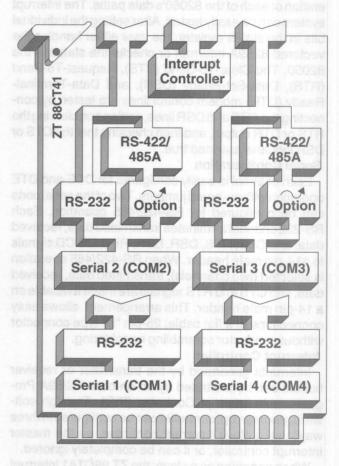
Interrupts generated by the transmitter or receiver

buffers are arbitrated by an on-board 8259A Programmable Interrupt Controller (PIC). The 8259A PIC can provide unique interrupt vectors for the STD CPU.

The ZT 88CT41 is a TTL backplane-compatible CMOS interface with low power consumption and an extended temperature operating range of -40°C to +85°C. It can be used with either TTL or CMOS STD Bus systems.



- STD 32®- and STD-compatible
 - Four independent serial channels (independent 82050 UARTs)
 - Four RS-232 channels with two channels configurable for RS-422/485
 - Programmable baud rates to 56K
 - TTL backplane-compatible CMOS for low power



- Extended temperature operation (-40° to +85°C)
- On-board interrupt controller
- Loopback diagnostic capability
- Optional optical isolation on RS-422/485 channels
- Optional four-byte transmit and receive FIFO for each channel

Note: CT denotes CMOS, TTL backplane-compatible and extended temperature operation of -40 $^{\circ}$ to +85 $^{\circ}$ C (Users should make adjustments for temperature rise in enclosures.)



Functional Considerations Serial Controller

Each of the four serial channels of the ZT 88CT41 has an independent 82050 Universal Asynchronous Receiver/Transmitter (UART) chip. The 82050 chip is fully backward-compatible with the 8250 UART, the chip used in the original IBM PC. Each 82050 UART has individual baud rate generators operating from 50 to 56,000 baud; directly addressable registers for status, control, and data; and fully programmable serial interface characteristics. These characteristics include 5-, 6-, 7-, or 8-bit character transmission; even, odd, or no parity bit generation and detection; and 1-, 1-1/2, or 2-stop-bit generation.

For loopback testing, each serial channel's transmitter shift register output can be internally connected to the receiver shift register. This verifies the correct operation of each of the 82050's data paths. The interrupt system can be easily tested. After setting the individual bits in the status register, the user either handles the vectored 8259A interrupt or checks the status in the 82050. The Clear-To-Send (CTS), Request-To-Send (RTS), Data-Set-Ready (DSR), and Data-Terminal-Ready (DTR) modern control lines are tested by connecting the CTS and DSR lines, setting and clearing the RTS or DTR output, and then checking that the CTS or DSR signal is asserted true.

Serial Configuration

Each channel is easily configured for DCE and DTE operation with on-board jumpers. Two of the serial ports can be configured for RS-422/485 operation. Each RS-232 channel terminates transmitted data, received data, and CTS, RTS, DSR, DTR, RI, and DCD signals to a14-pin male header. When RS-422/485 operation is selected (two channels), transmitted data, received data, and CTS and RTS signals are made available on a 14-pin male header. This arrangement allows easy connections to a flat cable, 25-pin "D" type connector without conductor scrambling or soldering.

Interrupt Controller

Interrupts generated by the transmitter or receiver buffers can be arbitrated by an on-board 8259A Programmable Interrupt Controller (PIC). Through software, the interrupt controller can be configured in three ways: as a slave interrupt controller, as the master interrupt controller, or it can be completely ignored.

When operating as a slave, the ZT 88CT41 interrupt controller receives the 8252A cascade address over STD Bus address lines A8 through A10 as defined in the STD-80 Bus Specification. When the cascade address is received, the PIC outputs a unique vector for each of the on-board UARTs.

Base Address Selection

The ZT 88CT41 requires 40 I/O port addresses. The upper six address lines are jumper-selectable for any 16-bit I/O address generated by an 80x86 CPU. For IBM

PC-compatible operation, the UARTs can be located at 3F8h (COM1), 2F8h (COM2), 3E8h (COM3), and 2E8h (COM4), with the default PIC at 0A8h or 020h. The upper six address lines are factory-jumpered for zero.

FIFO Option

When the FIFO option is ordered, each serial channel will have dual four-byte transmit and receive First In First Out (FIFO) buffers. Each FIFO buffer can be configured to be from one to four bytes in length, with interrupt capability.

The FIFO option also features UARTs that operate from DC to 288K baud, have a power-down mode, and have MCS-51 support. MCS-51 allows multiprocessor communications over the serial link.

Optical Isolation Option

When optical isolation is ordered, each of the RS-422/485 channels is optically isolated from the serial cable by 600V. This option should be ordered when the ZT 88CT41 will be operating in outdoor or electrically noisy environments that may cause high voltage transients.

Specifications

Compatibility

• EIA Standard RS-232-C or RS-422/485

Electrical

• Data Rate: 56 Kbaud maximum

Power Req. (RS-232)	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, V _{CC} =5.0V	-	92mA	200mA
Aux Voltage, V _{aux+}	10.8V	12.0V	13.2V
Aux Current, V _{aux+} =12.0V	-1-1	30mA	60mA
Aux Voltage, V _{aux} -	-13.2V	-12.0V	-10.8V
Aux Current, Vaux-=-12.0V	-	30mA	60mA

Power Req. (RS-485)	Min.	Тур.	Max.
Supply Voltage, Vcc (1)	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	-	162mA	345mA

(1) If RS-232 is not used, ±12V are not required.

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 mechanical specifications
- Occupies one STD slot (0.065" or 1.603cm)
- Connectors

J1-J4: 14-pin latching male headers for serial I/O

J5: 10-pin latching male header for frontplane interrupt access

Environmental	
Operating Temp. (RS-232)	-40° to +85° Celsius
Operating Temp. (RS-422/485)	0° to 65° Celsius
Storage Temperature	-55° to +105° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

STD 32 Compliance Level

• I/O Slave: SA8-I, ICA

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz).

Reliability

• MTBF: 25 years

MTTR: five minutes (based on board replacement)

Ordering Information

Ordering innorm	iation
ZT 88CT41-D1	Quad Serial Interface and
	RS-232/422/485 drivers
ZT M88CT41	ZT 88CT41 manual
D1	RS-232/422/485 drivers
D2	Add FIFO to all channels
D3	Add optical isolation to RS-422/
	RS-485 channels
D4	Add options D2 and D3 to board

Accessories

Cables (see Data Book cable section for details): ZT 90014 40" (1m), 14-pin to 25-pin female

ZT 90014 40" (1m), 14-pin to 25-pin female 40" (1m), 14-pin to 25-pin male ZT 90063 8.25" (21cm), frontplane interrupt

All products are shipped FOB San Luis Obispo, CA USA. OEM discounts are available for some products. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.



ZT 8843

2400 BPS Modem

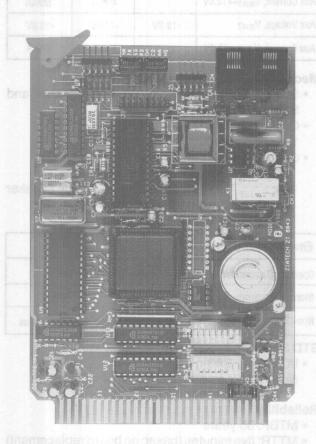
Modem interface features data rates up to 2400 bps, auto answer/dial capability

The ZT 8843 provides modem capability to STD 32® and STD Bus computers at data rates of 300, 1200, and 2400 bits per second (bps). Automatic answer capabilities allow for unattended operation, while a speaker interface allows on- or off-board audible phone line monitoring. Call progress and additional monitoring are provided by eight on-board LEDs.

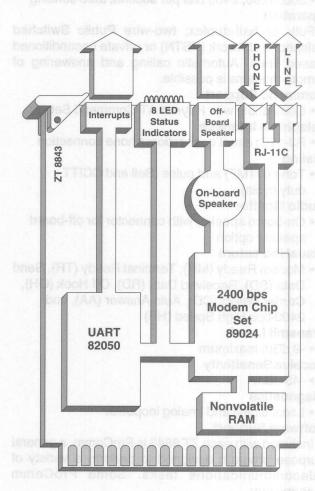
The ZT 8843 is fully compatible with the industry standard Hayes® AT Command Set, providing access to a vast range of existing PC communications software.

If a standard communications software package is not used, the Hayes command set allows easy programming of the ZT 8843.

In addition to linking STD systems over phone lines, the ZT 8843 enables an STD system in the field to be remotely diagnosed through a modem hookup. Modem-equipped STD systems can also be programmed to collect data and automatically provide updates to a central control system.



- STD 32- and STD-compatible
- Direct telephone interfaceLocal digital and analog loopback
- · Auto answer/dial
- TTL-compatible CMOS to minimize power consumption



- 1024-bit non-volatile phone number and configuration memory
- Hayes® AT-compatible
- Burned-in at 55° C and tested to guarantee reliability



Modem Interface

The on-board modem circuitry is interfaced to the STD Bus via an 82050 (8250-compatible) UART. This UART can be addressed as COM1, 2, 3, or 4 as needed by a DOS system. For non-DOS systems, the UART is addressable on any 8-port I/O boundary within the 64K I/O address map. The modem specifications follow.

Compatibility

Bell 103, 212A; CCITT V.21, V.22, and V.22bis provide dual communication standards. Bell 103 and 212A are U.S. standards for 300 and 1200 bps, while CCITT V.21 (300 bps), V.22 (1200 bps), and V.22bis (2400 bps) are international standards.

Data Rate

300, 1200, 2400 bits per second, auto sensing
 Operation

Full- or half-duplex; two-wire Public Switched Telephone Network (PSTN) or private unconditioned leased lines. Automatic calling and answering of remote modems is possible.

Command Support

Compatible with Hayes® AT Command Set

Telephone Interface

- RJ-11C; direct connection; phone connection
 Dialing
 - Tone (DTMF) and pulse (Bell and CCITT duty cycle)

Audio Monitor

On-board speaker with connector for off-board speaker option

Visual Indicators

 Modem Ready (MR), Terminal Ready (TR), Send Data (SD), Received Data (RD), Off Hook (OH), Carrier Detect (CD), Auto Answer (AA), and 2400 bps High Speed (HS)

Transmit Level

• -9 dBm maximum

Receive Sensitivity

• -45 dBm

Diagnostics

Local digital and analog loopback

Software Support

Included with each ZT 8843 is ProComm, a general purpose program designed to perform a variety of telecommunications tasks. Some ProComm features are:

- Terminal emulation
- Dialing directory
- Automatic redial facilities
- Transfer protocols such as XMODEM, Kermit, and Telink
- Command file for automatic log-on and unattended operation

Base Address Selection

The ZT 8843 requires eight I/O port addresses. The base address is jumper-selectable on any 8-byte boundary within the 8- or 16-bit I/O address generated by the CPU.

Specifications

Compatibility

- Compatible with Bell 103, 212A (300, 1200 baud)
- Compatible with CCITT V.21, V.22, V.22bis (300, 1200, 2400 baud)
- Compatible with Hayes® AT Command Set

Electrical

• Data Rates 300, 1200, 2400 baud

Power Req.	Min.	Тур.	Max.
Supply Voltage, VCC	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	moo DS pi	450mA	800mA
Aux Voltage, Vaux1	10.8V	12.0V	13.2V
Aux Current, Vaux1=+12.0V		40mA	80mA
Aux Voltage, V _{aux2}	-13.2V	-12.0V	-10.8V
Aux Current, Vaux2=-12.0V	90. - 10. 77	40mA	80mA

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 mechanical specifications
- Occupies one STD slot (0.625" or 15.90mm spacing)
- Connectors

J1, J2: RJ-11C telephone connectors

J3: Two-pin connector for external speaker

J4: 10-pin right-angle male header for frontplane interrupt access

Environmental	
Operating Temperature	-10° to +80° Celsius
Storage Temperature	-40° to +125° Celsius
Non-Condensing Relative Humidity	less than 90% at 40° Celsius

STD 32 Compliance Level

I/O Slave: SA8-I

Note: SA8 is equivalent to STD Series Rev. 2.3 (5 and 8 MHz)

Reliability

MTBF: 35 years

• MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8843 2400 BPS Modem Interface,

modem software

ZT M8843 ZT 8843 manual

Accessories

Cable (see Data Book cable section for details):

ZT 90063 8.25" (21.0cm), one 26-pin and

four 10-pin

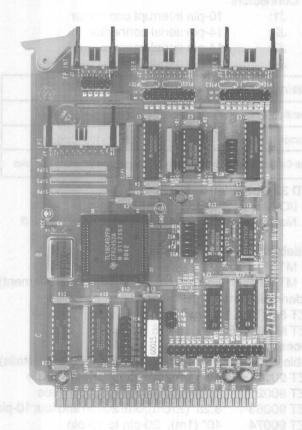


Expansion card provides two serial ports, a parallel (Centronics) I/O interface, and a two-stage watchdog timer for STD 32® and STD Bus systems

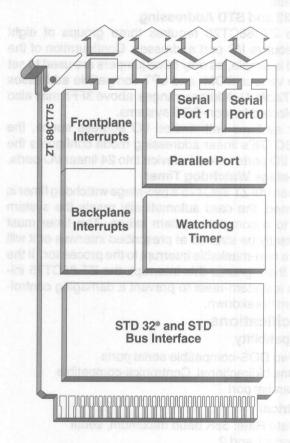
The ZT 88CT75 provides two individually programmable serial ports and a bidirectional, Centronics-compatible parallel port on a single STD card. The serial ports can be configured for RS-232 DTE/DCE or RS-485 operation, and the parallel port can operate as a bidirectional 8-bit data port or as a printer interface. Both serial ports are 8250A-style components to

ensure PC/AT compatibility. The ZT 88CT75 also provides a two-stage watchdog timer for STD systems.

The ZT 88CT75 utilizes CMOS components to ensure reliable operation in extended temperature environments (-40° to +85° C) and to minimize power consumption.



- STD 32- and STD-compatible
- Two fully programmable serial I/O channels, configurable for RS-232 or RS-485 operation
- Independent DTE or DCE configuration for each serial port
- Serial and parallel printer ports are PC/AT-compatible
- Programmable baud-rate generator and modem control signals for each serial channel
- Loopback controls for fault isolation on each serial channel



- Fully prioritized independent interrupt controls
- Bidirectional, Centronics-compatible parallel port
- Linear addressing mode available to minimize system I/O port requirements
- · 8- and 16-bit I/O addressing
- Two-stage watchdog timer
- Software support via Ziatech's STD Device Driver Package (STD DDP)
- Burned-in at 55° C and tested to guarantee reliability

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40° to $+85^{\circ}$ C. (Users should make adjustments for temperature rise in enclosures.)



Centronics and Serial Interface

The 16C452B chip used by the ZT 88CT75 features two fully programmable, 8250A-compatible serial I/O channels with complete status reporting capabilities. Each serial channel has a programmable baud-rate generator, modem control signals, and selectable baud rates from 50 to 56 Kbaud.

Each channel is also double-buffered to allow read/write operations to be performed simultaneously with serial-to-parallel or parallel-to-serial conversions.

The 16C452B also features a bidirectional, Centronics-compatible parallel port. This port can be used as a byte-wide parallel I/O port or as a printer interface.

STD 32 and STD Addressing

The ZT 88CT75 requires three groups of eight consecutive I/O port addresses. Configuration of the board is simple, as only three jumpers are used to set these various COM- and LPT-compatible addresses (see Table 1). Address ranges above 3FFh may also be selected for non-DOS systems.

For systems with limited I/O address space, the ZT 88CT75's linear addressing mode configures the eight I/O ports for each device into 24 linear I/O ports. **Two-stage Watchdog Timer**

When the ZT 88CT75's two-stage watchdog timer is activated, the card automatically resets the system prior to a complete system failure. The timer must constantly be strobed at prescribed intervals or it will send a non-maskable interrupt to the processor. If the CPU then ignores this interrupt, the ZT 88CT75 initiates a system-reset to prevent a damaging control-system breakdown.

Specifications Compatibility

- Two DOS-compatible serial ports
- One bidirectional, Centronics-compatible parallel port

Electrical

Table 1.

 Data Rate: 56K baud maximum, serial ports 1 and 2

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.0V	5.25V
Supply Current, V _{CC} =5.0V		60mA	120mA
Aux Voltage, Vaux+	11.4V	12.0V	12.6V
Aux Current, Vaux+ = 12.0V		200μΑ	800µА
Aux Voltage, Vaux-	-12.6V	-12.0V	-11.4V
Aux Current, Vaux- = -12.0V	owi seok	680μA	1200µA

Mechanical

- Size- and backplane-compatible with STD 32 and STD mechanical specifications
- Occupies one STD slot (0.625" or 1.59cm spacing)
- Connectors

J1: 10-pin interrupt connector
J2: 14-pin serial connector
J3: 14-pin serial connector
J4: 20-pin parallel connector

Environmental		
Operating Temperature	-40° to +85° Celsius	
Storage Temperature	-55° to +105° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

STD 32 Compliance Level

I/O Slave: SA8-1

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz).

Reliability

- MTBF: 76 years
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 88CT75 Centronics and Serial Interface

ZT M88CT75 ZT 88CT75 manual

Accessories

Cables (see Data Book cable section for more details):

ZT 90014 40" (1m), 14-pin to 25-pin female ZT 90027 40" (1m), 14-pin to 25-pin male ZT 90063 8.25" (21cm), one 26-pin and four 10-pin

7T 90074 40" (1m) 20 pin to 25 pin

ZT 90074 40" (1m), 20-pin to 25-pin

*Linear Addressing Mode (x0E0-x0F7h)

W46	W45	W44	СОМ	СОМ	LPT
IN	IN	IN ON	2 (02F8-02FFh)	3 (03E8-03EFh)	2 (0278-027Fh)
IN	IN	OUT	1 (03F8-03FFh)	2 (02F8-02FFh)	2 (0278-027Fh)
IN	OUT	IN	* (x0E0-x0E7h)	* (x0E8-x0EFh)	* (x0F0-x0F7h)
IN	OUT	OUT	2 (02F8-02FFh)	3 (03E8-03EFh)	1 (0378-037Fh)
OUT	IN	IN	1 (03F8-03FFh)	2 (02F8-02FFh)	1 (0378-037Fh)
OUT	IN	OUT	3 (03E8-03EFh)	4 (02E8-02EFh)	1 (0378-037Fh)
OUT	OUT	IN	3 (03E8-03EFh)	4 (02E8-02EFh)	2 (0278-027Fh)
OUT	OUT	OUT	3 (03E8-03EFh)	4 (02E8-02EFh)	3 (03BC-03BFh)





ZT 8932

Intelligent, Multi-Channel Serial Controller

High-density, high-performance, eight-channel serial controller with 16 MHz V53 processor

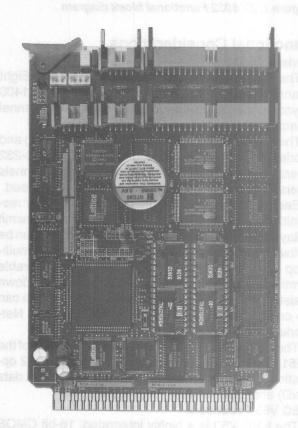
The ZT 8932 is an Intelligent Serial Controller for STD 32® Bus or stand-alone applications. Its on-board 16 MHz V53 (286 class) processor manages eight asynchronous serial channels with a ninth channel available for development and debugging. The eight serial channels include 12 byte FIFOs and full modem handshake capability. Two channels are configurable for RS-485 operation. Communication rates up to 115 Kbaud are supported.

The ZT 8932 and the host processor communicate through 16 Kbytes of dual-port RAM located in the ZT 8932. The RAM is selectable by the host processor so that up to eight ZT 8932 controllers can occupy the same memory space in a system. The dual-port interface supports interrupt driven and locked transfers to reduce bus traffic and increase performance.

Up to 1 Mbyte of on-board RAM and 1 Mbyte of flash EPROM provide ample space for user-written communication applications and offer enough flexibility for stand-alone applications. A version of the board is available without the dual-port logic (ZT 89132).

The ZT 8932 can be ordered with an on-board communications executive and host software driver for DOS (other operating environments will follow). This driver provides extended COM support. Alternatively, users can develop their own communications front-end software using Ziatech's powerful development environment, STD ROM. STD ROM can also be used to develop stand-alone communications applications for the ZT 89132.

- Eight asynchronous RS-232 channels with modem control (CD-CL1400)
- Individual transfer rates to 115 Kbaud
- Combined transfer rates to 19.2 Kbaud
- 16 MHz, V53 (286 class) microprocessor
- 12 byte FIFO support per channel
- Up to 1 Mbyte flash/ROM
- Up to 1 Mbyte total, optional battery backup
- 32 Kbyte dual-port RAM
- Two channels configurable for 2- or 4-wire RS-422/485 operation
- Host interface-compatible with Star Gate[™]
 Avanstar 100 Series software
- Additional RS-232 channel for development and debug
- +5V operation (±12V not required)
- Three 16-bit timers (8254)
 - Eight bidirectional digital I/O lines with event sense
- Real-time clock, optional battery backup
- •AC/DC power-fail detection
- Single-stage watchdog timer
- Push-button reset
- User-written applications supported





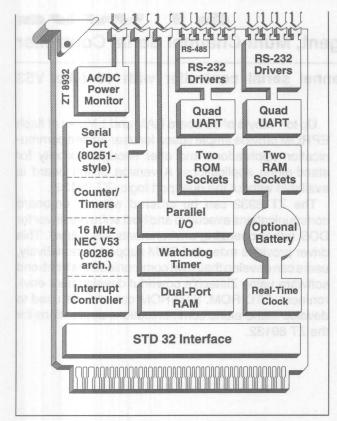


Figure 1. ZT 8932 Functional block diagram

Serial Interface

The ZT 8932 provides nine serial channels. Eight channels are available via the Cirrus Logic CD-CL1400 asynchronous serial controller, and the ninth channel is implemented via the V53 microprocessor.

The CD-CL1400 chip supports all handshaking and modem control signals configured as DTE for RS-232 operation. The overall throughput with all channels operating continuously is approximately 19.2 Kbaud.

Each serial channel features special character recognition/generation and the ability to insert transmit delays in the data stream. One or two channels can be software selected for RS-422/485 operation. For multidrop applications, the ZT 8932 features jumperable termination resistors and socketed pull-up/pull-down resistor SIPs. One or two of the RS-485 channels can be configured for SAE-J1708 for Vehicle Area Networks (VAN).

The V53 provides one serial channel (a subset of the 8251A) optionally configured as DTE for RS-232 operation. This serial channel supports the transmit data (TxD) and receive data (RxD) signals only.

NEC V53 Processor

The NEC V53 is a highly integrated, 16-bit CMOS microprocessor. The V53 includes several standard

the 80286 CPU. The processor has been optimized to execute instructions up to 20% faster than an 80286 operating at the same clock frequency. The primary difference between the V53 CPU and the 80286 is in the method used to address memory between the 1 Mbyte and 16 Mbyte address range.

The V53 uses an extended addressing scheme to software bank select from the 16 Mbyte physical address range. It does not support the protected address mode available on the 80286.

Memory Addressing

Local memory consists of two pairs of sockets for use by the V53 microprocessor. One pair of 32-pin memory sockets accepts RAM devices (32, 128, 256, and 512 Kbyte) with standard 0.6-inch DIP package. The other pair accepts ROM/EPROM devices (32, 128, 256, and 512 Kbyte) and flash devices (128, 256, and 512 Kbyte) with a standard 32-pin PLCC package. Flash devices requiring +12V for programming can use the ZT 8932's on-board voltage generator with software shutdown capability.

The ZT 8932 does not allow an STD Bus host CPU to access its local memory.

Bus Interface

The ZT 8932 (not the ZT 89132) includes 16 Kbytes of software-selectable RAM that can be accessed by both the V53 microprocessor and the STD 32 host processor. The hardware handles all arbitration for simultaneous access. To increase system performance, the dual-port memory is physically separated from the local memory. This permits the V53 to continue executing local instructions at full speed while a host processor accesses the shared memory. The host processor can also continue to execute instructions while the V53 is accessing dual-port memory. Only when both processors attempt a dual-port access is the operation of one suspended until the other is completed. Repetitive accesses from both processors are interleaved on an instruction basis. The dual-port memory also supports software mechanisms to facilitate software communication. A locking mechanism allows either the master processor or the V53 to keep the other from accessing the dual-port memory until the lock is removed. The host processor can enable one of eight ZT 8932s on the bus via a memory port. This saves valuable BIOS extension memory space in large systems.

Digital I/O Interface

Eight buffered parallel I/O lines can be programmed for input or output with read back operation. The open collector outputs sink 12mA (suitable for driving LEDs, low current lamps, etc.) and do not glitch during power-up or power-down. Event sense capability can optionally generate an interrupt on a negative or positive edge.

ZT 8932 Intelligent, Multi-Channel Serial Controller

Interrupts

The interrupt controller (8259) within the V53 supports eight maskable inputs. Features of the interrupt controller include level- and edge-triggered sensing, fixed and rotating priorities, and the ability to mask individual inputs. There are eight interrupt sources, timer 0, serial I/O, V53 serial I/O, real-time clock, parallel I/O event sense, and STD Bus.

The serial interrupts provide a versatile and efficient mechanism for servicing modem, transmit data, receive data, and error condition service requests. Each service request is "daisy-chained" between the two CL-CD1400 devices. This allows them to arbitrate and set priorities between themselves regarding which type of service request is asserted. Once the request is asserted, the V53 can read a "vector" register and serial channel register within the CL-CD1400 to determine a response. Once executed (load transmit FIFO, read receive FIFO, etc.), it issues an "end-of-service."

Counter/Timers

The V53 includes three independent, 16-bit timers (8254). An interrupt can be generated on the end-ofcount for timer 0.

Watchdog Timer

The ZT 8932's watchdog timer monitors system operation. If enabled, the watchdog timer must be strobed at a periodic rate of 100ms by the application software. Failure to strobe the watchdog timer will result in an on-board reset 100 to 600ms later.

Real-Time Clock

The real-time clock uses the National Semiconductor 8572A to perform time keeping functions and includes 44 bytes of RAM. Time keeping features include resolution down to 0.01 seconds, 12- or 24-hour operation, leap year adjustment, rollover status, time comparison and periodic interrupts, and automatic time logging in the event of power failure. With the optional battery installed, these features continue to operate when power is removed.

AC Power-Fail Protection

With the addition of an optional AC transformer, AC power can be monitored to permit an orderly shutdown during a power failure. When AC power falls below an acceptable operating range, a non-maskable interrupt is generated to notify the V53 microprocessor of the impending AC power failure. The application software can then save critical data before the processor is reset by the precision on-board reset circuitry.

Software Support

Intelligent Serial Controller (ISC) Software

The ZT 8932 can be ordered with the Intelligent Serial Controller (ISC) executive software and drivers. The host interface is compatible with the Star Gate Avanstar 100 Series of PC-based controllers. This

includes a software executive on the ZT 8932 that handles all the communication channels and exchanges data with the host processor via buffers in the dual-port RAM. Device drivers on the host processor provide operating system support for the eight serial channels on the ZT 8932. Microsoft® MS-DOS® support is now available with other operating environments under development.

User Written Applications

Users requiring specialized processing of serial data may want to develop their own applications for the ZT 8932's on-board processor. Developing code for the ZT 8932 is relatively simple because the controller is based on PC architecture. Ziatech's STD ROM package supports standard Borland and Microsoft "C" compilers for both source level debugging and embedding in flash EPROM. Additionally, the device driver package includes linkable library routines for buffered, interrupt driven communications over the serial channels. Full "C" source code for these routines lets the user customize them for specific requirements. STD ROM also includes utilities for on-board programming of the flash EPROM, downloading new applications, and communicating through the dual-port RAM. An onboard jumper selects whether to boot a user application or the debugger.

Specifications Electrical

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, V _{CC} =5.0V	nord neits	0.5A	1.0A

Mechanical

Measures:	45" (11	3cm) by	6.5"	(16 5cm	۱

Height: 0.5" (1.3cm) Weight: 6.5oz (184g)

Connectors

P1:	136-pin STD 32 Bus card edge
	connector on 0.0625" (0.16cm)

spacing

J1, J2: 40-pin latching four channel RS-232

serial I/O

J3: 10-pin latching interrupt

J4: 10-pin latching 8-bit parallel I/O

J5: 3-pin V53 RS-232 serial I/O

J6: 2-pin latching A/C interrupt

J7: 10-pin latching two channel RS-422/ 485 serial I/O

J8: 2-position power connector (ZT 89132 only)

STD 32 Compliance

· Memory Slave: SAI6, SA8-I, IXL

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz)



Environmental				
Operating Temperature	0° to +70° Celsius			
Storage Temperature	-40° to +85° Celsius			
Non-Condensing Relative Humidity	less than 95% at 40° Celsius			

Reliability

• MTBF: 28 years

• MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8932 Intelligent, Multi-Channel

Serial Controller

ZT M8932 ZT 8932 manual

ZT 8932-ISC-DR1 Intelligent, Multi-Channel

Serial Controller with on-board executive and installable device drivers for DOS. Includes 256 Kbytes of Boot Block flash memory and

256 Kbytes of RAM.

ZT 8932-ISC-DRx Support for other operating environments. Contact Ziatech

for more information.

Ordering example for OEM applications: A ZT 8932 Intelligent, Multi-Channel Serial Controller with 256 Kbytes of flash memory, 256 Kbytes of static RAM, and boot loader and flash reprogrammer installed is ordered as: ZT 8932-P1R1S1.

Must choose one option from each category: Flash Options

P1 256 Kbytes flash (boot block), 150ns

RAM Options

R1 256 Kbytes static RAM, 100ns

R2 256 Kbytes static RAM, 55ns

R3 1 Mbyte static RAM, 120ns

R4 1 Mbyte static RAM, 55ns

(option R4 cannot be battery backed)

Software Options

S1 Boot loader, and flash reprogrammer installed

Development Software

ZT 94031 STD

STD ROM Development Environment; STD ROM development system for PROM-based target systems. Includes Virtual Terminal Interface (VTI) installed on PROM, Paradigm LOCATE and startup modules, STD DDP, Paradigm DEBUG/RT, one serial cable, and a PLCC extractor tool.

Accessories

Cables (see Data Book cable section for details):

ZT 90069 39" (1m), 3-pin to 25-pin female

D-shell

ZT 90182 10" (25cm), 40-pin to four 9-pin

male D-shells

ZT 90183 10" (25cm), 40-pin to four 10-pin

headers

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.

STD 32 is a registered trademark of Ziatech Corporation. Star Gate is a trademark of Star Gate Technologies, Inc.



STD Bus Network I/O

8

STD Bus Network I/O Product Feature Guide

Product	Bus Data Width (bits)	Buffer Size	Maximum Data Rate	Transmission Type	Media	Indicator Lights
ZT 8895 STD Bus Ethernet Interface	8	2K	10 Mbps	CSMA/CD (Probabilistic)	Coax and AUI interface	•
ZT 89CT90 ARCNET Interface for STD Bus Computers	8/16 [•]	2K	2.5 Mbps	Token-passing (Deterministic)	Coax (Fiber-optic and twisted-pair optional)	٠
ZT 89CT93 STDIM™ for GE Fanuc Genius™ I/O	8	16K	153.6K	Token (Deterministic)	Twisted-pair	•

[◆] Feature included or available ● Requires an STD 32 backplane for data transfers greater than 8 bits.

STO32°

ZT 88CT93

STDIM™ for GE Fanuc Genius™ I/O

STD Interface Module (STDIM™) for GE Fanuc Genius™ I/O provides network support for STD 32® and STD-80 Bus computers

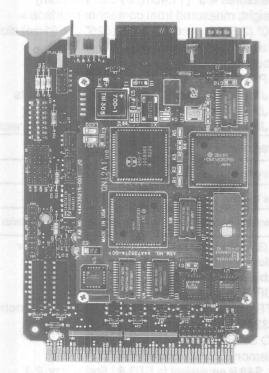
The ZT 88CT93 STD Interface Module (STDIM™) allows STD 32- and STD Bus-based industrial computers to communicate with GE Fanuc PLCs, industrial computers, MicroVAXes, and IBM-compatible PCs via the GE Fanuc Genius™ I/O bus. The interface and the Genius I/O bus also allow STD computers to control remote I/O.

GE Fanuc's Genius Network is a powerful and reliable remote I/O system that allows I/O blocks to be placed at the point of control. The new ZT 88CT93 interface, with its on-board Micro Genius Network I/O Interface (microGENI), gives STD systems access to all of the I/O communications functions supported by this network. These functions include the ability to

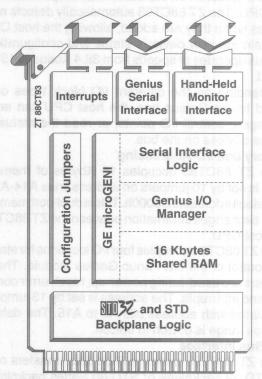
configure devices, access diagnostic information, read and write I/O points, and exchange messages with other computers or PLCs.

The Genius I/O bus can extend up to 4,500 feet while connecting up to 32 devices, and up to 7,500 feet while connecting up to 16 devices. Data communication rates range from 38.4 to 153.6 Kbits per second.

Ziatech SDTIM is software compatible with GE Fanuc's Genius I/O PCIM (PC Interface Module), the interface between the IBM PC and Genius I/O Products. This allows GE Fanuc's software libraries to be used to develop applications quickly. The STDIM can also be used with standard software applications that can communicate with a PCIM.



- STD 32- and STD-compatible (5 and 8 MHz)
- Software-compatible with GE Fanuc Genius I/O IBM PC Interface Module (PCIM)
- GE Fanuc Genius-compatible 38.4 to 153.6 Kbaud data transfer rates
- Supports up to 32 devices
- Supports I/O monitoring, control and data acquisition



- Interfaces to entire family of Genius I/O products
- 20- or 24-bit memory addressing
- Status LEDs: card select, Genius OK, Genius Comm OK
- · Polled or interrupt operation
- -40° to +85° Celsius operation (See GE Fanuc Genius specifications for deviations)

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40 $^{\circ}$ to +85 $^{\circ}$ C. (Users should make adjustments for temperature rise in enclosures.)



The Genius I/O bus is a standard network developed by GE Fanuc Automation. This network supports up to 32 CPU or I/O devices over 4,500 feet and 16 devices over 7,500 feet.

GE Fanuc Genius Network Interface

The ZT 88CT93 incorporates the Micro Genius Network Interface (microGENI) on board. The microGENI is a compact version of the GENI board used on the GE Personal Computer Interface Module (PCIM), and makes the ZT 88CT93 fully software compatible with the GE PCIM. The MicroGENI module has complete control of the Genius bus and makes it unnecessary for the host STD 32 CPU to manage the network.

Genius Network Communication

A host STD 32 CPU can control access to the Genius bus through the ZT 88CT93. The ZT 88CT93 automatically controls the serial interface independent of the STD 32 CPU. Information is passed to and from the host CPU and the ZT 88CT93 via 16 Kbytes of shared RAM. If a device does not respond for three consecutive scans, the ZT 88CT93 automatically logs the device in question off the network and reports it to the host CPU. The ZT 88CT93 automatically detects new devices when they are added, allowing the host CPU to obtain the new device's status and configuration. The bus operates at speeds from 38.4 Kbaud to 153.6 Kbaud.

Depending on the different I/O block types connected to the Genius bus, the host CPU can send messages, control I/O points, or read the status of various devices on the bus.

Memory and I/O Addressing

The ZT 88CT93 occupies 16 Kbytes of memory which is set by 10 jumpers on address lines A14-A23. The default address is D0000h. This is dual-port memory which exchanges information between the ZT 88CT93 and host CPU.

The ZT 88CT93 occupies four I/O locations for status and control of the GE Fanuc Genius Module. These registers are used during power-up, reset, error conditions and interrupts. The address is set by 13 jumpers associated with address bits A2 to A15. The default address range is 03E0h to 03E3h.

STD Bus Interface

The ZT 88CT93 performs 8-bit data transfers over the STD 32 backplane or STD-80 Series backplane. The ZT 89CT93 decodes all 16 I/O address bits for I/O decoding and all 24 address bits for memory addressing. The ZT 88CT93 supports the six backplane and five frontplane interrupts.

Software

The ZT 88CT93 is software-compatible with the PCIM, GE Fanuc's Genius I/O IBM PC Interface Module. Any code developed on this platform easily transfers to the STD platform.

The software drivers used for control and communications with the STDIM are identical to GE's PCIM drivers. A complete set of manuals and software are available directly from GE Fanuc or may be purchased through Ziatech.

Specifications

Electrical

- GE Genius[™] I/O System-compatible
- Size- and backplane-compatible with STD 32 and STD Bus specifications

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc=5.0V	350mA	450mA	600mA

Serial Network

Data Rate (K bits/sec.)	153.6 Standard	153.6 Extended	76.8	38.4
Max Bus Cable Length (ft.)	2,000	3,500	4,500	7,500
Max. # of Devices per Bus	32	32	32	16

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 specifications
- Measures 4.5" (11.4cm) by 6.5" (16.5cm)
- Height: measured from component surface = 1.0" (2.5cm); occupies two 0.625" (1.581cm) slots
- Weight: 0.458lbs (207.7g)
- Connectors

P1: STD 32 and STD Bus connector

J1: 10-pin connector, frontplane interrupts

J2: 6-pin, 5mm, PLC interface connector

J3: 9-pin D-shell, hand-held monitor connector

Environmental *				
Operating Temperature	-40° to +85° Celsius			
Storage Temperature	-55° to +105° Celsius			
Non-Condensing Relative Humidity	10% to 90% at 40° Celsius			

^{*} See GE Fanuc Genius I/O Interface Specification for deviations

Reliability

MTBF: 30 years (excluding microGENI)

MTTR: five minutes (based on board replacement)

STD 32 Compliance Level

I/O Slave: SA8-I, ICA, IXP, IXL

Memory Slave: SA8-I, ICA, IXP, IXL

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz)

Ordering Information

STDIM™ for GE Fanuc Genius™ I/O ZT 88CT93 ZT M88CT93 STDIM™ for GE Fanuc Genius™ I/O manual

IC641GBE647 Programming software and manuals for STDIM

(See GE Genius I/O Module Specification for a list of cables)





ZT 8895

STD Bus Ethernet Interface

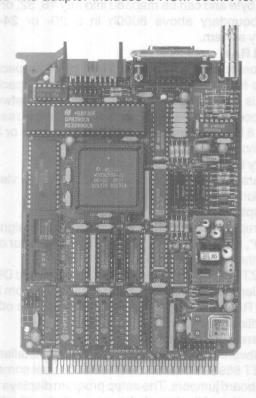
High-performance STD Ethernet interface is compatible with Thick and Thin Ethernet™ and IEEE 802.3 standards

The ZT 8895 STD Bus Ethernet Interface board allows STD 32® and STD Bus computers to communicate over the Ethernet network protocol. Both Thin Ethernet (Cheapernet, 10 BASE 2), twisted-pair (10 BASE T), and Thick Ethernet (10 BASE 5) are supported on one versatile board.

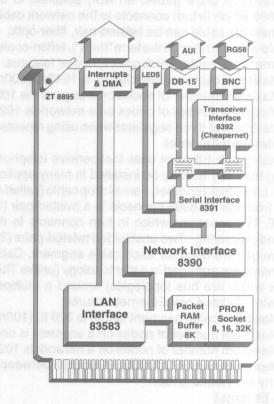
The ZT 8895 conforms to the IEEE 802.3 and Ethernet standards for a 10 Mbps Carrier Sense Multiple Access/Collision Detection (CSMA/CD) local area network. The adapter includes a ROM socket for BIOS

extensions, and software drivers for the following: Novell's NetWare®, DEC's DECnet-DOS, Sun's NFS, 3Com's 3+, NetBIOS, and UNIX® Streams. Software support is also available for TCP/IP protocol.

The ZT 8895 can be used in STD systems to implement remote data acquisition units, cell controllers, or file server communications for diskless systems, or for simple data communications in a DOS or non-DOS STD system.



- STD 32- and STD-compatible
- Supports true 16-bit I/O addressing
- · Supports 20- or 24-bit memory addressing
- Software is compatible with Western Digital WD 8003EB EtherCard PLUS PC Ethernet Interface
- Supports 10 BASE 5 (Thick Ethernet)
 IEEE 802.3, 10 BASE 2 (Thin Ethernet),
 10 BASE T (twisted-pair), and Ethernet (pre-IEEE 802.3) interfaces



- Dual-port RAM interface for fast buffer accesses
- EEPROM stores system configurations
- Software packages available for TCP/IP support
- Transmit and receive activity LEDs
- Software-compatible with Western Digital's 8003
 EB Ethernet adapter
- · Low power CMOS design



Network Interface

The network interface is implemented by the National Semiconductor DP8390C Network Interface Controller (NIC). It provides the media access control as defined by Ethernet and IEEE 802.3 standards. Although the terms Ethernet and IEEE 802.3 are sometimes interchanged, they are not identical. The IEEE standard, developed years after the introduction of Ethernet by Xerox Corporation, has some variations from the earlier implementations. The ZT 8895 can be jumper configured to support both Ethernet versions 1 and 2 (pre-IEEE 802.3) as well as IEEE 802.3.

Thick Ethernet

Thick Ethernet, often referred to as simply "Ethernet," differs from Thin Ethernet in the type of cable used to connect network nodes. Thick Ethernet systems use a small drop cable (called an AUI) attached to the ZT 8895 which in turn connects to the network cable. The network cable can be twisted-pair, fiber-optic, or double-shielded (hence the term "thick"), teflon-coated Ethernet coax cable. Thick coax Ethernet features:

- Maximum cable segment length is 1640 ft. (500m)
- Maximum number of nodes on a segment is 100
- Maximum number of nodes on a network is 1024
- Maximum of three segments when using repeaters

Twisted-pair Ethernet

Twisted-pair Ethernet uses inexpensive telephone wiring that may already be installed in many applications. Like Thick Ethernet, a small drop cable (called an AUI) from the ZT 8895 connects to a twisted-pair (10 BASE T) transceiver which in turn connects to the twisted-pair wiring. Two unshielded twisted-pairs (22-26 gauge) are used for each cable segment. Cable segments are arranged in a star topology (unlike Thin/Thick which are bus topologies) around a multiport repeater. Twisted-pair Ethernet features:

- Maximum cable segment length is 320 ft. (100m)
- · Maximum number of nodes on a segment is one
- Maximum number of nodes on a network is 1024
- Maximum number of multiport repeats between any two nodes is four

Thin Ethernet

The ZT 8895 also contains a thin Ethernet interface that uses the small and more flexible coax cable. This cable is connected directly to each ZT 8895 via a BNC "T" connector resulting in a lower cost system. Thin Ethernet features:

- Maximum cable segment length is 600 ft. (185m)
- Maximum number of nodes on a segment is 30
- Maximum number of nodes on a network is 1024
- Maximum of five segments when using repeaters
- Extended length segments are also supported

I/O Addressing

The ZT 8895 decodes all 16 bits for its I/O address. Eight bits of the I/O address are stored in software-configurable EEPROM, with the remaining three bits

being jumper-selectable along with IOEXP on any 32 byte boundary within the 64 Kbyte I/O address space. As shipped, the ZT 8895 requires 32 bytes of I/O at 0280-029Fh.

Memory Addressing

The ZT 8895 decodes either 20 or 24 memory address bits for its on-board PROM socket and packet RAM buffer. For 20-bit memory addresses, six of the upper memory address bits (A18-13) are stored in software-configurable EEPROM, with the upper address bit (A19) required to be a one. For 24-bit memory addressing, the upper four bits (A20-23), along with MEMEX, are jumper-selectable, and the remaining bits are decoded just like 20-bit systems.

PROM Socket

A PROM socket is provided for vendor-specific BIOS extensions for diskless workstations or for custom software. The PROM size is configurable for 16, 32, or 64 Kbyte and can be mapped into any 16, 32, or 64 Kbyte boundary above 8000h in a 20- or 24-bit memory system.

Packet RAM

The on-board 8 Kbyte static RAM provides packet storage for receive and transmit buffers. The packet buffer is dual-ported, allowing interleaved network and processor accesses. The packet buffer can reside on any 8 Kbyte boundary above 8000H in a 20- or 24-bit memory system.

Activity LEDs

Separate transmit and receive LEDs provide visual indication of network activity.

Interrupts and DMA

Interrupts can be output on the backplane signals INTRQ*, INTRQ1*, INTRQ2* (CNTL), or IRQx, or output on the frontplane connector.

The ZT 8895 is DMA-compatible. An off-board DMA controller can be used to transfer data to and from the packet RAM, allowing the processor to perform other time-critical processing functions.

Software Configuration

A software setup program simplifies the installation of the ZT 8895 and eliminates the need to set some of the on-board jumpers. The setup program displays the configuration of the board, detects conflicts with other boards in the system, and allows the I/O address and memory address.

Software Drivers

Ziatech includes Western Digital software drivers for Novell's NetWare, 3Com's 3+, DEC's DECnet-DOS, Sun's NFS, and UNIX with each ZT 8895 shipped under license agreement with Western Digital. TCP/IP software is available from FTP Software including remote log-in, file transfer, electronic mail and other functions. A NetBIOS emulator is also included. When used in DOS systems, the ZT 8895 is the software equivalent of the Western Digital 8003 EB PC Bus adapter.

8

Specifications

Compatibility

- Compatible with Ethernet versions 1 and 2
- Compatible with Thick Ethernet (IEEE 802.3, 10 BASE 5)
- Compatible with Thin Ethernet (IEEE 802.3, 10 BASE 2)
- Compatible with twisted-pair (IEEE 802.3, 10 BASE T)

Electrical

- · Data Rate: 1 Mbit per second
- Power Requirements for Thick Ethernet

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, V _{CC} = 5V		420mA	700mA
Aux Voltage, V _{aux+} = 12V	11.4V	12.0V	12.6V
Aux Current, V _{aux+} = 12V	-	320mA	500mA

• Power Requirements for Thin Ethernet

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	-	840mA	1200mA

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 mechanical specifications
- Occupies one STD slot (0.625" [1.6026cm] spacing)
- Connectors

J1: BNC Thin Ethernet connector

J2: 15-pin latching "D" connector for

Ethernet AUI transceivers

J3: 20-pin latching header for interrupts

and DMA

Environmental		
Operating Temperature	0° to 70° Celsius	
Storage Temperature	-40° to +85° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

STD 32 Compliance

- I/O Slave: SA8-SDMA8, I, IXP, IXL
- Memory Slave: SA8
 Note: SA8 is equivalent to STD-80 Series Rev. 2.3
 (5 and 8 MHz).

Reliability

- MTBF: 25 years
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8895 STD Ethernet Interface, driver software ZT M8895 STD Ethernet Interface manual

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for some products. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.

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- · Compatible with Thin Ethemet (IEEE 80
 - (S BASE 2)
 - Compatible with twisted-pair (IEEE 802.3.)

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 - Ethernet AUI transceivers
- and DMA.



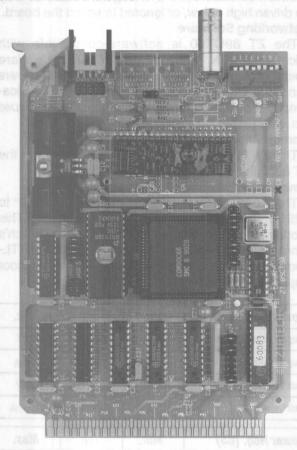
ZT 89CT90

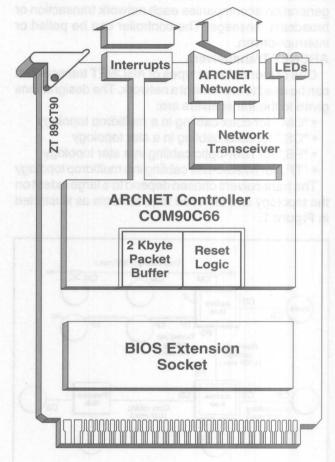
ARCNET Interface for STD Bus Computers

16-bit ARCNET® Interface gives STD Bus computers local area network capability

The ZT 89CT90 is an STD Bus ARCNET interface providing high-performance Local Area Network (LAN) capability for token-bus networks. A complete controller, the ZT 89CT90 features an on-board 2 Kbyte packet buffer, an eight-position DIP switch for setting the node address, hardware or software reset, and a 12 Kbyte PROM socket for BIOS extensions or other code. The on-board packet buffer supports 8-bit STD-80 or 16-bit STD 32® data transfers.

ARCNET can support 255 nodes at 2.5 Mbps operation for distances of up to four miles. It supports several network media and network topologies, including star or multidrop configurations. Coax cable (RG 62AU 93 ohm) can be used in both star and multidrop configurations, while fiber-optic cable is used only in star configurations. Twisted-pair is available for multidrop configurations.





- STD 32- and STD-compatible
- ARCNET Local Area Network-compatible
- Token bus protocol
- Compatible with Novell's NetWare® and Microsoft's LAN Manager
- 2 Kbyte packet buffer, 12 Kbyte BIOS extension
- Baseband operation using low-cost RG 62 coax
- Optional fiber-optic or twisted-pair operation
- 8- or 16-bit I/O port addressing
- · 20- or 24-bit memory addressing
- 8- or 16-bit data operation
- Diagnostic LEDs
- Polled or interrupt operation

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40 $^{\circ}$ to +85 $^{\circ}$ C. (Users should make adjustments for temperature rise in enclosures.)



Functional Considerations ARCNET Overview

Originally developed as a high-performance LAN, ARCNET employs a token-passing protocol at speeds of 2.5 Mbits per second. Because it is a token-bus protocol, each node's response time can be pre-determined, making ARCNET well suited for industrial automation applications that require a deterministic network.

ARCNET Controller

The ZT 89CT90 employs an I/O- and memory-mapped controller (Standard Microsystems' COM 90C66) to provide complete ARCNET capability while providing transparent network operation and control. Self-reconfiguring nodes can be added or deleted from the network and a 16-bit CRC check/generation accompanies each network transaction or broadcast message. The controller can be polled or interrupt-driven.

ARCNET Transceivers

One of four different types of ARCNET transceivers can be used to implement a network. The designations given to the transceivers are:

- · "CM," for coax cabling in a multidrop topology
- "CS," for coax cabling in a star topology
- "FS," for fiber-optic cabling in a star topology
- "TP," for twisted-pair cabling in a multidrop topology
 The transceivers chosen depend to a large extent on
 the topology and distance requirements as illustrated
 in Figure 1.

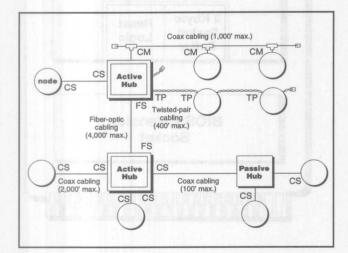


Figure 1. The ARCNET standard uses many topologies

Interrupts

The ZT 89CT90 can operate in either polled or interrupt mode. Backplane interrupts INTRQ*, INTRQ1*, and INTRQ2* are jumper selectable, IRQx is also supported for STD 32 users. Five frontplane interrupts are available via jumpers to a 10-pin latching header.

Memory Addressing

The ZT 89CT90 has an on-board 2 Kbyte packet buffer which holds up to four data packets for transmit and receive functions. The packet buffer is memory mapped into the STD Bus address space. A 12 Kbyte BIOS extension PROM socket is included on-board for use in DOS or non-DOS environments. The base address of the PROM and data packet buffer is switch-selectable, and either 20- or 24-bit addressing can be selected.

I/O Addressing

Sixteen I/O ports are decoded by the ZT 89CT90 from either 8- or 16-bit STD I/O addresses. Eight of these ports decode the COM 90C66, while the remaining eight are used to implement a software reset to the ZT 89CT90. The COM 90C66 I/O base address is switch-selectable in 8-byte segments. IOEXP may be driven high or low, or ignored to select the board.

Networking Software

The ZT 89CT90 is software-compatible with Microsoft's LAN Manager and Novell's NetWare operating systems. As an alternative, simple drivers can be written to support peer-to-peer communications. Please refer to the application note Ziatechniques No. 6 for further details.

Compatibility

The ZT 89CT90 is backward-compatible with the ZT 8890 that it replaces.

Low Power/Extended Temperature

The ZT 89CT90 is designed and tested for -40° to +85° Celsius operation in harsh environments. This product is designed for use in conjunction with Ziatech's other LT (low temperature) and CT (CMOS, TTL-backplane-compatible) products for mobile and outdoor applications.

Power Req. (CM)	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, V _{CC} = 5.0V	11	180mA	380mA
Aux Voltage, V _{aux+}	11.4V	12.0V	12.6V
Aux Current, V _{aux+} = 12.0V		55mA	130mA
Power Req. (CS)	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	liscono et	140mA	300mA
Aux Voltage, V _{aux+}	11.4V	12.0V	12.6V
Aux Current, V _{aux+} = 12.0V	eMelleve	15mA	40mA
Power Ren (FC)	Min	Tun	May

Power Req. (FS)	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V		130mA	280mA

Power Req. (TP)	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	-	165mA	350mA
Aux Voltage, Vaux+	11.4V	12.0V	12.6V
Aux Current, V _{aux+} = 12.0V	-	50mA	120mA

Specifications

Electrical

ARCNET-compatible

• Data Rate: 2.5 Mbits per second maximum

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 mechanical specifications
- Occupies one STD slot (0.625" [1.59cm])
- Connectors

CM, CS: J1 is a right angle female BNC

connector. J2 is not installed.

FS: J1 is an SMA compatible fiber-optic

receiver. J2 is an SMA-compatible

fiber-optic transmitter.

TP: J1 and RJ-11 are phone connectors.

All boards: J3 is a 10-pin right angle,

dual-row male header for frontplane interrupt routing.

Environmental	
Operating Temperature	-40° to +85° Celsius
Storage Temperature	-55° to +105° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

STD 32 Compliance

• I/O Slave:

SA16, SA8-I, IXP

· Memory Slave: SA16, SA8-I, IXP

Note: SA8 is equivalent to STD Series-80 Rev. 2.3

(5 and 8 MHz)

Reliability

· MTBF: 35 years

MTTR: five minutes (based on board replacement)

Ordering Information

An ARCNET interface for STD Bus computers with a coax-multidrop transceiver and BIOS software is ordered as: ZT 89CT90-D1S.

ZT 89CT90

ARCNET interface for STD Bus

computers

ZT M89CT90

ZT 89CT90 manual

Must choose one driver from below Driver Options

D1 Coax-multidrop transceiver
D2 Coax-star transceiver
D3 Fiber-optic star transceiver
D4 Twisted-pair transceiver

Software Options

S BIOS for STD ARCNET Interface

Accessories:

ZT 91004 ZT 91005 Coax BNC tee junction 93 ohm terminator pair for

multidrop configuration

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.



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- Data Rate: 2.5 Mous per second maximum

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- Size- and backplane-compatible with STD 32 and STD-00 mechanical specifications
 - Occupies are STD stot (0.625" [1,50cm])
 - * Connactors
- CM, 6 s .11 is a nont single female BND.
- S: Ut is an SMA compatible liber-optic
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- All boards: J3 is a 10-pin right angle, dust-row male header for

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An ARONE I interface for STD Bus computers with a pax-multidice transceiver and BIOS software is interest as: ZT 88GT90-D18.

ARCNET Injertace for STD But

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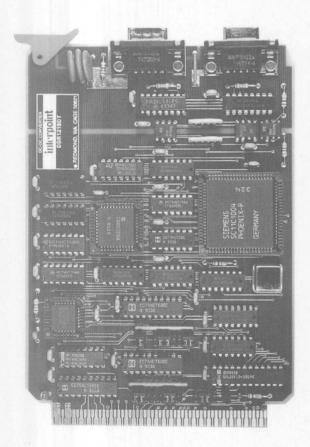
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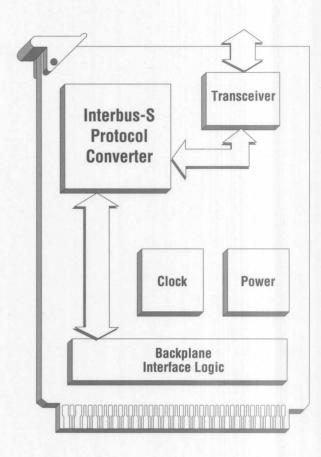


E9002

Interbus-S Interface

Interface connects STD 32 and STD computers to Phoenix Contact's Interbus-S open standard, high-speed, distributed I/O system





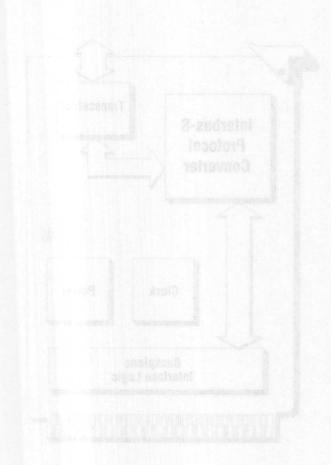
- Fully compatible with the Interbus-S 2-twistedpair (2-TP) network
- · Master or slave mode operation
- · Electrical isolation between STD backplane and Interbus-S network
- 16 or 32 bits of input and output in slave mode
- Controls up to 4096 I/O points in master mode
- Fully compatible with Interbus-S Peripherals Communication Protocol (PCP) in both master and slave mode
- Communication drivers available for C, BASIC and Assembler
- Interbus-S connection via dual 9-pin D connectors
- STD 32® Compliance: I/O Slave: SA-8, I, IXL
- Occupies only 16 STD I/O addresses, provides 8-,10-, or 16-bit I/O addressing
- Requires 700ma of +5V from STD backplane





S 108 3U





Fully competible with the Interbus-5 2-twistedneit (2-TP) network

Master or stave mode operation
 Electrical solution between STD backplane and

Costrols up to 4036 I/O points in master mode

Communication Protocol (PCP) in both master

STD Bus Digital I/O

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mination Assembly
O Cable Adapter
I/O Mounting Rack

9

STD Bus Digital I/O Product Feature Guide

Product	STD 32 STD-80 (MHz)	STD- 8085 (MHz)	STD- Z80 (MHz)	# of Lines	Input	Output	Event Sensing Lines	Vectored Interrupts	Max. Input Current	-40° to +85° C
ZT 8845 ZT 88CT45 48-Point Digital I/O Interface	5/8	3/5	2.5/4/6	48	*	•	4	1	45mA	+
ZT 8846 ZT 88CT46 Real-Time Event Sense Interface	5/8			24	•		48	48		+
ZT 88CT49A Optically Isolated Digital Input Interface	5/8		2.5/4/6	48	٠		4	1	18mA	•
ZT 88CT62 Optically Isolated Input and Counter/ Timer Interface	5/8			24 and 3 counter/ timers	*		1	1	127mA	+
ZT 88CT72 144-Point Digital I/O Interface	5/8	3/5	2.5/4	144	*	•	_	_	12mA	•
ZT 88CT73 Optically Isolated Industrial I/O Interface	5/8			16	٠	•	8	1	335mA	٠
ZT 89CT61 96-Point Digital I/O Interface	5/8			96	٠	•	16	1	12mA	+

Note: Additional digital I/O products can be found in the Personal Computer I/O and SBX Expansion Module sections of this data book.

Also Inside This Section

- ZT 2223 Industrial I/O Adapter Board
- ZT 2224 24-Line Termination Assembly
- ZT 2225 Industrial I/O Cable Adapter
- ZT 2226 24-Channel I/O Mounting Rack

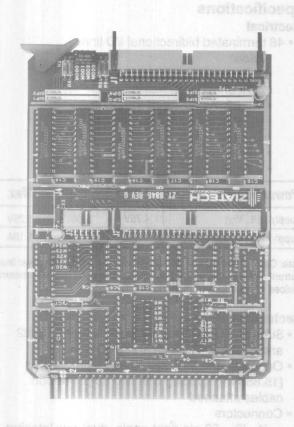
ZT 8845

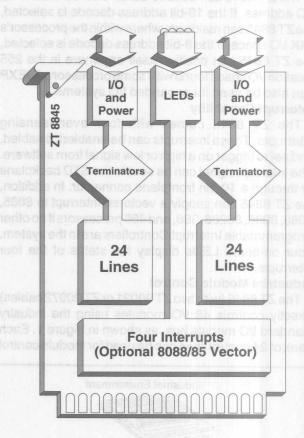
48-Point Digital I/O Interface

Parallel interface with 48 bidirectional lines for industrial and general purpose digital I/O

The ZT 8845 is a high-current, bidirectional interface providing 48 digital lines for STD Bus computers. These lines connect STD computers to instruments, peripherals, and industry standard signal conditioning modules such as those manufactured by Opto 22, Gordos, Crydom, Grayhill, Potter & Brumfield, etc. The ZT 8845 interfaces directly to two industry standard 24-channel I/O module mounting racks.

Interrupts are included through four event-sensing inputs, with vectoring capability provided for most processors. An interrupt can also be generated over the front or backplane. Interrupts are generated on high or low signals and can be individually enabled or disabled with software.





- STD 32®- and STD-compatible
- Processor-independent
- 8- or 16-bit I/O addressing
- 48 bidirectional digital I/O signals with termination
- 45mA sink current at V_{OL} of 0.5V
- Compatible with Opto 22, Gordos, Ziatech, and other popular industrial I/O module racks
- Four event-sensing inputs with LED status indicators
- Vectored interrupts for Intel x86 Series processors
- Optional cables for connection to I/O module mounting racks
- Two independent +5V at 1A fused power lines on I/O connectors
- Software support through device driver software (STD DDP)
- Burned-in at 55° C and tested to guarantee reliability



TTL Interface - General

The ZT 8845 has 48 bidirectional I/O lines configured as two banks of 24 lines each. Each data line has its own ground and can be configured as input, output, or output with readback. The I/O lines can be accessed through two standard 0.1" (2.54mm) spaced latching 50-pin connectors.

Terminated TTL Lines

The ZT 8845 is shipped with 4.5k ohm termination resistance and 45mA of sink current on each data line. To reduce signal reflection, the ZT 8845 is designed to accept a pullup/pulldown termination in place of the 4.5k ohm resistors.

I/O Addressing

The ZT 8845 can decode either 8 or 16 bits for its I/O address. If the 16-bit address decode is selected, the ZT 8845 can reside anywhere within the processor's 64K I/O space. If the 8-bit address decode is selected, the ZT 8845 can position itself anywhere in the 255 location I/O space found with some processors. IOEXP can also be used for expanded I/O systems.

Interrupt Capability

The ZT 8845 comes with four event-sensing interrupts. These interrupts can be enabled, disabled, and set to trigger on a high or low signal from software. The interrupt signal can be sent to the STD backplane or through a 10-pin frontplane connector. In addition, the ZT 8845 can supply a vectored interrupt to 8085, 8088, 8086, 80286, 386, and 486 processors if no other Programmable Interrupt Controllers are in the system. Four on-board LEDs display the status of the four interrupts.

Industrial Module Control

The ZT 8845 (with two ZT 90021 or ZT 90072 cables) directly controls 48 I/O modules using the industry standard I/O module bus, as shown in Figure 1. Each bank of 24 control lines can be used for module control

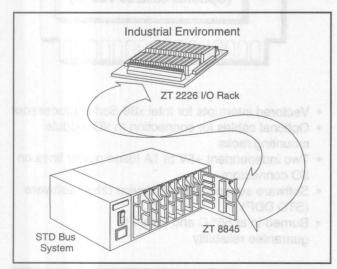


Figure 1. The ZT 8845 connects STD 32 and STD Bus systems to various industrial environments

or interrogation. Each bank also has its own fused, 1A 5V logic supply for the modules. These industrial modules control machinery in automation applications.

Power Available for User

There are two 1A 5V fused power lines available on each connector. Space is also provided for a user-mounted terminal that can be used for custom applications. This terminal strip allows access to +5V and ground with the turn of a screwdriver.

Software

The ZT 8845 manual includes several examples of software routines used to drive the ZT 8845. An application note is also included to explain the use of the industrial I/O racks. For software support, a linkable device driver for the ZT 8845 is provided in STD DDP, Ziatech's device driver package.

Specifications

Electrical

- 48 terminated bidirectional I/O lines Output:
 - Inverting open collector operation
 - · 4.7k ohm pullup resistor
 - V_{OH}=2.0V minimum at -12.0mA
 - V_{OL}=0.5V maximum at 45.0mA Input:
 - Inverting buffers
 - 4.7k ohm pullup resistor

Power Req.	Min.	Тур.	Max.
Supply Volt., Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V		0.60A	1.10A

Note: Current given does not include two fused 1A logic power lines. Currents measured during quiescent operation will vary with external devices attached

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 mechanical specifications
- Occupies one STD slot (0.625 inch [15.88mm]) spacing with two 50-pin ribbon cables attached
- Connectors
 - J1, J2: 50-pin right-angle, dual-row latching male header (0.10" [2.54mm] centers) for 50-pin ribbon cable. For general purpose I/O.
 - J3: 10-pin right-angle, dual-row latching male header (0.10" [2.54mm] centers) for 10-pin ribbon cable. For frontplane interrupt routing.

STD 32 Compliance

• I/O Slave: SA8-I

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz)

Environmental	
Operating Temperature	0° to 65° Celsius
Storage Temperature	-20° to +75° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

Reliability

- MTBF: 63 years
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8845 48-Point Digital I/O Interface

ZT M8845 48-Point Digital I/O Interface manual

Accessories

Cables (see Data Book cable section for details):

ZT 90021 10' (3m), 50-pin header to 50-pin

ZT 90028 40" (1m), for printer, 50-pin to 25-pin

ZT 90072 10' (3m), 50-pin both ends ZT 90137 2' (0.6m), 50-pin both ends

Boards (see separate data sheets for details):

ZT 2224 24-Line Termination Assembly ZT 2226 24-Channel I/O Mounting Rack

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for some products. Contact Ziatech for additional information.

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- MTTR; five naledtes (besed on board replacement)

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Cables (see Data Book cable section for details):
ZT 90021 10' (3m), 50-pin header to 50-pin.
ZT 90028 40' (1m), for printer, 50-pin to 25-pin.
ZT 90072 10' (3m), 50-pin both onds.
ZT 900127 21' (1 5m), 50-pin both ends.

Boards (see separate data sixeels for details):
ZT 2224 24-(Joe Terminétion Assembly
ZT 2226 24-Channel I/O Mounting Rack

All products are shipped FOB San Luis Obispo, CA, USA, OEM discounts are available for some products.



ZT 8846

Real-Time Event Sense Interface

STD Bus interface provides 24 event sense input lines for high-speed industrial applications

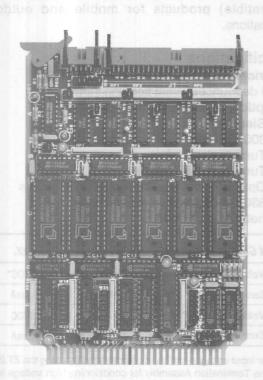
The ZT 8846 STD interface provides 24 highspeed digital event sensing inputs for real-time applications.

The ZT 8846 can be programmed to generate interrupts when an event occurs, such as a tripped switch on a material handling conveyor. Both positive and negative transitions can be detected on each input line, and a unique interrupt vector can be generated for each condition. Forty-eight unique interrupt vectors can be generated by the ZT 8846. These interrupts provide an efficient means of notifying an STD processor of real-time events without the burden of polling digital I/O points. This feature is ideal for

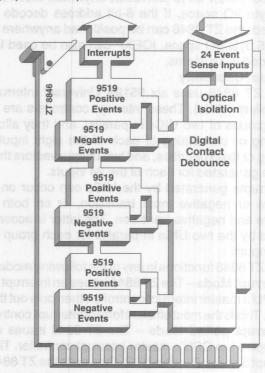
applications with large amounts of digital I/O because it keeps the CPU free until there is a change in status.

The event sense interface takes full advantage of the unique ability of the STD bus to support cascaded interrupt controllers. Six programmable interrupt controllers allow each of the 24 lines on the ZT 8846 to generate two unique interrupt vectors for the STD processor with a single hardware interrupt line.

The ZT 8846, which offers event sense capabilities to STD bus systems, is compatible with industry standard I/O modules such as Opto 22 and Gordos. The ZT 8846 is supported by Ziatech's device driver package (STD DDP).



- STD 32- and STD-compatible
- · 8- or 16-bit I/O addressing
- · 24 TTL input lines with debouncing
- Fully compatible with all popular industrial I/O mounting racks (e.g., Ziatech, Opto 22, and Gordos)
- Compatible with Ziatech's ZT 8845 TTL I/O card
- Software controllable vectored interrupts (9519A)
- Supports interrupt, interrupt-polled, and polled modes



- Forty-eight vectored interrupts for Intel x86
 Series processors
- Optional cables for connection to I/O module mounting racks
- Optical isolation of all input signals
- Software support through device driver package (STD DDP)
- ZT 88CT46 available for extended temperature operation (-40° to +85° C)

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40° to $+85^{\circ}$ C. (Users should make adjustments for temperature rise in enclosures.)



TTL Interface - General

The ZT 8846 has 24 input lines. Each data line has its own ground and can be configured to sense positive and/or negative event transitions. The I/O lines can be accessed through a standard 0.1" (2.5mm) spaced latching 50-pin connector.

Debounced TTL Inputs

The ZT 8846 comes with a digital contact bounce eliminator circuit for interfacing with mechanical contacts. The sample time for the bounce eliminators can be selected by changing the timing capacitors.

The "on" state input voltage is 5V. If higher voltages must be sensed, then the signal must be conditioned with external resistors in series. Signal conditioning is possible with the optional ZT 2224 24-Line Termination Assembly from Ziatech.

I/O Addressing

The ZT 8846 can decode either 8- or 16-bit addresses for its eight I/O ports. If the 16-bit address decode is selected, the ZT 8846 can reside anywhere within the 64 Kbyte I/O space. If the 8-bit address decode is selected, the ZT 8846 can be positioned anywhere in the 255 byte I/O space. IOEXP can also be used for expanded I/O systems.

Interrupt Capability

The ZT 8846 uses six 9519A Universal Interrupt Controllers (UICs). These interrupt controllers are in three groups of two UICs in parallel, and they allow masking or unmasking of each of the eight inputs, rotating or fixed priorities, and two unique vectors that can be generated for each of the 24 inputs.

Interrupts generated by the UICs can occur on a positive or negative input transition, or on both a positive and negative transition. The latter is accomplished by the two UICs in parallel for each group of eight inputs.

The ZT 8846 functions in any of the following modes: Interrupt Mode – The ZT 8846 issues an interrupt to the CPU's master interrupt controller, then puts out the vector. This is the most efficient form of interrupt control.

Interrupt-polled Mode – The ZT 8846 issues an interrupt to the CPU's master interrupt controller. The Interrupt Service Routine (ISR) then polls the ZT 8846 status registers to identify the interrupt that needs servicing. This mode is useful in a system that does not support the STD cascade signals, or in systems that require sharing of interrupt lines.

Polled Mode – The ZT 8846 does not issue interrupts; however, the CPU periodically polls the ZT 8846 status registers to determine if there are interrupt sources that need servicing. This mode is useful for non time-critical interrupt sources, for systems that lack a CPU master interrupt controller, or if the master interrupt controller inputs are unavailable.

Optical Isolation

The ZT 8846 provides 300Vrms isolation on all 24 inputs. This feature helps isolate STD Bus computers from electrally noisy environments.

Industrial Module Control

The ZT 8846 (with ZT 90072 cable) allows direct sensing of 24 input modules using the industry standard I/O module rack, from Ziatech, Opto 22, Gordos, etc. **Software**

The ZT 8846 manual includes several examples of software routines that drive the ZT 8846. An application note is also included to explain the use of the industrial I/O racks. For software support, Ziatech strongly recommends using the linkable device driver included in STD DDP (Ziatech's STD Device Driver Package).

Low Power/Extended Temperature

The ZT 88CT46 is designed and tested for -40° to +85° Celsius operation in harsh environments. This product is designed for use in conjunction with Ziatech's other LT (low temperature) and CT (CMOS, TTL-compatible) products for mobile and outdoor applications.

Specifications

Electrical

- 24 debounced event sensing input lines
 Optical Isolation Section (socketed
 Siemens ILQ2)
 - 300V spike protection; socketed
 - Turn-on delay: 3 µsec
 - Turn-off delay: 70 µsec
 - · Opto-isolators may be replaced by shunts
 - 330 ohm current limiting resistor network provided

Input Characteristics	Min.	Max.
Input Voltage "ON State" (VIN)	2.0VDC	6.9VDC*
Input Current "ON State" (IIN)	1.4mA	19.0mA
Input Voltage "OFF State" (VIN)	0.0	1.3VDC
Input Current "OFF State" (IIN)	0.0	0.2mA

^{*}Higher input voltages can be accommodated by using the ZT 2224 24-Line Termination Assembly for conditioning high voltage input signals. Current given for quiescent operation will vary with external devices attached.

Debounce Section (MC14490)

- Debounce delay: 3 msec in standard configuration
- Delay may be user configured by changing capacitor

Power Req.	Min.	Тур.	Max.	
Supply Voltage, VCC	4.75V	5.00V	5.25V	
Supply Current, Vcc = 5.0V	0.30A	0.60A	1.10A	

9

Mechanical

- Size- and backplane-compatible with the STD 32 and STD-80 mechanical specifications
- Occupies one STD slot (0.625" [15.88mm] spacing) with one 50-pin ribbon cable attached
- Connectors
 - J1: 50-pin right-angle, dual-row latching male header (0.100" [2.54mm] centers) for 50-pin ribbon cable for event sense inputs
 - 2: 10-pin right-angle, dual-row latching male header (0.100" [2.54mm] centers) for 10-pin ribbon cable for frontplane interrupt routing

Environmental		
Operating Temperature (ZT 8846)	0° to 65° Celsius	
Operating Temperature (ZT 88CT46)	-40° to +85° Celsius	
Storage Temperature	-55° to +105° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

STD 32 Compliance

• I/O Slave: SA8-I, ICA

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz).

Reliability (5 a

• MTBF: 45 years

MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8846 Real-Time Event Sense Interface ZT 88CT46 Real-Time Event Sense Interface, extended temperature

ZT M8846 ZT 8846 manual

Accessories

Cables (see Data Book Cable section for details):

ZT 90021 10' (3m) flat, 50-pin header to 50-pin

card edge

ZT 90063 8.25" (21cm) frontplane interrupt,

one 26-pin and four 10-pin

ZT 90072 10' (3m) flat, 50-pin both ends ZT 90137 2' (0.6m) flat, 50-pin both ends

Boards (see separate data sheets for details):

ZT 2224 24-Line Termination Assembly ZT 2226 24-Channel I/O Mounting Rack

All products are shipped FOB San Luis Obispo, CA, U.S.A. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.



Jachenical

- Size- and had optione compatible with the STD 32
 and STD an reaching and distinct
 - Occupies one STD sigt (0.625" [15.68mm].
 spacing) with one 50-pin ribbon cable attached
 - Cannecto -
- 11: 50-c n.righi-angle, dual-row latching male hender (0.100* [2.54mm] centers) for 50-pin robon cable for event sense
- 2: 10-pin right-angle, dual-row latering male hasder (0.100" [2,54mm] centers) ior 10-pin ribbon cable for frontplane internal routing

Environmental

STD 82 Complened

- NO Slave: SA8-I, ICA
- Note: SAB is equivalent to STD-80 Series Rev. 2.8 fr. acri 2 Meter

validelet

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professing information

- ZT 8846 Real-Time Event Sense Interface
- ZT 8807 40 Rest-Time Event Sense Internos.
 - extended temperature
 - Isunam 9486 TX 6488M TX

e shoepaga/

- Cables (see Data Book Cable section for details):
- ZF BOO2 1 10' (3m) flat, 50-pin neager to 50-pin

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 - inches morning ran-op page
 - 27 90972 10° (3m) hat, 50 pm both ends
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Boards (see separate data sheets for details):

- ZT 2224 24-Line Termination Assumbly
- ZT 2226 24 Channel I/O Mounling Rack
- All products are shipped FOB San Luis Obispo, CA, U.S.A. OEM discounts are available for quantity mirchaeas. Contact Ziatech for additional information.
- Warrany Five years with an optional five year exension. See the juli warranty statement in the Technical



ZT 88CT49A

Optically Isolated Digital Input Interface

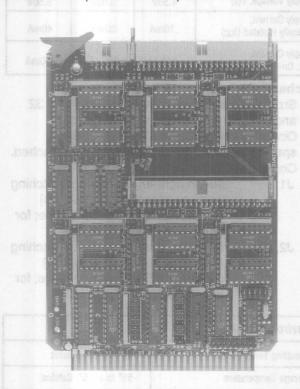
STD Bus digital interface with extended temperature features brings optical isolation and event sense capability to the factory floor

The ZT 88CT49A is a 48-input STD interface board that provides optical isolation from the harsh environment of the factory floor. CMOS technology allows the ZT 88CT49A to operate reliably in extreme temperatures. Its event sense capability also eliminates the time-consuming task of polling multiple input points.

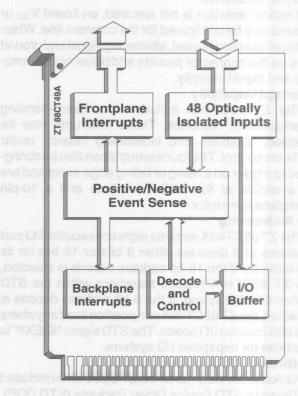
The optical isolation of the ZT 88CT49A provides an electrical barrier between the control system and data collection points located in a harsh environment. This isolates system electronics from conducted noise and high voltage levels. For non-standard voltage levels, an optional termination rack (ZT 2224) can be used to reduce the inputs to an acceptable level.

The ZT 88CT49A can be programmed to generate interrupts on four inputs when an event occurs, such as a tripped relay in the arc welding portion of an assembly line. This feature is well suited for applications that require large amounts of digital I/O because it keeps the CPU free until there is a change in status.

The ZT 88CT49A offers this event sense capability to STD $32^{\$}$ and STD systems. At the same time, it eliminates the need to externally protect control system inputs with expensive I/O modules such as Opto 22 or Gordos.



- STD 32- and STD-compatible
- Processor-independent
- · 48 optically isolated inputs
- · 320V input isolation voltage
- Extended temperature operation: -40° to +85° C
- · 8- or 16-bit I/O addressing
- · Four high/low event-sensing inputs



- Software-controllable interrupts
- Jumper-selectable path for backplane interrupts
- Optional cables for connection to other Ziatech
 I/O cards or external I/O module mounting rack
- Software support through device driver package (STD DDP)
- Burned in at 55° C and tested to guarantee reliability

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40 $^{\circ}$ to +85 $^{\circ}$ C. (Users should make adjustments for temperature rise in enclosures.)



I/O Interface

The ZT 88CT49A has 48 input lines configured as six banks of eight lines that are optically isolated from the control environment. Each bank has its own unique I/O address and may be read individually by software in polled or event-driven modes. The input lines are accessed through two standard latching 50-pin connectors (2 x 25 pins, 0.1" [2.54mm] pin-to-pin spacing). These inputs are software-compatible with Ziatech's ZT 8845 48-Point Digital I/O Interface.

Optical Isolation

The ZT 88CT49A supports 48 separately isolated input pairs. The ZT 88CT49A may be configured for common anode operation. The optional ZT 2224 24-Line Termination Assembly will support bussed, common, or isolated input configurations.

The optically isolated inputs will accept a voltage differential of 2.2 to 6.8VDC between the common line and the inputs to turn on the internal LED and phototransistor.

If optical isolation is not required, on-board V_{CC} or ground may be configured for the common line. When this configuration is used, alternating signal and ground pins on the connector provide additional noise immunity and signal integrity.

Interrupt Capability

The ZT 88CT49A includes four event-sensing interrupts with readback. These interrupts may be enabled, disabled, and individually cleared under software control. The four interrupts can also be configured to trigger on a rising or falling edge event and are all available at the STD backplane and a 10-pin frontplane connector.

I/O Addressing

The ZT 88CT49A requires eight consecutive I/O port locations and decodes either 8 bits or 16 bits for its I/O address. If the 16-bit address decode is selected, the ZT 88CT49A resides anywhere within the STD Series 64K I/O space. If the 8-bit address decode is selected, the ZT 88CT49A can position itself anywhere in a 255 location I/O space. The STD signal "IOEXP" is available for expanded I/O systems.

Software

A linkable device driver for the ZT 88CT49A is included in Ziatech's STD Device Driver Package (STD DDP), sold separately.

Specifications

Electrical

- · 48 optically isolated digital input lines
- · Inverting (negative true) operation
- · 320V optical isolation

T_{rise}: 20 μsec T_{fall}: 2 μsec

Input Characteristics	Min.	Max.
Input Voltage "ON State" (VIN)	2.2VDC	6.8VDC*
Input Current "ON State" (IIN)	2.0mA	18.4mA
Input Voltage "OFF State" (VIN)	0.0	1.4VDC
Input Current "OFF State" (IIN)	0.0	0.3mA

* Note: Higher input voltages can be accommodated by using the ZT 2224 24-Line Termination Assembly for conditioning high voltage input signals. Currents given for quiescent operation will vary with external devices attached.

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.50V	5.00V	5.50V
Supply Current, Optically Isolated (Icc)	10mA	30mA	40mA
Supply Current, Pos. On-board Source (Icc)	200mA	550mA	750mA

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 mechanical specifications.
- Occupies one STD slot (0.625" [15.88mm] spacing) with two 50-pin ribbon cables attached.
- Connectors

J1: 10-pin right-angle, dual-row latching male header (0.100" [2.54mm] centers) for 10-pin ribbon cable; for frontplane interrupt routing

J2, J3: 50-pin right-angle, dual-row latching male header (0.100" [2.54mm]

centers) for 50-pin ribbon cable; for general purpose digital I/O

Environmental		
Operating Temperature	-40° to +85° Celsius	
Storage Temperature	-55° to +105° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

9

STD 32 Compliance

• I/O Slave: SA8-I

Note: SA8 is equivalent to STD-80 Series Rev. 2.3

(5 and 8 MHz)

Reliability

• MTBF: 50 years

• MTTR: five minutes (based on board replacement)

Ordering Information

ZT 88CT49A Optically Isolated Digital Input Interface

Accessories

Cables (see Data Book cable section for details):

ZT 90021 10' (3.0m) 50-pin both ends. Two

cables maximum per ZT 88CT49A.

ZT 90063 8.25" (21cm) frontplane interrupt

cable, one 26-pin and four 10-pin. ZT 90072 10' (3.0m) 50-pin both ends. Two

cables maximum per ZT 88CT49A.

Boards (see separate data sheet for details): ZT 2224 24-Line Termination Assembly

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for most products. Contact Ziatech for additional information.



- I/O Stave: SAB-I

Note: SA3 is equivaler (5 and 3 MHz)

Heliability

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ZT 88CT 49A Optically isolated Digital

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cable, one 25-pin and four 10-pin. 21 90072 10' (3.0m) 50-pin beth ends, Two

Source (see replanted data sheet for details): ZT 2224 24-Line Termination Assembly

All products are shipped FOB San Lels Opispo, DA USA OEM discounts are available for most products Centre of Viete on the additional Information.

Mangary - Five years with an optional five-year extension. See the full warranty statement in the Technical Date Coolean confer



ZT 88CT62

Optically Isolated Input and Counter/Timer Interface

STD Bus interface with CMOS/extended temperature features brings optical isolation and event counting to the factory floor

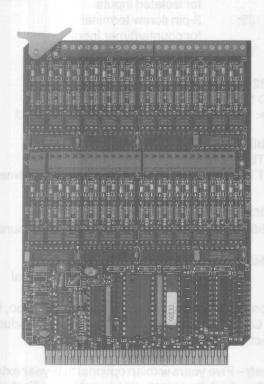
The ZT 88CT62 is a general purpose, 24-input, STD interface board that provides optical isolation from the electrical "noise" typically generated on the factory floor. CMOS technology allows the ZT 88CT62 to operate reliably in extreme temperatures.

The optical isolation of the ZT 88CT62 provides an electrical barrier between the control system and data collection points located in a harsh environment. This isolates system electronics from conducted noise and high voltage levels.

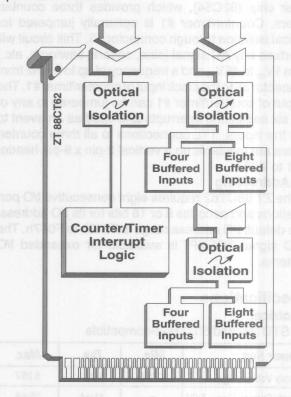
Each of the inputs on the ZT 88CT62 has a pair of screw terminals. One terminal is for the current/voltage source and the other is for the current return. The ZT 88CT62 also supports a wide input voltage range of up to 91V.

The ZT 88CT62 also includes an on-board optically isolated counter/timer. A pair of screw terminals allows an alternating signal (square, sine, sawtooth, etc.) with a range of $1V_{\rm pp}$ to $45V_{\rm pp}$ and a frequency of up to $2~\rm kHz$ to be amplified, isolated, and to drive the clock input of one of the counter/timers. The output of the counter/timer can be used to drive a backplane interrupt that signals the completion of a control process or assembly line.

The ZT 88CT62 offers these capabilities to all STD 32® and STD systems. At the same time, it eliminates the need to externally protect control system inputs with expensive I/O modules such as those offered by Opto 22 or Gordos.



- 24 individual optically isolated inputs
- On-board counter/timer (also optically isolated)
- Extended temperature operation (-40°C to +85°C)
- · 8-bit or 16-bit I/O addressing
- Software controllable counter/timer interrupts



- Jumper-selectable path for backplane interrupts
- STD 32- and STD-compatible
- Burned in at 55°C and tested to guarantee reliability
- Processor-independent

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of $\,^{-40^\circ}$ to $\,^{+85^\circ}$ C. (Users should make adjustments for temperature rise in enclosures.)



The ZT 88CT62 has 24 inputs configured as two banks of eight inputs and two banks of four inputs. Each bank has its own unique I/O address that can be read individually by software in polled or event-driven modes. The upper four bits of the banks with only four inputs will always return a zero.

Each of the 24 inputs has a dedicated pair of terminals, one for the current/voltage source, and the other for the current return path. The terminals accept wire of up to 16 AWG in diameter.

Optical Isolation

Optical isolation is achieved with low-current, high-gain photo transceivers. Inputs are preconditioned with a pair of Zener diodes and current limiting resistors. This allows each optically isolated input to accept a voltage differential of 15 to 91VDC across the input terminals to guarantee an "ON" state. Less than 5.0VDC guarantees an "OFF" state. For custom input characteristics, other Zener and resistive values can be substituted. Contact Ziatech for more information.

Counter/Timer

The ZT 88CT62 includes an on-board CMOS counter/timer chip (82C54), which provides three counter/timers. Counter/timer #1 is optionally jumpered for optical isolation through connector J5. This circuit will interface any AC signal (sine, square, sawtooth, etc.) from $1V_{\rm pp}$ to $45V_{\rm pp}$ and a frequency of up to 2 KHz from connector J5 to the clock input of counter/timer #1. The output of counter/timer #1 can be jumpered to any of the six backplane interrupts and used as an event to poll the inputs. TTL connections to all three counter/timers are available on a vertical 2-pin x 9-pin header (W1 to W9).

I/O Addressing

The ZT 88CT62 requires eight consecutive I/O port locations and decodes 8 or 16 bits for its I/O address. The default I/O address range is F040h to F047h. The STD signal "IOEXP" is available for expanded I/O systems.

Specifications

Electrical

STD 32- and STD Bus-compatible

Power Req.	Min.	Тур.	Max.
Supply Voltage, V _{CC}	4.75V	5.00V	5.25V
Supply Current, V _{CC} = 5.0V	111-11	11mA	35mA
Aux Voltage, 11-16V	11.00V	12.00V	16.00V
Aux Current, 15V	elem bos	9.8mA	15mA

 Optically Isolated Input Specifications 1500V Isolation

> T_{rise}: 100µsec T_{fall}: 5µsec

Standard Input Characteristics

ON OFF $15.0V < V_{in} < 91V$ $0 < V_{in} < 5.0V$ $0.25\text{mA} < I_{in} < 6.3\text{mA}$ $0 < I_{in} < 6.4\mu\text{A}$

Environmental		
Operating Temperature	-40° to +85° Celsius	
Storage Temperature	-55° to +105° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

Mechanical

- Backplane-compatible with STD 32 and STD-80 mechanical specifications
- Measures 4.5" (11.4cm) by 6.5" (16.5cm)
- Component Height: 0.38" (9.7mm)
 Weight: 5.6 oz (158.8g)
- Connectors

P1: 114-pin STD 32 Bus

J1-J4: 12-pin screw terminals

for isolated inputs

J5: 2-pin screw terminal for counter/timer input

W1-9: clock, gate, and output

for the three counter/timers

STD 32 Compliance

• I/O Slave: SA8-D8, A16, I, IXP

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz)

Reliability

- MTBF: 50 years
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 88CT62 Optically Isolated Input and Counter/ Timer Interface

ZT M88CT62 Optically Isolated Input and Counter/Timer Interface manual

All products are shipped FOB San Luis Obispo, CA USA. OEM discounts are available for most products. Contact Ziatech for additional information.



ZT 88CT72

144-Point Digital I/O Interface

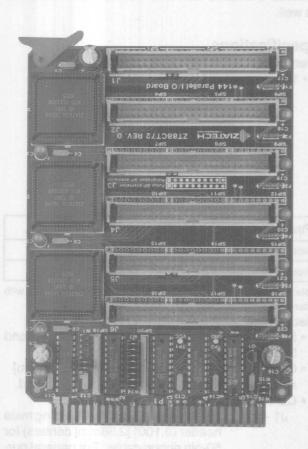
Interface provides 144 digital lines for I/O-intensive STD Bus computer applications

The ZT 88CT72 is a high-current, bidirectional interface providing 144 digital lines that interface STD Bus computers with instruments, peripherals, and industry standard signal conditioning racks such as those manufactured by Ziatech, Opto 22, Gordos, Crydom, Grayhill, Potter & Brumfield, etc.

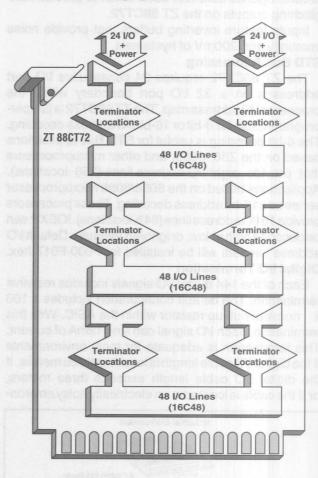
The interface is designed for I/O-intensive STD computer applications that normally require multiple digital I/O cards. Application Specific Integrated Circuit (ASIC) technology on the interface allows system

integrators to consolidate their I/O requirements, reducing system board count and cost while increasing system reliability.

The ZT 88CT72 combines low power consumption with an extended temperature operating range to accommodate harsh industrial or outdoor environments. It utilizes CMOS components but is also TTL backplane-compatible. The digital interface operates in temperatures ranging from -40° to +85° Celsius.



- STD 32[®]- and STD-compatible
- · Selectable 8- or 16-bit I/O addressing
- 144 bidirectional digital I/O signals with termination
- 12mA sink current at VOL of 0.4V
- · Write-protect mask register for output registers
- Self-contained power-up reset circuitry



- Cables available for connection to I/O mounting racks
- Extended temperature operation (-40° to +85° C)
- Compatible with industry standard I/O signal conditioning modules
- Software support through device driver software (STD DDP)

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40° to $+85^{\circ}$ C. (Users should make adjustments for temperature rise in enclosures.)



Digital I/O Operation

The ZT 88CT72 includes 144 digital I/O signals. Each signal is individually programmable for input, output, or output with readback operation. The 144 signals are provided through six 50-pin latching connectors. Each connector is organized to provide 24 digital I/O signals with alternating grounds to improve noise immunity. Each connector also includes fused power (+5V at 1A), required by many industry standard I/O signal conditioning racks, such as those manufactured by Opto 22 and Ziatech.

Each output point provides low true, open collector, non-glitching operation. Non-glitching outputs are desirable to prevent inadvertent I/O operation of a critical nature. Special care has been taken to provide non-glitching outputs on the ZT 88CT72.

Inputs feature inverting buffers that provide noise immunity and 200mV of hysteresis.

STD Bus Addressing

The ZT 88CT72 requires 24 consecutive I/O port addresses on a 32 I/O port boundary within the processor I/O address map. The ZT 88CT72 is jumper-programmable for 8-bit or 16-bit I/O address decoding. The 8-bit decoding is useful for STD Bus applications based on the Z80, 8085, and other microprocessors that provide eight I/O address lines (256 locations). Applications based on the 8088/8086 microprocessor series use 16-bit address decoding. These processors provide 16 I/O address lines (64 K locations). IOEXP can be decoded high or low, or ignored (default). Default I/O address jumpers will be installed for F000-F017 hex. Digital I/O Termination

Each of the 144 digital I/O signals includes resistive termination. The default configuration includes a 100 k nominal pull-up resistor within the ASIC. With this termination, each I/O signal can sink 12mA of current. This termination is adequate for most environments if the digital I/O cable length is less than three meters. If the digital I/O cable length exceeds three meters, or if the cable is located in an electrically noisy environ-

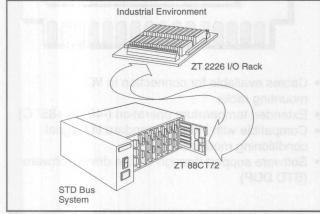


Figure 1. The ZT 88CT72 connects STD 32 and STD Bus systems to various industrial environments

ment, it may be necessary to add pull-up termination or a pull-up/pull-down termination. Termination network locations are provided for user-installed termination networks.

Signal Conditioning Modules

The ZT 88CT72 (with six ZT 90072 cables) allows direct control of 144 signal conditioning modules using the industry standard 50-pin I/O module bus. Each bank of 24 control lines can be used for module control or interrogation. Each bank also has its own fused, 1A 5V logic supply for the modules. These industrial modules control machinery for process control, automation, etc.

Software Support

The ZT 88CT72 manual includes several examples of software routines used to drive the ZT 88CT72. Ziatech's STD Device Driver Package (STD DDP) includes a linkable device driver for the ZT 88CT72 as well.

Specifications

Electrical

 144 terminated bidirectional I/O lines Output:

Inverting open collector operation 100 k nominal pull-up resistor

V_{OH} = 3.0V min.at -4.0mA

• V_{OL} = 0.4V max. at 12.0mA

Input:

Inverting buffers

100 k nominal pull-up resistor

Power Req.	Min.	Тур.	Max.
Supply Voltage, V _{CC}	4.75V	5.00V	5.25V
Supply Voltage, V _{CC} = 5.0V	16mA	32mA	70mA

Note: Currents given for quiescent operation will vary with external devices attached.

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 specifications.
- Occupies two STD slots (0.625-inch [15.88 mm] spacing) with six 50-pin ribbon cables attached.
- Connectors

J1 - J6: 50-pin vertical, dual-row latching male header (0.100" [2.58mm] centers) for 50-pin ribbon cable. For general purpose digital I/O, including fused +5V.

Environmental		
Operating Temperature	-40° to +85° Celsius	
Storage Temperature	-55° to +105° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

STD 32 Compliance

• I/O Slave: SA8-I

Note: SA8 is equivalent to STD-80 Series Rev. 2.3

(5 and 8 MHz).

Reliability

• MTBF: 86 years

• MTTR: five minutes (based on board replacement)

Ordering Information

ZT 88CT72 144-Point Digital I/O Interface ZT M88CT72 144-Point Digital I/O Interface manual

Accessories:

Cables (see Data Book cable section for details):

ZT 90021 10' (3m), 50-pin to 50-pin card ZT 90028 40" (1m), 50-pin to 25-pin D-shell ZT 90072 10' (3m), 50-pin both ends ZT 90137 2' (0.6m), 50-pin both ends

Boards (see separate data sheets for details):

ZT 2224 24-Line Termination Assembly ZT 2226 24-Channel I/O Mounting Rack

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

40" (1m), 50-pin to 25-pin D-shell

ZIATECH



ZT 88CT73

Optically Isolated Industrial I/O Interface

Interface provides eight optically isolated inputs and outputs for industrial STD Bus computer applications

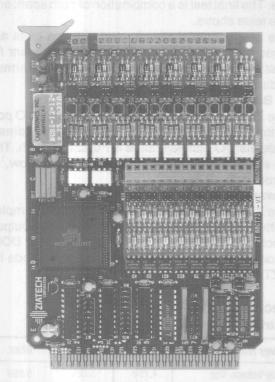
The ZT 88CT73 is a general purpose 8-input and 8-output interface board that operates over extended temperatures with optical isolation. Its wide voltage range and current capacities make it useful for many applications, from transportation to machine control. Optical isolation on the ZT 88CT73 provides immunity from the electrical "noise" found in many environments.

Each input on the ZT 88CT73 provides debouncing over the input ranges up to 91VDC and is terminated to a pair of screw terminals. One terminal is for the current/voltage source and the other is for the return. Input transitions can generate an event sense interrupt, and one input can be used as an emergency

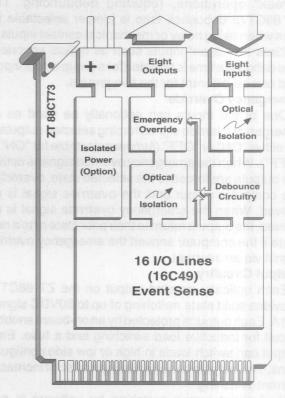
override that forces selected outputs either ON or OFF as desired.

Each output on the ZT 88CT73 provides solid state switching of up to 80VDC signals at 1A. The outputs are protected with on-board snubber circuits for inductive load switching and are also fused. Each output can switch loads in high or low side configurations and is terminated to a pair of screw terminals. One terminal is for the current/voltage source and the other is for the return. Two outputs can operate in parallel for increased current switching.

Both input and output terminals are located on removable plugs for easy maintenance and wiring.



- STD 32®- and STD-compatible
- Selectable 8- or 16-bit I/O addressing
- · Eight optically isolated and debounced inputs
- · Optional event sense on inputs
- Eight optically isolated and protected outputs
- Optional emergency override with output forcing



- Screw terminals on removable plugs for input and outputs
- · Write-protect mask register for outputs
- Low power/extended temperature operation (-40° to +85° C)
- Software support through device driver software (STD DDP)



Input Circuitry

The ZT 88CT73 provides eight separate debounced, optically isolated inputs that are conditioned to sense a wide range of DC voltage levels. Each input can be jumpered to sense "ON" and "OFF" conditions on three different voltage ranges. The factory default configuration senses 40 to 80VDC for "ON" and 0 to 5.4VDC for "OFF." Two other voltage ranges are also available. In addition to the default, 10 to 40VDC and 0 to 1.8VDC are available for "ON" and "OFF", as well as 4.5 to 5.5VDC and 0 to 0.4VDC for "ON" and "OFF."

Each of the eight inputs can be software programmed to generate an interrupt for an "ON" or "OFF" event. The inputs event sense polarity is programmed in groups of four. The event sense interrupt is jumper selectable on the backplane.

Debouncing

Each isolated input features debouncing of extraneous level changes that could result when interfacing to electrically noisy inputs or mechanical contacts. Mechanical contacts bounce on both the "make" and "break" operations, requiring debouncing. The ZT 88CT73 debounce time is jumper selectable for 3ms when using noisy or mechanical contact inputs or 0.03ms for "clean" inputs such as optical encoders. The debounce time is selected for a group of four inputs and can be different for the two groups.

Emergency Override

One of the inputs can optionally be used as an emergency override signal, forcing selected outputs to be either "ON" or "OFF" (jumper selectable for "ON" or "OFF"). When the emergency override signal is active, the outputs are forced to the selected state, overriding the computer output until the overrride signal is removed. When the emergency overrride signal is removed, the outputs return to their prior state or to a new state if the computer sensed the emergency override signal via an interrupt.

Output Circuitry

Each optically isolated output on the ZT 88CT73 provides solid state switching of up to 80VDC signals at 1A. Each output is protected by an on-board snubber circuit for inductive load switching and a fuse. Each output can switch loads in high or low side configurations. Two outputs can operate in parallel for increased current switching.

Inadvertent output switching by software is prevented by using the on-board write-mask register. The write-mask register is used to unlock the output register that controls the outputs.

Screw Terminal Connections

Both inputs and outputs are connected to the ZT 88CT73 by removable screw terminal plugs. Each group of eight inputs or outputs is located on a separate plug, which may be purchased from Ziatech (ZT 98044) or directly from Phoenix Contact.

Optical Isolation

Optical isolation is achieved with low-current, highgain photo transceivers. All inputs and outputs are isolated from each other by 1500V. The computer is isolated by a 1500V barrier.

Isolated Power Output Option

The ZT 88CT73 can be configured with an optional isolated power output for external devices such as optical encoders, resolvers, interface circuitry, etc. For a current list of output voltages and currents for this option, please see the ordering information. Contact Ziatech for special configurations.

Transient and Noise Suppression

The ZT 88CT73 features transient and noise suppression circuitry to protect the host computer from exposure to inductive and capacitive load switching and exposure to lightning strikes. The board passes both spark and surge voltage tests.

The spark test simulates exposure to mechanical relay contacts and signals with very short rise times. The spark test uses a 5 kHz, 2kV burst with a rise time of 5 nanoseconds.

The surge voltage test uses a 3kV, 50 microsecond pulse. The final test is a combination of both spark and surge tests above.

The environmental stimuli used in these tests are derived from IEC 801.1-5, *Electronic Equipment for Industry and Trade*, and several Swedish and German standards.

STD Bus Addressing

The ZT 88CT73 requires eight consecutive I/O port locations and decodes 8 or 16 bits for its I/O address. The default I/O address range is F0E0 to F0E7h. The STD signal IOEXP can be decoded high or low, or ignored (default).

Software Support

The ZT 88CT73 manual includes several examples of software routines used to perform input and output. Ziatech's STD Device Driver Package (STD DDP) includes a linkable device driver and source code for the ZT 88CT73.

Specifications

Electrical

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	illet u nos-	235mA	335mA
-V1 Option	B Ullin	91 10 Fo 91	BIDEIOS
Aux Voltage, V _{aux+}	11.0V	MUSCH VILSON	15.0V
Aux Current, V _{aux} = +12.0V I _{Load} = 0-200mA	25mA	Host Viscili	285mA

ZT 88CT73 Optically Isolated Industrial I/O Interface

Input Characteristics #1	Min.	Max.
Input Voltage "ON State" (VIN)	40V	80V
Input Current "ON State" (IIN)	2mA	4.8mA
Input Voltage "OFF State" (VIN)	OV	5.4V
Input Curent "OFF State" (IIN)	0μΑ	10μΑ
Input Characteristics #2		
Input Voltage "ON State" (VIN)	10V	40V
Input Current "ON State" (IIN)	2.0mA	15mA
Input Voltage "OFF State" (VIN)	0V	1.8V
Input Curent "OFF State" (IIN)	ОμΑ	10μΑ
Input Characteristics #3		
Input Voltage "ON State" (VIN)	4.5V	5.5V
Input Current "ON State" (IIN)	1mA	10mA
Input Voltage "OFF State" (VIN)	0V	.4V
Input Curent "OFF State" (IIN)	0μΑ	10μΑ

Output Characteristics	Min.	Тур.	Max.
Voltage (continuous)	0V	-	80V
Voltage (peak)			100V
Load Current	0	-	1A
"ON-state" resistance	_	.27Ω	.40Ω
"OFF-state" resistance	400kΩ	FI -T	-
Output capacitance	nii - i	160pF	300pF
Turn-on time	-	100µs	520µs
Turn-off time	-	800µs	1ms

Mechanical

- Backplane compatible with STD 32 and STD-80 mechanical specifications
- Dimensions: 4.5" x 6.5" (11.4cm x 16.5cm)
- Height: 0.42" one STD slot (10.7mm)
- Weight: 6.0 oz. (170.1g)
- Connectors

P1: 114-pin STD 32 Bus

J1: 16-pin header compatible with 16-pin screw terminal on removable plug (ZT 98044) for isolated outputs

J2: 16-pin header compatible with 16-pin screw terminal on removable plug (ZT 98044) for isolated outputs

J3: 2-pin screw terminal for isolated power output option

Environmental					
Operating Temperature	-40° to +85° Celsius				
Storage Temperature	-40° to +85° Celsius				
Non-Condensing Relative Humidity	less than 95% at 40° Celsius				

STD 32 Compliance

• I/O Slave: SA8-I, IXL

Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz)

Reliability

• MTBF: 50 years

• MTTR: five minutes (based on board replacement)

Ordering Information

ZT 88CT73-Vx Optically Isolated Industrial

I/O Interface

ZT M88CT73 ZT 88CT73 manual

Must choose one isolated output voltage option

V0 No isolated output voltage desired V1 11 to 15VDC unregulated at

200mA

Other output voltages are available. Please contact Ziatech Corporation.

Accessories

ZT 98044 Set of two 16-screw terminal plugs

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.



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STD32°

ZT 89CT61

96-Point Digital I/O Interface

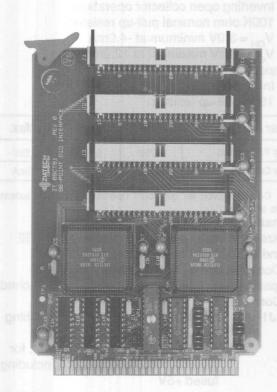
Interface provides 96 digital lines for I/O-intensive STD 32® and STD Bus computer applications

The ZT 89CT61 is a high-current, bidirectional interface providing 96 digital I/O lines for STD Bus computers. These lines connect the STD computer to instruments, peripherals, and industry standard signal-conditioning racks such as those manufactured by Ziatech, Opto 22, Gordos, Crydom, Grayhill, Potter & Brumfield, etc.

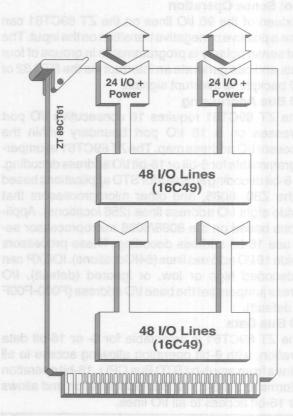
The interface is designed for I/O-intensive STD computer applications that normally require multiple digital I/O cards. Application Specific Integrated Circuit (ASIC) technology on the interface allows system

integrators to consolidate their requirements, reducing system board count and cost while increasing system reliability. The ZT 89CT61 also provides full 16-bit data operation on STD 32 systems or 8-bit data operation on STD systems.

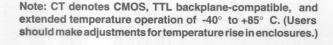
The ZT 89CT61 is designed and tested for -40° to +85° Celsius operation in harsh environments. This product is designed for use in conjunction with Ziatech's other LT (low temperature) and CT (CMOS, TTL-backplane-compatible) products for mobile and outdoor applications.



- STD 32- and STD-compatible
- Selectable 8- or 16-bit I/O addressing
- · Selectable 8- or 16-bit data operation
- 96 bidirectional digital I/O signals with termination
- 12mA sink current at V_{OL} of 0.4V
- · Write-protect mask register for output registers
- · Self-contained, power-up reset circuitry



- Sixteen event sense inputs for interrupts
- Cables available for connection to I/O mounting racks
- Extended temperature operation (-40° to +85° C)
- Compatible with industry standard I/O signal-conditioning modules





Digital I/O Operation

The ZT 89CT61 includes 96 digital I/O signals. Each signal is individually programmable for input, output, or output with readback operation. The 96 signals are provided through four 50-pin latching connectors. Each connector is organized to provide 24 digital I/O signals with alternating grounds to improve noise immunity. Each connector also includes fused power (+5V at 1A) required by many industry standard I/O signal conditioning racks.

When programmed for output, low true open collector, non-glitching operation is provided. Non-glitching outputs are desirable to prevent inadvertent critical I/O operation. Special care has been taken to provide non-glitching outputs on the ZT 89CT61.

When programmed for input, inverting buffers provide input hysteresis of 200mV, as well as noise immunity on the input signals.

Event Sense Operation

Sixteen of the 96 I/O lines on the ZT 89CT61 can sense a positive or negative transition on the input. The input sense polarity is programmable in groups of four inputs and can generate an interrupt via the STD 32 or STD backplane interrupt signals.

STD Bus Addressing

The ZT 89CT61 requires 16 consecutive I/O port addresses on a 16 I/O port boundary within the processor I/O address map. The ZT 89CT61 is jumper-programmable for 8-bit or 16-bit I/O address decoding. The 8-bit decoding is useful for STD applications based on the Z80, 8085, and other microprocessors that provide eight I/O address lines (256 locations). Applications based on the 8088/8086 microprocessor series use 16-bit address decoding. These processors provide 16 I/O address lines (64K locations). IOEXP can be decoded high or low, or ignored (default). I/O address jumpers set the base I/O address (F000-F00F hex default).

STD Bus Data

The ZT 89CT61 is selectable for 8- or 16-bit data operation, with 8-bit operation allowing access to all I/O lines from any 8-bit STD Bus CPU. 16-bit operation conforms to the STD 32 Bus Specification and allows 8- or 16-bit access to all I/O lines.

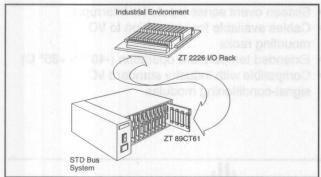


Figure 1. The ZT 89CT61 connects STD 32 and STD Bus systems to various industrial environments

Signal Conditioning Modules

The ZT 89CT61 (with four ZT 90072 cables) allows direct control of 96 signal conditioning modules using the industry standard 50-pin I/O module bus. Each bank of 24 control lines can be used for module control or interrogation. Each bank also has its own fused, 1A 5-volt logic supply for the modules. These industrial modules control machinery for process control, automation, etc.

Software Support

The ZT 89CT61 manual includes several examples of software routines used to drive the ZT 89CT61. Ziatech's STD Device Driver Package (STD DDP) includes a linkable device driver for the ZT 89CT61 as well.

Specifications

Electrical

 96 terminated bidirectional I/O lines Output:

Inverting open collector operation 100K ohm nominal pull-up resistor V_{OH} = 3.0V minimum at -4.0mA V_{OL} = 0.4V maximum at 12.0mA Input:

Inverting buffers 100K pull-up resistor

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	10mA	35mA	75mA

Note: Currents given for quiescent operation vary with external devices attached.

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 mechanical specifications
- Occupies one STD slot (0.625" [15.88mm] spacing) with four 50-pin ribbon cables attached
- Connectors

J1- J4: 50-pin right-angle, dual-row latching male header (0.100" [2.54mm] centers) for 50-pin ribbon cable; for general purpose digital I/O, including fused +5V

Environmental Commentation Comm					
Operating Temperature	-40° to +85° Celsius				
Storage Temperature	-55° to +105° Celsius				
Non-Condensing Relative Humidity	less than 95% at 40° Celsius				

STD 32 Compliance

• I/O Slave: SA16, SA8-I, IXP

Note: SA8 is equivalent to STD-80 Series Rev. 2.3

(5 and 8 MHz)

Reliability

• MTBF: 127 years

• MTTR: five minutes (based on board replacement)

Ordering Information

ZT 89CT61 96-Point Digital I/O Interface
ZT M89CT61 96-Point Digital I/O Interface manual

Accessories

Cables (see Data Book Cable section for details):

ZT 90021

10' (3m) flat, 50-pin header to

50-pin card

ZT 90028

40" (1m), printer emulation, 50-pin

header to 25-pin D-shell

ZT 90072

10' (3m) flat, 50-pin both ends

ZT 90137

2' (0.6m) flat, 50-pin both ends

Boards (see separate data sheets for details):

ZT 2224

24-Line Termination Assembly

ZT 2226

24-Channel I/O Mounting Rack

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for some products.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.

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ZT 2223

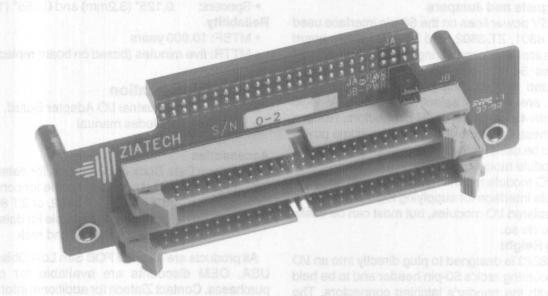
Industrial I/O Adapter Board

An adapter board for interfacing two 24-channel I/O mounting racks to Ziatech's ZT 8801, ZT 8802, and ZT 8901 single board computers

The ZT 2223 Industrial I/O Adapter Board converts the 56-pin (48 signal lines) digital I/O interface used on Ziatech's ZT 8801 and ZT 8802 single board V40 computers and ZT 8901 Single Board V53 Computer into two 50-pin, I/O mounting rack-compatible connectors with alternating signal and ground lines. The ZT 2223 adapter plugs directly onto the first I/O mounting rack using a downward-facing 50-pin connector and is secured to the mounting plate with standoffs. A 56-pin header on the ZT 2223 provides a cable connection to the host computer board, while a second 50-pin header provides a daisy-chain cable interface for a second I/O mounting rack.

The ZT 2223 is intended primarily for connecting I/O mounting racks that do not accept Opto 22 Genera-

tion 4® (G4) miniature modules. These I/O mounting rack manufacturers include Grayhill, Potter & Brumfield, Gordos, Crydom, Analog Devices, and many others. The standoffs on the ZT 2223 are designed to provide the appropriate mounting height when plugged into the 50-pin dual-row headers used on these manufacturers' racks. The ZT 2223 is not designed to mount to racks using a card edge connector. Ziatech manufactures the ZT 2226 24-Channel I/O Mounting Rack for use with Opto 22 G4 miniature modules. The ZT 2226 interfaces directly to the 56-pin connectors of the ZT 8801, ZT 8802, and ZT 8901 and provides daisychain capability to a second rack.



- Converts 56-pin digital I/O connector to two 50-pin connectors
- Interfaces to Ziatech's ZT 8801, ZT 8802, and ZT 8901 single board computers
- Interfaces to most 24-channel I/O module mounting racks
- Extremely compact 1.75" x 4.50" (4.4cm x 11.4cm)
- · Integral mounting hardware



Computer Interface

The ZT 2223's 56-pin latching dual-row header (connector J1) is used for interfacing to the 56-pin digital I/O connector used on the ZT 8801, ZT 8802, or ZT 8901 single board computers. Forty-eight signal lines, five ground lines, and three +5V power lines are provided on the standard Ziatech 56-pin interface. A 40-inch (1-meter) cable, the ZT 90089, is available to connect the host single board computer to the ZT 2223.

Connections to I/O Mounting Racks

Two 50-pin connectors are available on the ZT 2223 which provide interfacing for two I/O module mounting racks with up to 24 digital I/O lines each. The JA connector is a downward facing 50-pin female socket connector that allows the ZT 2223 adapter to plug directly into the 50-pin dual-row headers used on almost all I/O module mounting racks. Signal lines MOD0 to MOD23 are routed to the JA connector.

Connector JB is a 50-pin dual-row latching header, referred to as the daisy-chain connector. A 2-foot (61.0cm) 50-pin cable (ZT 90137) is available to connect the JB connector to a second I/O mounting rack. Signal lines MOD24 to MOD47 are routed to the JB daisy-chain connector.

Power Signals and Jumpers

Three +5V power lines on the 56-pin interface used by the ZT 8801, ZT 8802, and ZT 8901 single board computers are used for powering I/O module logic. +5V power lines 54, 55, and 56 are combined on the ZT 2223 and two shorting jumpers (JA_PWR and JB_PWR) are used to selectively route +5V logic power to pin 49 of the JA or JB connectors. Routing power to these connectors is useful if a single power supply is to be used for the entire system including the two I/O module mounting racks.

Not all I/O module mounting racks use pin 49 of the ribbon cable interface for supplying logic power to the optically isolated I/O modules, but most can be easily modified to do so.

Mounting Height

The ZT 2223 is designed to plug directly into an I/O module mounting rack's 50-pin header and to be held in place with the header's latching connectors. The ZT 2223 has two 1.125" (2.9cm) standoffs and a hardware spacer kit so that it can be mounted to I/O racks of varying heights. Both boards will rest flush on the mounting surface and allow both the ZT 2223 and the I/O mounting rack to be secured with number 6-32 machine screws.

Specifications Compatibility

- Compatible with 56-pin digital I/O connectors used on the ZT 8801, ZT 8802, and ZT 8901 single board computers
- Compatible with I/O module mounting racks using 50-pin dual-row headers

Mechanical

- Dimensions: 4.50" (11.4cm) W, 1.75" (4.4cm) L, 1.825" (4.6cm) H
- Connectors

J1: 56-pin male header, dual-row, vertical locking

JA: 50-pin female dual-row header,

downward facing

JB: 50-pin male header, dual-row,

vertical locking

Jumpers

JA_PWR: Power selection shorting jumper for

connector JA

JB_PWR: Power selection shorting jumper for

connector JB

Mounting hardware

• Standoffs: 1.125" (2.9cm) height spacers with

0.150" (3.8mm) smooth bores

• Spacers: 0.125" (3.2mm) and 0.065" (1.7mm)

Reliability

• MTBF: 10,800 years

MTTR: five minutes (based on board replacement)

Ordering Information

ZT 2223

Industrial I/O Adapter Board,

includes manual

Accessories

Cables (see Data Book cable section for details):

ZT 90089 40" (1m), 56-pin cable for connection

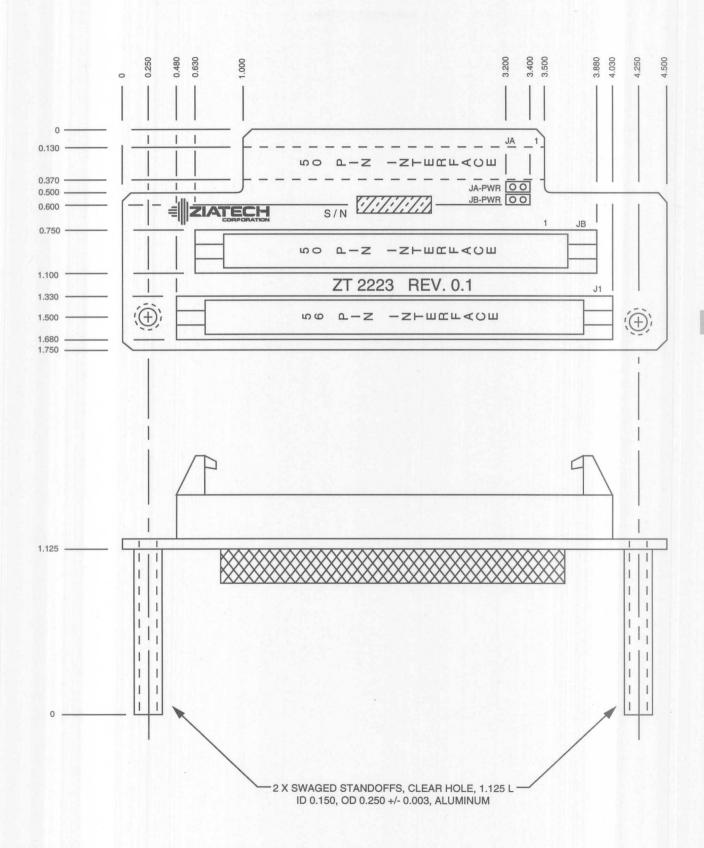
to ZT 8801, ZT 8802, or ZT 8901

ZT 90137 2' (0.6m), 50-pin cable for daisy-chain

connection to second rack

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Figure 1. Mechanical dimensions of ZT 2223 (in inches)





ZT 2224

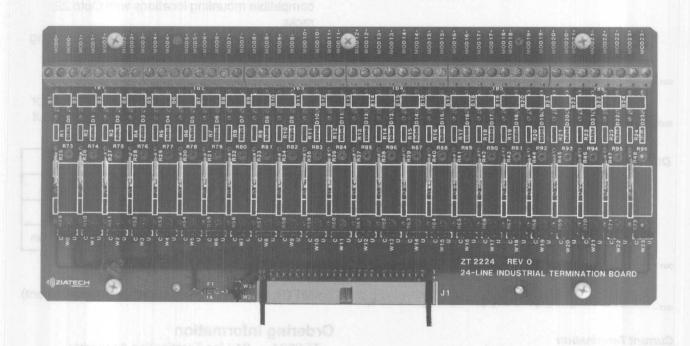
24-Line Termination Assembly

Termination assembly provides termination points and signal conditioning for Ziatech digital interface cards

The ZT 2224 24-Line Termination Assembly provides termination points and signal conditioning capabilities for Ziatech's ZT 8902/8911 processor cards, or any of Ziatech's general purpose digital I/O cards or input-only cards that accept TTL-level inputs. It can also be used with any of Ziatech's general purpose digital I/O cards for the STD Bus and PC Bus that accept TTL-level inputs.

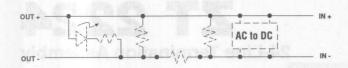
Screw terminals provide connections for 24 pairs of 14 AWG wire.

Locations are provided for user-installed signal conditioning components and display LEDs. This allows the ZT 2224 to accept AC or DC voltage or current inputs which are then conditioned into TTL-level inputs. Isolation between signals is 300V peak. A standard 50-pin ribbon cable connects the ZT 2224 to the STD interface card.

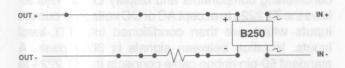


- Supports 24 unique inputs
- Locations for user-installed resistors/diodes for AC or DC voltage and current inputs
- · Locations for user-installed LEDs for each input
- Supports DC inputs from 0 to 300V
- · Supports AC inputs from 0 to 300V peak
- · Supports current inputs from 0 to 2.5A
- Input screw terminals accept up to 14 AWG wire
- Ribbon cable-compatible with Ziatech optically isolated input boards and general purpose I/O boards
- Mounting standoffs and screws included

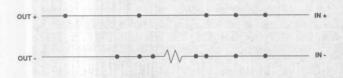




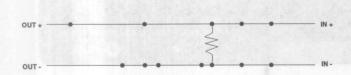
Termination Input Circuit



AC Termination - Uses Diode Bridge B250C from General Instruments.



DC Termination



Current Termination

The ZT 2224 provides a low-cost and versatile method for signal conditioning a wide range of inputs. The ZT 2224 interfaces to Ziatech digital input cards with optical isolation (ZT 8846 event sense, ZT 88CT49A digital input, ZT 88CT73 industrial I/O interface), as well as Ziatech's non-optically isolated digital I/O cards for the STD bus (ZT 8845, ZT 88CT72, ZT 89CT61), digital I/O cards for the PC bus (ZT 14CT72, ZT 14CT73), and Ziatech's ZT 8902/8911 processor

Specifications

Electrical

- Provides 300V isolation between inputs
- Supports DC inputs from 0 to 300V
- Supports AC inputs from 0 to 300V peak
- Supports current inputs from 0 to 2.5A

Mechanical

- Dimensions: 4.5" (11.4cm) to 9.9" (25.1cm), compatible mounting locations with Opto 22
- Mechanically compatible with Opto 22 mounting
- Connectors

TB1-TB6: Screw terminals for field

wiring inputs

50-pin latching rubber header for J1:

outputs to optically isolated input

boards

Environmental					
Operating Temperature	-40° to +85° Celsius				
Storage Temperature	-55° to +105° Celsius				
Non-Condensing Relative Humidity	less than 95% at 40° Celsius				

Reliability

MTBF: 2,430 years

MTTR: five minutes (based on board replacement)

Ordering Information

ZT 2224

24-Line Termination Assembly (for use with ZT 8902/ZT 8911 ZT 88CT49A, ZT 8846 ZT 8845, ZT 88CT72, ZT 89CT61 ZT 14CT72/ZT 14CT73), includes manual

Accessories:

ZT 90072 10' (3m), 50-pin ribbon cable. For connecting the ZT 2224 to the 50-pin connectors on the above mentioned boards



ZT 2225

Industrial I/O Cable Adapter

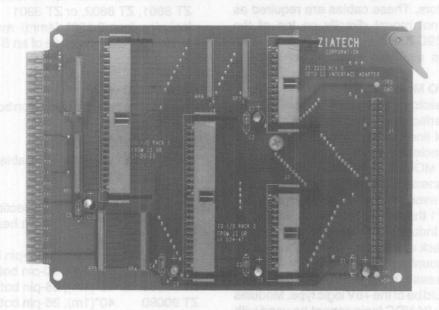
A piggy-back adapter board for interfacing two 24-channel I/O mounting racks to Ziatech's ZT 8801, ZT 8802, and ZT 8901 single board computers

The ZT 2225 Industrial I/O Cable Adapter converts the 56-pin (48 signal lines) digital I/O interface used on Ziatech's ZT 8901, ZT 8802, and ZT 8801 single board computers (SBCs) into two 50-pin, I/O mounting rack-compatible connectors with alternating ground and signal lines. The ZT 2225 adapter mounts directly on top of the SBCs, mating directly to the 56-pin digital I/O connector and a nylon standoff. Two 50-pin cables, up to 10 feet (3m) in length (ZT 90072 or ZT 90021), are attached between the ZT 2225 and two 24-channel industrial I/O mounting racks.

Any I/O mounting rack using a standard 50-pin connector can be connected to the ZT 2225, such as those manufactured by Ziatech, Opto 22, Grayhill,

Crydom, Potter & Brumfield, Analog Devices, Gordos, and others. Ziatech's ZT 2226 24-channel I/O Mounting Rack interfaces directly to the 56-pin connectors of the SBCs and provides daisy-chain capability to a second rack. The ZT 2226 accepts Opto 22 G4 and Grayhill G5 miniature modules.

The ZT 2225 may also be used to convert up to two digital I/O 26-pin connectors found on the ZT 8832 I/O Control Processor and ZT 89CT30 Integer DSP Control Processor boards into 50-pin I/O mounting rack-compatible connectors. Additional cables (ZT 90090) between the ZT 2225 and the processor board are required in this configuration.



- Converts 56-pin digital I/O connector of the ZT 8801, ZT 8802, or ZT 8901 to two 50-pin connectors
- Mounts directly to the ZT 8801, ZT 8802, and ZT 8901 (requires one additional backplane slot)
- Converts two 26-pin digital I/O connectors of the ZT 8832 and ZT 89CT30 processors to two 50-pin connectors
- Can be remotely mounted from the processor board
- Interfaces to most 24-channel I/O module mounting racks
- Enables two I/O mounting racks to mount up to
 10 feet away from the computer
- STD card size with integral mounting hardware
- Extended operating temperature



Computer Interface

The ZT 2225's primary purpose is to convert the 56pin digital I/O connector on the ZT 8801, ZT 8802, or ZT 8901 into two 50-pin connectors with interleaved ground and signal lines. The ZT 2225 mounts directly to the 56-pin digital I/O connector on the SBCs using the downward facing 56-pin female socket (J1). In this configuration, the ZT 2225 uses one additional STD slot in the card cage to the left of the processor board. The ZT 2225 can also be connected to an SBC using a 56-pin ribbon cable. The ZT 2223 Industrial I/O Adapter Board is the preferable adapter if this is the desired configuration. Forty-eight signal lines, five ground lines, and three +5V power lines are provided on the standard Ziatech 56-pin digital I/O interface. The ZT 2225 divides the forty-eight signal lines evenly between two 50-pin latching connectors.

The ZT 2225 also converts the 26-pin digital I/O connectors found on the ZT 8832 and ZT 89CT30 processors into industrial I/O rack-compatible 50-pin connectors. Two 26-pin latching connectors are provided (J2 and J3) for cabling the ZT 2225 to 26-pin digital I/O connectors. These cables are required as the ZT 2225 will not mount directly on top of the ZT 8832 or ZT 89CT30 processor boards. The ZT 90090 cable is available from Ziatech for this purpose.

Connections to I/O Mounting Racks

Two 50-pin connectors (J4 and J5) are available on the ZT 2225 for interfacing to two I/O module mounting racks with up to 24 lines each. Signal lines MOD0 to MOD23 from connector J1 are routed to connector J5 while signal lines MOD24 to MOD47 are routed to connector J4. Connectors J4 and J5 provide ground signals on all the even pins while MOD signals are found on odd pins 1 through 47. Pin 49 provides +5V logic for powering industrial I/O modules on the connected mounting rack across the 50-pin ribbon cable. Not all industrial mounting racks accept power on pin 49, but most can be easily modified. I/O modules on the mounting rack should be of the +5V logic type. Modules using +15 VDC or +24 VDC logic cannot be used with Ziatech equipment.

Ziatech provides several 50-pin cables for connecting the ZT 2225 to industrial I/O mounting racks using dual-row headers and card edge connectors. The longest recommended cable distance is 10 feet (3m) without additional shielding. The interleaved ground signals on the standard 50-pin interface provide immunity to noise and crosstalk.

Specifications Compatibility

- Compatible with the 56-pin digital I/O connectors used on the ZT 8801, ZT 8802, and ZT 8901 single board computers
- Compatible with the 26-pin digital I/O connectors used on the ZT 8832 and ZT 89CT30 processor boards
- Interfaces to any industry standard I/O module mounting rack using 50-pin dual-row headers or 50-pin card edge connectors, with a 50-pin ribbon cable

Mechanical

- Dimensions: 4.5" (11.3cm) x 6.5" (16.5cm)
- Connectors
 - J1: 56-pin female dual-row socket, on bottom side of board
 - J2, J3: 26-pin male latching dual-row header J4, J5: 50-pin male latching dual-row header

Mounting hardware

- Includes a nylon standoff for mounting on top of the ZT 8801, ZT 8802, or ZT 8901
- Includes four 0.156" (4mm) mounting holes for remote mounting outside of an STD bus card cage

Reliability

- MTBF: 100 years
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 2225 Industrial I/O Cable Adapter

Accessories

Cables (see Data Book Cable section for details):

ZT 90021	10' (3m), 50-pin header to 50-pin
	card edge
ZT 90022	9.5"(24cm), 50-pin both ends
ZT 90072	10' (3m), 50-pin both ends
ZT 90089	40"(1m), 56-pin both ends
ZT 90090	40"(1m), 26-pin both ends
ZT 90137	2' (61cm), 50-pin both ends

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.



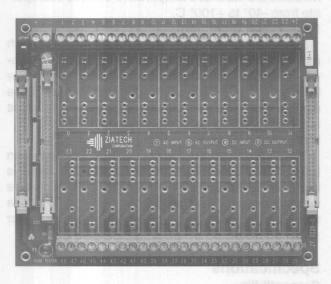
ZT 2226 24-Channel I/O Mounting Rack

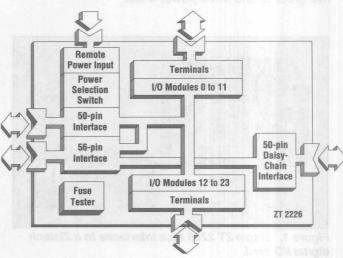
A 24-position I/O module mounting rack for industrial control applications that require optically isolated field connections

The ZT 2226 24-Channel I/O Mounting Rack accommodates up to 24 Generation 4 (G4) I/O modules from Opto 22 or G5 modules from Grayhill. The ZT 2226 connects to the host computer using the industry standard 50-pin ribbon cable (24 signal lines) or Ziatech's high-density 56-pin ribbon cables (48 signal lines). A second ZT 2226 or another vendor's 24-channel rack may be daisy-chain connected using a 50-pin cable. In this way, two ZT 2226 racks easily

connect to any Ziatech single board computer via a high-density 56-pin (48 signal line) digital I/O port.

In addition to the 24 mounting positions for G4 and G5 miniature modules, the ZT 2226 features a fuse tester and large 10 AWG screw terminals for field wiring each I/O channel. The user can also selectively provide power for I/O modules across the host computer's ribbon cable or at the rack itself.





- Supports 24 I/O modules
- Expandable to 48 I/O modules (daisy-chain feature)
- Physically compatible with Opto 22 G4 I/O racks
- Compatible with Opto 22 G4 and Grayhill G5 miniature modules
- Interfaces to most 50-pin (24-signal) industrial I/O interfaces
- Interfaces directly to all Ziatech digital I/O cards for STD and PC bus
- Interfaces directly to Ziatech single board computers with 56-pin (48 signal) headers
- Latching, dual-row headers used for all three connectors
- · Integral mounting hardware
- User selectable power inputs
- Large 10 AWG screw terminal connectors
- Integral fuse tester with LED
- Extended operating temperature (-40° to +85° C)



Computer Interface

The ZT 2226 supports industry standard 50-pin ribbon cables that interface with 24 signal lines interleaved with ground lines. The J1 connector provides the 24 signal lines on odd numbered pins (1, 3, ... 45, 47) and interleaved grounds on even numbered pins (2, 4, 6, ... 48, 50). Pin 49 can be used to receive +5V logic power for the I/O modules across the ribbon cable. All Ziatech digital I/O cards provide +5V on pin 49. A slide switch selects power for the I/O modules from either the ribbon cable or separate power screw terminals. *Figure 1* shows a ZT 2226 interfaced to a Ziatech digital I/O card using the 50-pin J1 interface.

Another way to interface to the host computer is through the 56-pin J2 connector. This dual-row header provides direct connection to the 56-pin headers of Ziatech single board computers such as the ZT 8801 Single Board V40 Computer and ZT 8901 Single Board V53 Computer. The 56-pin headers provide 48 signal, five ground, and three power lines.

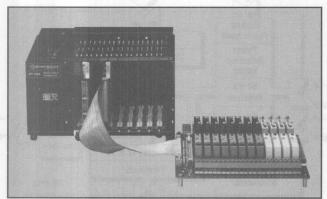


Figure 1. Single ZT 2226 rack interfaces to a Ziatech digital I/O card.

Daisy-Chain Connection

When connecting the ZT 2226 to a Ziatech single board computer using the 56-pin (48-signal line) digital I/O connector, 24 of the 48 signal lines route to the ZT 2226's I/O modules and the other 24 signals route to the 50-pin daisy-chain connector (J3) on the opposite end of the ZT 2226. This feature enables a second ZT 2226, or any industry standard I/O mounting rack with a standard 50-pin connector, to interface to the host computer. Figure 2 shows two ZT 2226 I/O mounting racks connected to a ZT 8901 Single Board V53 Computer. This configuration is possible by connecting a 56-pin ribbon cable to J2 of rack #1, and connecting a short, 50-pin ribbon cable from J3 of rack #1 to J1 of rack #2. This configuration terminates signals MOD 0 to 23 on rack #1 and MOD 24 to 47 on rack #2. The daisy-chain configuration also routes power and ground to both ZT 2226 racks. A second ZT 2226 is not required to use the 56-pin interface.

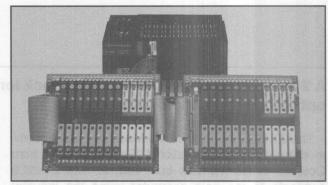


Figure 2. Two ZT 2226 racks in a daisy-chain configuration with a Ziatech single board computer.

I/O Module Capability

Both Opto 22 and Grayhill offer a complete line of miniature I/O modules that plug directly into the ZT 2226. The compact Opto 22 G4 modules have an operating temperature range of -30° to +70° C. The Grayhill G5 modules are extended temperature devices that operate from -40° to +100° C.

Input Power Selection

5 volt power sources are selected with a slide switch mounted on the ZT 2226. The user can choose between a power source attached to the 10 AWG screw terminals or the ribbon cable interface. This feature is useful when remote power supply operation is required.

Integral Fuse Tester

The ZT 2226 has a go/no-go fuse tester that lights an LED when a good fuse is installed. The fuse tester is designed to accept a Schurter MSF 250 microfuse which is used on the Opto 22 G4 modules. The fuse tester can be used as a spare fuse holder or power status indicator.

Specifications

Compatibility

- Compatible with Opto 22 G4 modules and Grayhill G5 modules
- Compatible with all standard 50-pin I/O interfaces
- Compatible with all Ziatech 56-pin I/O interfaces

Electrical

- 10 AWG Field Terminals
 Rated to 500 Vrms
 Rated at 5 Amps
- Power requirements (The ZT 2226 accommodates 5V logic I/O modules only and is not intended for 15V or 24V modules.)

Power Req.	Min.	Тур.	Max.
Supply Voltage, V _{CC}	4.75V	5.00V	5.25V
Supply Current, V _{CC} = 5.0V		-	2.0*A

^{*}This current exceeds what can be supplied through ribbon cables.

Mechanical

- Dimensions: 6.25" (15.9cm) by 7.5" (19.0cm)
- Height with G4 modules installed: 2.40" (6.1cm)
- Height with G5 modules installed: 3.30" (8.4cm)
- Weight without modules installed: 9 oz. (255.1g)
- Connectors

J1 and J3: 50-pin low-profile male header,

dual-row, vertical, locking

J2: 56-pin low-profile male header,

dual-row, vertical, locking

J4 and J5: Screw terminal strips accept up to

10 AWG wire for field wiring

J6: Logic power screw terminals accept

up to 10 AWG wire for 5V and GND

F1: Fuse tester accepts Schurter MSF

250 microfuses

Power Source Switch

SW1: SPDT slide switch has two positions

to select ribbon cable or screw terminal power

Mounting hardware

• Standoffs: 0.625" (15.9mm) height spacers with

0.150" (3.8mm) smooth bores

Environmental	
Operating Temperature	-40° to +85° Celsius
Storage Temperature	-55° to +105° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

Refer to the Opto 22 and Grayhill data sheets for operating and storage temperature specifications on G4 and G5 modules.

Opto 22 Compatibility

- Compatible with these Opto 22 module types: G4OAC5*, G4ODC5*, G4IAC5*, G4IDC5*
- * And all suffix types preceded by this part number

Grayhill Compatibility

- Compatible with these Grayhill module types: 70G-OAC5**,70G-ODC5**,70G-AC5**,70G-IDC5**
- ** And all suffix types preceded by this part number

Reliability

- MTBF: 224 years
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 2226 24-Channel I/O Mounting Rack ZT M2226 24-Channel I/O Mounting Rack

manual

Accessories

Cable (see Data Book cable section for details):

ZT 90022 9.5" (24.1cm), flat, 50-pin both ends

ZT 90072 10' (3m), flat, 50-pin both ends

ZT 90089 40" (1m), flat, 56-pin both ends

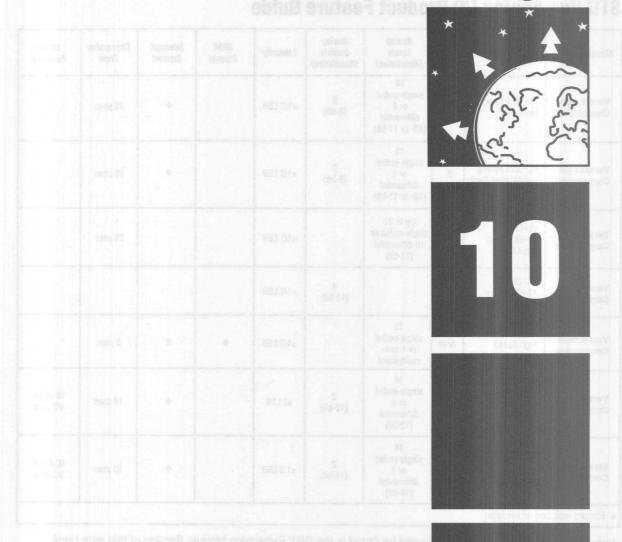
All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.

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STD Bus Analog I/O



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STD Bus Analog I/O Product Feature Guide

Manufacturer*	Product	Data Path (bits)	Analog Inputs (Resolution)	Analog Outputs (Resolution)	Linearity	DMA Support	Interrupt Support	Conversion Time	Other Features
VersaLogic Corporation	VL-1225 Analog Input Card	8	16 single-ended or 8 differential (10- or 11-bit)	2 (8-bit)	±1/2 LSB		٠	25 µsec	
VersaLogic Corporation	VL-1226 Analog Input/Output Card	8	16 single-ended or 8 differential (10- or 11-bit)	2 (8-bit)	±1/2 LSB		٠	25 µsec	
VersaLogic Corporation	VL-1260 12-Bit Analog Input Card	8	Up to 32 single-ended or 16 differential (12-bit)		±1/2 LSB			25 µsec	
VersaLogic Corporation	VL-1262 12-Bit Analog Output Card	8		4 (12-bit)	±1/2 LSB				
VersaLogic Corporation	VL-1295 High Speed Analog Input Card	8/16	16 single-ended or 1 non- multiplexed		±1/2 LSB	•	٠	3 µsec	
VersaLogic Corporation	VL-12CT96 Analog and Digital Input/Output Card	8/16	16 single-ended or 8 differential (12-bit)	2 (12-bit)	±1 LSB		٠	10 µsec	16 digital I/O lines
VersaLogic Corporation	VL-12CT97 Analog and Digital Input/Output Card	8/16	16 single-ended or 8 differential (16-bit)	2 (12-bit)	±1.5 LSB		•	10 µsec	16 digital I/O lines

Note: Additional analog I/O products can be found in the SBX Expansion Module Section of this data book.

^{*} VersaLogic Corporation's Analog I/O cards are available directly from Ziatech. Each interface is compatible with Ziatech STD and STD 32 products, and is supported by a software driver in Ziatech's STD Device Driver Package (STD DDP). A brief description of these VersaLogic products is included in this section. For the complete technical data sheets, contact Ziatech. VersaLogic can be contacted directly at (800) 824-3163.

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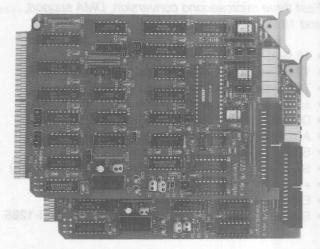
STD Bus Analog I/O Products

from VersaLogic Corporation

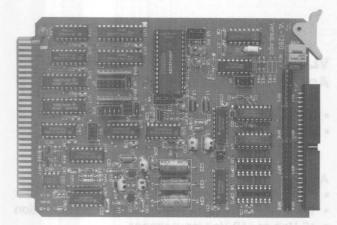
VL-1225/26 Analog Input/Output Card



- 16 single-ended / eight differential input channels
- 10-bit or 11-bit input resolution (jumper selections)
- · Fast 25 microsecond input conversion time
- 0 to +10, ±5, and ±10 Volt ranges
- Two 8-bit output channels (VL-1225 only)
- Interrupt support
- +5 Volt single supply operation
- I/O or memory addressing
- Universal STD bus processor-compatible
- Plug-in replacement for Analog Devices RTI-1225/26
- STD 32®- and STD 80-compatible



VL-1225/26 Analog Input/Output Card



VL-1260 12-Bit Analog Input Card

VL-1260 12-Bit Analog Input Card

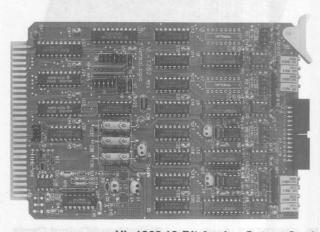
Wide input range, and up to 32 input channels

- 16 single-ended / eight differential input channels
- 32 single-ended / 16 differential inputs (optional)
- 12-bit resolution (4096 counts)
- Fast 25 microsecond conversion time
- 10 mVolt to ±10 Volt input range
- +5 Volt single supply operation
- I/O or memory addressing
- Universal STD bus processor-compatible
- Plug-in replacement for Analog Devices RTI-1260

VL-1262 12-Bit Analog Output Card

Four output channels, 12-bit resolution, and optional current loop outputs

- Four analog output channels
- Dual current loop outputs (optional)
- 12-bit resolution (4096 counts)
- 0 to 5, 0 to 10, ±5, and ±10 Volt output ranges
- +5 Volt single supply operation
- Extended temperature version available
- Plug-in replacement for Analog Devices RTI-1262



VL-1262 12-Bit Analog Output Card



Telephone (800) 824-3163



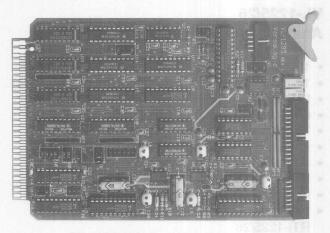
VL-1295

STO32

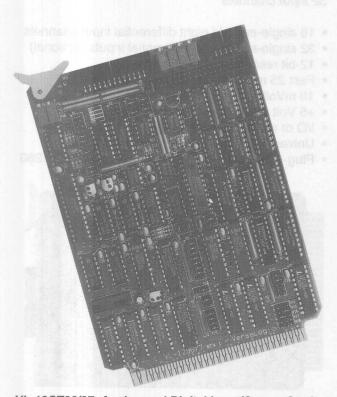
High Speed Analog Input Card

Fast three microsecond conversion, DMA support, and 16 input channels

- · 16 single-ended input channels
- 12-bit resolution (4096 counts)
- Three microsecond conversion time
- ±5 Volt or ±10 Volt input ranges
- · DMA and interrupt capabilities
- Auto channel increment mode
- STD 32®-compatible (16-bit data path)
- STD 80- and STD Z80-compatible (8-bit data path)
- +5 Volt single supply operation
- Extended temperature version available
- Software compatible with Analog Devices RTI-1265



VL-1295 High Speed Analog Input Card



VL-12CT96/97 Analog and Digital Input/Output Cards

VL-12CT96/97 Analog and Digital Input/Output Cards

- Extended temperature operation
- STD 32- (8- or 16-bit data path), STD 80-, and STD Z80-compatible

Analog Input:

- · Eight differential or 16 single-ended input channels
- 12-bit (VL-12CT96) or 16-bit (VL-12CT97) resolution
- ±5 Volt or ±10 Volt input ranges
- Current loop input option (four channels)
- · Selectable low pass filter
- 10 microsecond conversion time
- · Auto channel increment mode
- Interrupt support
- 5B01 compatible pinout

Analog Output:

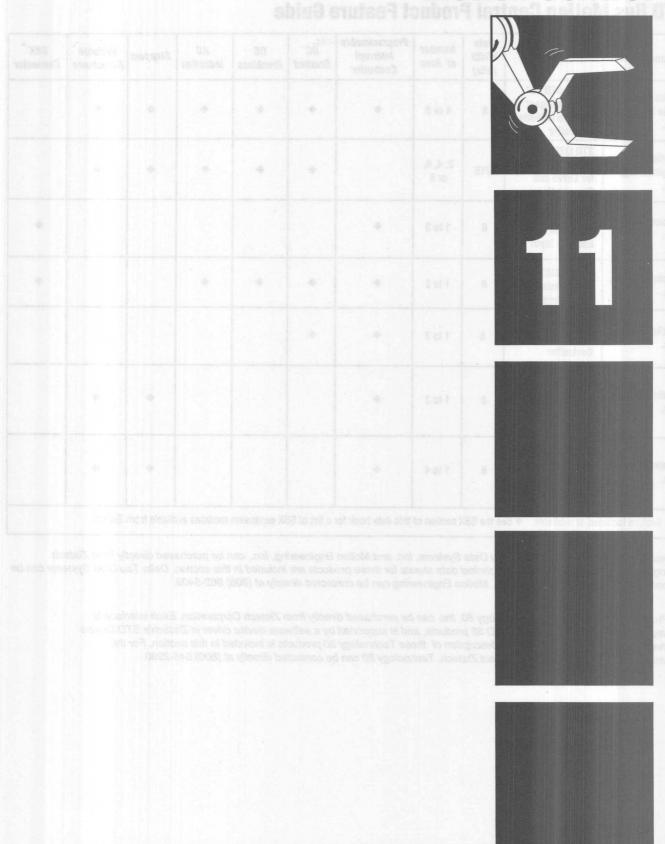
- Two output channels
- 12-bit resolution
- Independent ±5 Volt and ±10 Volt output ranges
- Current loop option (one channel)

Digital Input/Output

- 16 channel Opto 22-compatible
- Interrupt support
- Opto 22-compatible pinout
- TTL-compatible



STD Bus Motion Control



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STD Bus Motion Control Product Feature Guide

Manufacturer	Product	Data Width (bits)	Number of Axes	Programmable Interrupt Controller	DC Brushed	DC Brushless	AC Induction	Steppers	Variable Reluctance	SBX * Connecto
Delta Tau Data Systems, Inc.	PMAC-STD 32* STD Intelligent Multi-Axis Motion Controller	8	4 or 8	•	*	•	•	*	•	
Motion Engineering, Inc.	STD/DSP Series* Motion Controller for Servo and Stepper Motors	8/16	2, 4, 6, or 8		*	*	•	*	*	
Technology 80, Inc.	Model 4312C [†] Quadrature Encoder Input	8	1 to 3	•						•
Technology 80, Inc.	Model 4323/4333 [†] Servo Motor Controllers	8	1 to 2	•	*	+	*			•
Technology 80, Inc.	Model 4327B [†] Servo Motor Controller	8	1 to 2	•	•					
Technology 80, Inc.	Model 4335 [†] High Performance Stepper Motor Controller	8	1 to 2	•				٠	*	
Technology 80, Inc.	Model 4336 [†] High Performance Stepper Motor Controller	8	1 to 4	•				•	•	

Feature included of available from Ziatect

^{*} Products manufactured by Delta Tau Data Systems, Inc. and Motion Engineering, Inc., can be purchased directly from Ziatech Corporation or the manufacturer. Technical data sheets for these products are included in this section. Delta Tau Data Systems can be contacted directly at (818) 998-2095. Motion Engineering can be contacted directly at (805) 962-5409.

[†] Products manufactured by Technology 80, Inc. can be purchased directly from Ziatech Corporation. Each interface is compatible with Ziatech STD and STD 32 products, and is supported by a software device driver in Ziatech's STD Device Driver Package (STD DDP). A brief description of these Technology 80 products is included in this section. For the complete technical data sheets, contact Ziatech. Technology 80 can be contacted directly at (800) 545-2980.



PMAC-STD 32

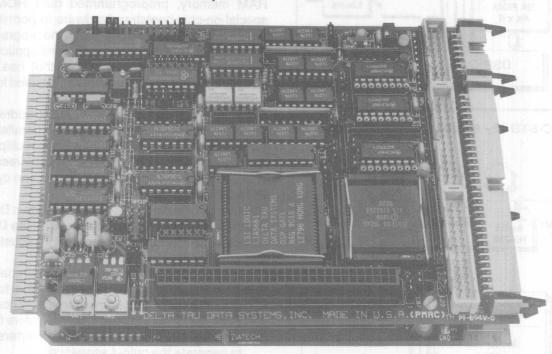
STD 32® Intelligent Multi-Axis Motion Controller

Intelligent PMAC card brings the highest level of performance and programmability to motion control on the STD 32® and STD buses

The PMAC-STD 32 is an intelligent Programmable Multi-Axis Controller (PMAC) for the STD 32 and STD Bus. Based on a high-performance, Digital Signal Processor (DSP) and gate array technology, the PMAC-STD 32 offers superior performance and programmability. It controls DC brush, DC brushless, AC induction, stepper, and variable reluctance motors.

The PMAC-STD 32 is a two-board set that contains a Digital Signal Processor, four axes of motion control, as well as encoder feedback and ancillary control functions. An optional third board may be added to support a total of eight axes. The PMAC-STD 32 is a joint development of Delta Tau Data Systems and Ziatech.

The board is based on the Motorola DSP56001 operating at 10 MIPS (millions of instructions per second). Its sophisticated motion control firmware uses a comprehensive series of functions that simplify many of the more complex motion control tasks.

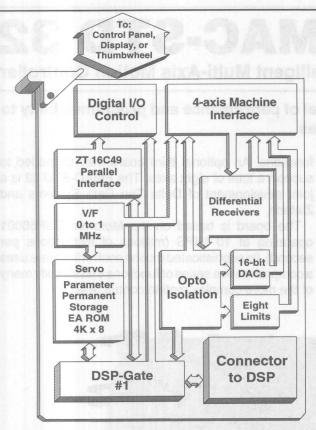


- Motorola DSP 56001 Digital Signal Processor
- Four or eight axes of motion control
- 20 MHz DSP clock (10 MIPS)
- Simple commands for complex motion control functions
- Controls DC brush, DC brushless, AC induction, stepper, and variable reluctance motors
- PID control loop with velocity and acceleration feed forward
- 10 MHz encoder rate
- · 48-bit position range (approx. 64 million counts)
- 16-bit DAC output resolution

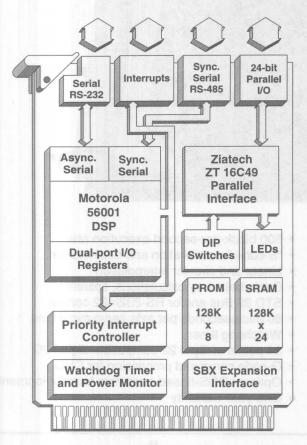
- 500 block-per-second execution rate
- "S-curve" acceleration and deceleration
- · Linear and circular interpolation
- · Cubic trajectory calculations, splines
- STD 32 Bus and/or RS-232/422 control
- 60 microseconds per axis servo cycle time
- Watchdog timer
- 24 points of Opto 22 compatible digital I/O
- G-code command processing for CNC
- Optional DOS-based executive for development
- One-year warranty







PMAC-STD 32 - Motion Control (Top (Board)



PMAC-STD 32 - Digital Signal Processor (Bottom Board)

Introduction

The PMAC-STD 32 combines powerful DSP technology, fourth generation motion control firmware, and Delta Tau Data's custom gate array IC . PMAC-STD 32 supports four output channels and four feedback channels. This capability can be expanded to eight output and feedback channels with the addition of another stackable motion control card. This configuration allows the PMAC to simultaneously command from 1 to 8 axes. Since each axis is completely independent, a single PMAC-STD 32 can command a single axis on each of 8 different machines, 8 axes of motion on 1 machine, or any combination in between.

DSP56001 Processor

The PMAC-STD 32 uses the Motorola DSP56001 running at 19.66 MHz. This Digital Signal Processor (DSP) chip features 512 words of full-speed on-chip RAM memory, preprogrammed data ROMs, and special on-chip bootstrap hardware to permit convenient loading of user programs into the program RAM. An important feature for motion control applications is the chip's pre-programmed ROM that has a four-quadrant sine wave look-up table that is used for phase commutation.

The data arithmetic logic unit (ALU), address logic units, and program controller operate in parallel. Therefore, an instruction prefetch, 24 x 24-bit multiplication, 56-bit addition, two data moves and two address pointer updates can execute in a single instruction cycle.

PMAC Custom Gate Array IC

A key factor in the PMAC's performance is Delta Tau Data's 10,000 gate IC, which interfaces the DSP processor to the machine under control. The custom gate array includes:

- · Four complete and identical encoder channels
- Four 16-bit, parallel/serial shift registers for receiving serial data from external A/D converters
- Four 16-bit, parallel/serial shift registers for sending data to the 16-bit D/A converters used to generate the output sequence
- 20 digital inputs used as encoder "C" channel, "home" flags, and "travel limits" etc.
- Eight general purpose digital outputs

Encoder channels handle the highest possible speeds needed for machine control. Besides speed, the encoder channels also provide the following special features:

- 10 MHz A/B quadrature encoder rate with 24-bit counters and registers
- Detection and reporting of illegal encoder transitions
- Digital noise filtering (necessary at high speeds)
- 1/T measurement, where time between encoder pulses is measured and used to calculate velocity (provides much smoother operation at low motor speeds)

PMAC-STD 32 Intelligent Multi-Axis Motion Controller

- An externally-triggered, 24-bit position, capture register that can be used to determine precise machine position upon occurrence of an external event
- A register that produces a pulse when the actual position equals the register's contents (eliminates "software" delays usually associated with this type of output)
- A phase capture register for exact determination of the motor's phase commutation as a function of rotational angle
- A control register that allows the CPU to control all modes of operation directly, including encoder multiplication factor, direction control, I/O polarity, etc.

Input Bandwidth

The PMAC-STD 32 is able to accept a 10 MHz maximum edge count rate with a digital filter. With the unique ability to use up to 5 bits of parallel binary data from the low-order, interpolated bits of high-resolution encoding devices, the PMAC can achieve effective input bandwiths of 320 MHz (10 MHz x 2⁵). In a typical laser application with 0.1 microinch resolution, this translates to a velocity of 32 inches per second.

Feedback

The PMAC is designed to take incremental A/B quadrature encoder feedback without additional accessories. However, the appropriate accessories enable resolvers, potentiometers, absolute encoders, magnetostrictive linear diplacement transducers, and laser interferometers to be interfaced to the PMAC. For calculation accuracy, and to avoid accumulated "round off" errors, the system uses a 24-bit up/down position register. This hardware counter is automatically extended in software to 48-bits. A software parameter allows position roll-over at a userspecified value: this is useful for controlling rotary axes.

Two methods are used by the PMAC to achieve subcount resolution with incremental encoding devices. The first is 1/T Decoding. Each encoder channel has two timing registers. Register 1 holds T1, the time between the last two encoder transitions. Velocity is proportional to this term. T2, timer Register 2 records the interval since the last transition. Fractional distance traveled since the last transition is estimated by dividing T2 by T1. This interpolation provides added smoothness to low speed moves. The second method of subcount resolution used by the PMAC is Parallel Fractional Feedback which accepts up to 5 bits of data in addition to the A/B quadrature edges. Data bits come directly from laser interferometers or as interpolated data from A/D conversion of analog encoders. Parallel fractional data is accepted both at rest and during programmed moves. If the A/D converter is unable to track the data during move sequences, the PMAC can change on the fly to 1/T subcount resolution.

Servo Loops

The PMAC-STD 32 provides both a PID and a Notch position servo loop filter with the following characteristics:

- A Proportional-Integral-Derivative (PID) control loop with individually adjustable gain terms
- A tunable notch filter from 1 to 500 Hz, usually used to damp a critical machine vibration frequency, if required
- Velocity and acceleration feedforward terms for reduction or elimination of following error
- Double position feedback loops, if required (one on the motor and one on the load), to control position accurately for a loosely-coupled load

Also included is software support for "auto tuning." It excites the load with impulse motions, evaluates and identifies the load characteristics and selects the optimal gain settings for the application.

Commutation

On-board commutation features of the PMAC provide support for the following motors:

- DC Brushless or AC Synchronous
- Variable (Switched) Reluctance
- AC Induction
- Stepper Motors

Commutation algorithms drive motor phases directly with only current loop bridges (transductance amplification) required in the amplifier. Two analog outputs per motor are required when the PMAC performs commutation, so a PMAC-STD 32-A2 with eight outputs can only control four motors if being used to provide commutation for all four motors. Using the PMAC to control commutation instead of the amplifier can significantly reduce amplifier cost and overall system cost. The torque performance and velocity smoothness of motors being commutated by the PMAC are also improved because the PMAC generates nearly perfect sinusoids.

Programming

The programming language used by the PMAC includes commands for: diagnostics and setup, personalization, and on-line system controls. Diagnostics and setup commands allow the user to perform comprehensive checks of the hardware. It also provides verification of machine, control panel, and I/O operations. Auto tuning and servo setup is available. There is also a "data gathering and display" mode that can store real-time data of position, following error, velocity, A/D input, D/A output, etc. The data can then be presented in tabular or graphic form for analysis.

Personalization commands set the servo parameters and axis operational characteristics, such as: following error limits, software travel limits, engineering units, backlash and deadband control, feedrates, encoder modes, commutation controls and other parameters that personalize each of the eight axes to their respective amplifiers, motors and intended task. The PMAC can use any of the A/D converters as position feedback or feedrate control. A special section allows the storing of tabular data for functions that include lead screw error, backlash, tool radius and tool offset compensation.

The on-line commands are a simple means to send

instructions to the PMAC for immediate execution. Included are: axis select, $jog \pm$, set zero position, start, stop, hold, quit, learn, etc.

The program buffer has special properties that enable the user to implement several "working" axis configurations. The eight axes can be independent of each other as if they are eight unrelated single-axis controllers, or conversely, configured as an eight-axis machine. This flexibility is accomplished by assigning a "coordinate system". Within each coordinate system, one to three "master axes" can be assigned, with the rest assigned as slave axes. A coordinate system may contain one to eight axes, so one to eight coordinate systems may be assigned.

Up to 256 programs may be stored in the PMAC, and any one may be executed by either of eight coordinate systems. This includes the case where one program is executed by eight coordinate systems synchronously or asynchronously.

A highly sophisticated DOS-based executive program is available, and is strongly recommended for industrial systems. This program greatly facilitates the installation, start-up, evaluation, servo loop tuning, and programming of the PMAC-STD 32.

A complete set of communications subroutines with source code are available from Delta Tau Data Systems for incorporation into host control programs as needed. Other programs are available which convert CAD drawings into PMAC programs. Training sessions are regularly conducted by Delta Tau Data Systems at its Southern California headquarters, or at customer sites. These classes provide valuable information and hands-on experience in a number of programming and hardware topics.

Background PLC Programs

While motion programs are running sequentially and synchronously in the foreground, the PMAC can run as many as 32 asynchronous PLC programs in the background. These programs perform many of the functions of a Programmable Logic Controller while sharing the same logical contructs of motion programs, yet are unable to command the motion of axes.

The PLC programs can monitor analog or digital inputs, set output values, send messages, monitor motion parameters, change gain values, and command motion Stop/Start sequences. PLC programs can even issue commands to the PMAC Motion Controller as if those commands came from the host processor itself. Typical PLC cycle times are 5 to 10 milliseconds.

Daisy Chaining Capability

The PMAC's software is limited to eight axes of control. Up to 16 PMACs may be daisy-chained, for a total of 128 axes of fully synchronized and interpolated controls with any type of amplifier and motor installed on any axis.

Interrupt Controller

An on-board interrupt controller allows the host computer to select, prioritize and mask the PMAC-STD 32's eight interrupt sources. These interrupt sources include an external source and several internal sources such as PLC program-generated interrupts on velocity, acceleration rates, etc.

Specifications

Electrical

Power Req. (4-axes)	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc=5.0V	in edition of	1.01A	2.01A
Aux Voltage, V _{aux+}	11.4V	12.0V	12.6V
Aux Current, V _{aux+} = 12.0V	tedigib a d	13mA	26mA
Aux Voltage, V _{aux} -	-12.6V	-12.0V	-11.4V
Aux Current V _{aux} - = -12.0V	agui tu tea Ma awalete	10mA	20mA

Power Req. (8-axes)	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	oni salistici	1.35A	2.7A
Aux Voltage, V _{aux+}	11.4V	12.0V	12.6V
Aux Current, V _{aux+} = 12.0V	areboos encodere	26mA	52mA
Aux Voltage, V _{aux} -	-12.6V	-12.0V	-11.4V
Aux Current V _{aux} - = -12.0V	abribot" !	20mA	40mA

- STD 32- and STD-80-compatible
- STD I/O Range: 16 ports located anywhere in 64 Kbyte address space on a 16 byte boundary

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 mechanical specifications
- Measures 4.5" (11.4cm) by 6.5" (16.5cm)
- Requires two STD slots (0.625" centers) for four axes, and three STD slots for eight axes
- Weight: 4-axis = 14.5 oz. (411.1g)
 8-axis = 21.0 oz. (595.5g)
- Connectors

Motion Control (top board):

- J1 JDISP 40 x 2 LCD display
- J2 JPAN control panel
- J3 JTHUMB thumbwheel inputs
- J4 JMACH1 machine 1
- J5 JS1 A to D inputs

DSP (bottom board):

- P1 114-pin STD 32 Bus card edge connector (0.625" spacing)
- J1 5-pin latching RS-232/485 serial I/O
- J2 10-pin latching frontplane interrupt connector

PMAC-STD 32 Intelligent Multi-Axis Motion Controller

- 20-pin latching RS-485 synchronous · J3 serial I/O
- J4 26-pin latching parallel I/O interface

Environmental	
Operating Temperature	0° to 65° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

STD 32 Compliance

 I/O Slave: EA8, SA8, I, IXP, IXL, ICA Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz)

Motion Control Specifications Servo Outputs

- ±10VDC at 16-bit resolution differential, optically
- · Can be used as general purpose DAC when not used in control loop

Servo Loop Cycle Time

(67% servo/33% background cycle)

- 55 microseconds · Per axis: Two axis: 110 microseconds
- Eight axis: 440 microseconds

Stepper Control

Accessory ACC-8D Option 2 (4 voltage-to-frequency [V/F] converters) is required for driving stepper motors

- Maximum step frequency: 10 kHz to 2.0 MHz (selectable)
- · Pulse and direction output can be cabled back to PMAC encoder (open loop)
- Separate encoder can be used for position verification (closed loop)

Kinematic Ranges

- · Position range: 36 bits, ±32 billion counts with programmable automatic rollover
- Velocity range: 0.0001 to 10,000,000 encoder counts/sec.

Position Feedback

- 10MHz A/B quadrature encoder with digital filtering
- 24-bit counter/registers
- Differential or single-ended inputs for A, B and C encoder channels with x1, x2, x4 count multiplication, or pulse and direction mode
- · Analog voltages (DC), resolvers, absolute encoders, and magnetostrictive devices can be used as feedback with optional accessories

Motion Profiles

- Velocity
- · Trapezoidal profile
- · S-curve acceleration and deceleration
- · Parabolic acceleration and deceleration

- Arbitrary moves:
 - Cubic Spline Mode
 - Position-Velocity-Time Mode

Ordering Information

PMAC-STD 32 Programmable Multi-Axis Controller (Delta Tau Data

Systems)

PMAC-STD 32-A1 Base model PMAC (4-axis unit)

Axis Options:

A1 4-Axis Motion Controller (two board set) A2 8-Axis Motion Controller (three board set)

General Accessories and Options:
Opt 9DA DOS-based software executive for host control of PMAC-STD 32 (used for startup, diagnostics and programming). Note: This option is highly recommended with the initial purchase.

Opt 8D Remote 4-channel terminal block for amp and motor connection w/16" cable

> Third phase generator for two Opt-1 PMAC-commutated motors, mounts to Acc 8D

Opt-2x Four Channel Voltage-to-Frequency (V to F) converter for stepper motor control, includes 16"(40.6cm) cable to Acc 8D (order one of six options below):

V to F converter for stepper motor control (10 kHz max)

- V to F converter for stepper motor control (50 kHz max)
- V to F converter for stepper motor control (100 kHz max)
- V to F converter for stepper motor control (500 kHz max)
- V to F converter for stepper motor control (1 MHz max)
- V to F converter for stepper motor control (2 MHz max)

Opt-4 Four Channel Hydraulic Valve/Motor Driver, 20W channel; with 16" cable to Opt 8D (30V max., 1.0A continuous, 2.0A peak)

Four Channel Hydraulic Valve/Motor Opt-4A Driver, 100W channel: with 16" cable to Opt 8D (48V max., 3.0A continuous, 5.0A peak)

Opt-6 Optically Isolated Encoder Inputs with four 16" cables to Opt 8D

(Continued on next page)

Accessories (Continued)

Cables (see Data Book cable section for details):

ZT 90068 40" (1m), digital I/O, 26- to 50-pin 40" (1m), digital I/O, 26- to ZT 2225

Industrial I/O Adapter Board

ZT 90099 40" (1m), RS-232 serial, 5- to 25-pin

ZT 90100 Frontplane interrupt

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

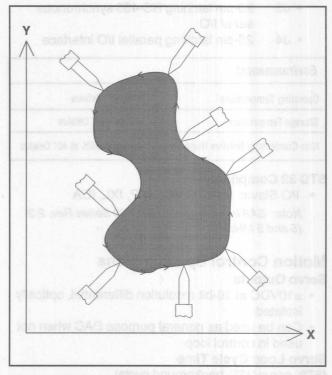


Figure 1. Motion control program illustration

Program Example

Rotary Tangent to X-Y System

This example shows how easy it is to keep a rotary tangent (or normal) to the movement of an X-Y system. The rotary axis is controlled by a separate program running sumultaneously that monitors X-Y variables. The X-Y part program does not need to know anything about the rotary axis—it is all automatic. (See *Figure 1.*)

```
*********Set-up and Definitions******
```

```
CLOSE
&1 #1->10000X
                             ; Motor 1 is X axis in Coordinate System 1
#2->10000Y
                             ; Motor 2 is Y axis in Coordinate System 1
                             ; Motor 3 is C axis in Coordinate System 2
&2 #3->40C
                             ; Do trig calculations in degrees
                             ; C axis rolls over every 14400 cts
T327=14400
                             ; Motor 1 present command position
M161->D:$0028
M163->D:$080B
                             ; Motor 1 target position
M261->D:$0064
                             ; Motor 2 present command position
M263->D:$08CB
                             ; Motor 2 target position
                             ; 1 count in Mx61, Mx63 units (div by 0 check)
```

*******Motion Program Text for Rotary Axis******

```
OPEN PROG 10 CLEAR
SPLINE1 TA20
                                                                                                                                                                                             ; Cubic spline segments of 20 msec
WHILE (P1>0)
                                                                                                                                                                                            ; As long as in this mode
 00=M163-M161
                                                                                                                                                                                             ; X target position - X current position
                                                                                                                                                                                            ; Y target position - Y current position
 01=M263-M261
  IF (ABS (Q0)>P10 OR ABS (Q1)>P10)
                                                                                                                                                                                            ; target pos <> current pos?
        Q2=ATAN2 (Q1)
                                                                                                                                                                                             ; Calculate angle - ATAN2 (Q1,Q0)
  ENDIF A MANAGEMENT OF SIGNO
 C(Q2)
                                                                                                                                                                                             ; Move rotary axis to new angle
ENDWHILE
CLOSE CLOSE CONTRACTOR OF THE CONTRACTOR OF THE
```





STD/DSP-Series

Motion Controller for Servo and Stepper Motors

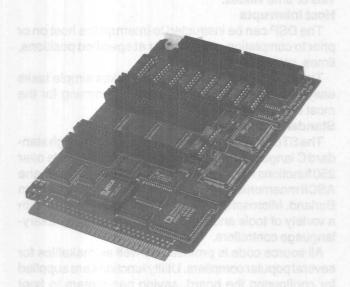
Motion Engineering's STD/DSP-Series brings high-performance motion control to the compact, rugged, STD 32[®] and STD buses

The STD/DSP controls both servos and steppers with one board and one programming interface. Motor types can even be mixed on a single board with the STD/DSP's full range of control and I/O capability.

Outputs include 16-bit resolution analog signals for brush and brushless servo motors and high-resolution step and direction signals for open-loop and closed-loop steppers. Inputs include incremental encoders, absolute encoders, analog sensors, laser interferometers and Temposonics™ transducers (optional).

A choice of PID, optional IIR or fuzzy logic control algorithms with velocity and acceleration feed-forward precisely control up to eight motors with update rates to 16 kHz.

Standard C function calls provide a fast, familiar programming interface. Operating system support includes: DOS, OS/2®, QNX® 2.x and 4, Lynx/OS, Microsoft Windows™ 3.1 and NT.



STD/DSP-X00 2105 DSP Memory 40 MHz A/D 16-bit D/A (Eight 12-bit **Analog Motor** Channels) Bus Signals Data Three 16-bit Counter/ **Pulse Generator Timers** Step/Direction Signals **Encoder Feedback 48 TTL Encoder input** I/O Lines

- One board controls:
 Brushless servos
 Brush servos
 Open-loop steppers
 Closed-loop steppers
- 2-, 4-, 6-, and 8-axis Models
- Standard C programming: Function libraries for DOS, Windows 3.1 and NT, QNX, Lynx/OS and OS/2 (sources included)

- Interpolation: 2-axis circular, 8-axis linear on independent coordinate systems
- · Continuous contouring
- Up to 48 user I/O lines, Opto 22 header
- Trapezoidal, parabolic and S-curve motion profiles
- Temposonics Interface (optional)
- 1 MHz communication from host to on-board shared memory





The STD/DSP features advanced hardware capable of accomplishing the most complex, and precise motion control applications.

High Precision Motor Commands

The STD/DSP uses a true 16-bit D/A converter and command update times from 60 to 330 microseconds (.3 to 16 kHz) to provide extremely smooth, accurate motion.

The accuracy of 0.08% at 1/2 RPS (equivalent to \pm 1 encoder count per DSP sample interval) was easily obtained with a standard Electrocraft BRU-200 servo motor with a 2,000-line encoder.

A 750 kHz voltage-to-frequency converter provides step and direction outputs in step rate increments of only 2 PPS for the fastest stepper accelerations possible.

Choice of Feedback Devices

The STD/DSP supports several position feedback devices with the standard firmware:

- Incremental encoder (Differential or single-ended)
- Absolute encoder
- · Laser interferometer (32-bit parallel)
- Analog sensor (LVDT or equivalent)

Device type can be software-selected and the selection stored on-board or set with C function calls.

Analog Inputs

Eight channels of single-ended (four channels differential) analog inputs are provided on each board for analog position feedback, joysticks, tensioners, etc. Either the DSP or the host processor can directly read the analog input values. Input voltage is 0 to 5 volt unipolar or ± 2.5 volt bipolar. Sample conversion rate is 75 kHz.

Servos and Steppers with One Board

Supporting servos and steppers with one board (in groups of two) minimizes programming time:

- · When a machine uses both servos and steppers
- · When motor types are changed for new designs

Optional Temposonics Support

A direct Temposonics interface can replace the step and direction outputs. This option sends a pulse to the transducer and gates the return pulse against a 40 MHz clock. The next pulse is sent automatically on return of the preceding pulse.

Dedicated and User I/O

The STD/DSP offers 72 bits of digital I/O to meet the requirements of most applications. Headers conform to Opto 22, Grayhill, and Gordos standards.

Dedicated I/O for each axis includes Positive/Negative Limits, Home and Amp Fault Inputs, and Amp Enable and In-Position Outputs. Additional dedicated inputs can be used to interrupt the DSP or the host CPU.

Each board also provides 48 (2-/4-axis models) or 24 bits (6-/8-axis models) of uncomitted user I/O. Note that user I/O pins are also used for interferometer and absolute encoder inputs when selected.

Torque Limiting

The maximum voltage (or step rate) output of the STD/DSP can be limited by a software command to a resolution of 16 bits.

Position Latching

When an input is sensed, the positions of all axes can be recorded in DSP memory in less than 1 microsecond per axis. The host can then read the positions at any time and reset the DSP for the next input.

Counter/Timer

The STD/DSP features user-programmable, threechannel, 16-bit 82C54 counter-timer. The chip can be programmed to interrupt the host at set position intervals or time values.

Host Interrupts

The DSP can be instructed to interrupt the host on or prior to completion of a move, or at specified positions, times, velocities, etc.

The STD/DPS's flexible design makes simple tasks easy to program, and simplifies programming for the most complex motion and I/O tasks.

Standard Languages

The STD/DSP controller is programmed through standard C language functions. The C libraries include over 250 functions with self documenting names—not arcane ASCII mnemonics. The use of standard languages from Borland, Microsoft, IBM or QNX provides the user with a variety of tools and support not found in proprietary-language controllers.

All source code is provided as well as makefiles for several popular compilers. Utility functions are supplied for configuring the board, saving parameters to boot memory, and performing diagnostics.

In addition, low level-functions are included for manipulating the DSP memory directly to perform special applications.

Support

MEI products are designed and our staff structured to provide the best software support possible.

STD/DSP-Series Motion Controller for Servo and Stepper Motors

MEI currently supports high-level programming in:

Borland C/C++®

MS-DOS

Microsoft C/C++®

Microsoft Windows™ 3 and NT

VisualBASIC for Windows

OS/2®

Borland PASCAL 7.0

QNX® 2 and 4

Microsoft QuickC

Lynx/OS

Visual C/C++

MEI maintains complete, fully licensed copies of each compiler/operating system to provide optimum support for customers programming efforts.

Specifications

Electrical

- Compatible with the STD 32 and STD-80 Bus specifications
- 8- or 16-bit data transfers
- Switch-selectable base address, I/O mapped
- Standard and slot-specific interrupts

Mechanical

- Compatible with STD 32 and STD-80 mechanical specifications
- Measures 4.5" (11.3cm) by 6.5" (16.5cm)
- Requires one STD slot (0.625" [1.59cm] centers)

Environmental	
Operating Temperature	0° to 60° Celsius
Non-Condensing Relative Humidity	20 to 95% at 40° Celsius

Servo Outputs

• ± 10VDC at 16-bit resolution

Servo Loop Update Rate

- User-programmable rate
- Maximum: 8.0 kHz (2 axes), 4.0 kHz (4 axes), 3.0 kHz (6 axes), 2.0 kHz (8 axes)
- Default: 1.25 kHz (all models)

Step Output

- Step/direction or clock up/clock down (optional)
- Maximum step frequency: 0.75 kHz with differential step outputs (non-linearity less than 1%)
- · ± or differential outputs at 20mA
- Pulse width: 50% duty cycle
- · Pulse rate ranges:

 Rate
 Resolution

 0 to 750kHz
 20 PPS

 0 to 200 KHz
 8 PPS

 0 to 50 KHz
 2 PPS

Kinematic Ranges

- Position range: 32-bit, ±2.15 billion counts (steps)
- Velocity range: 32-bit, ± 0.03 to ±6.7 million counts (steps)/sec.
- Acceleration range: 32-bit, ± 61 to 13.4 billion counts (steps)/sec².

Position Feedback

- Incremental encoder: 5.0 MHz, single-ended or differential RS-422 line receivers/digital filtering
- · Absolute encoder: up to 16-bit resolution
- Laser interferometer: 32-bit parallel interface
- Temposonics (optional): direct connection

Motion Profiles

- Trapezoidal profile
- · S-curve acceleration and deceleration
- · Parabolic acceleration and deceleration
- Velocity

Dedicated I/O (per axis)

- TTL-compatible, 4.0mA drive on outputs
- Inputs:

Positive and negative limits Home

Amp-fault

· Outputs:

In-position

Amp-enable

User I/O (per board):

- 2-/4-axis models: 48 lines; 6-/8-axis models: 24 lines
- TTL-compatible, 4.0mA drive on outputs, 82C55 ICs
- Direct access from host CPU

Analog Inputs (per board)

- 12-bit resolution, ± 1/2 LSB linearity
- 8-channel multiplexed inputs with track-and-hold
- Software configurable for 4-channel differential mode
- 75 kHz sampling rate
- Software configurable: unipolar (0 to 5V) or bipolar (± 2.5V)
- · Direct access from host processor

82C54 Counter/Timer

- Three independent 16-bit counters
- Six programmable counter modes
- Time base: 10 MHz, 1.25 MHz or user-supplied
- Programmable host processor interrupt generation

Construction

- 6-layer plus power and ground
- · Full SMT, double-sided
- Each board bed of nails and full function is tested with 48-hour burn-in





STD/DSP-Series Motion Controller for Servo and Stepper Motors

Power Requirements:

+5V lcc = 2.4A max

+12V lcc = 60mA max

-12V lcc = 60mA max

Ordering Information

STD/DSP-X00

Motion Controller for Servo and Stepper Motors (X = 2,4. 6, or 8 axes)

The following program demonstrates coordinated motion with the STD/DSP card. The program uses two axes to draw a box, then an inscribed circle. After that, a file called 'CONTOUR.DAT' is read and executed.

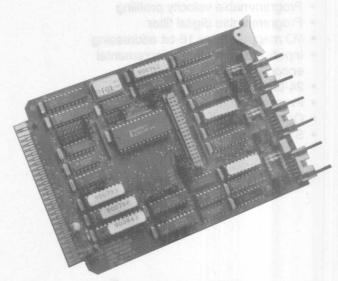
```
include "pcdsp.h"
   include < stdio.h>
   define CONTOUR FILE "contour.dat"
void main (void)
  FILE * contour file ;
double x, y;
set move speed(8000.0);
   set_move_accel(80000.0);
   start point list();
   move 2(5000.0, 5000.0);
   move_2(50000.0, 50000.0);
   move_2(0,50000.0);
   move_2(0, 0);
   move 2(10000.0,10000.0);
   arc_2(15000.0,10000.0,360.0);/*circle,rad.=5000cts.*/
   move 2(0, 0);
   contour file = fopen (CONTOUR FILE, "r"); /*readdata
file.*/
   while (fscanf(contour_file, "%lf, %lf", &x, &y) == 2)
  move_2(x, y);
   fclose(contour_file);
   end_point_list();
   move_2(0, 0);
   start_motion(); /* start motion and display position.
   while (! (axis_done(0) && axis_done(1)));
   { get position(0, &x);
       get_position(1, &y);
       printf("X: %12.01f Y: %12.01f\r", x, y);
 0.50000
                                      100000,50000
                 cicle at 50000.100000
                                         100000.0
```

STD Bus Motion Control Products

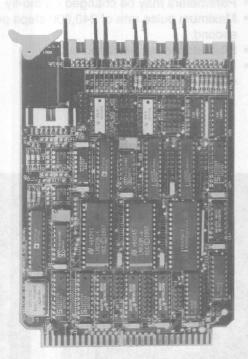
from Technology 80, Inc.

Model 4312C Quadrature Encoder Input (1-3 Axes)

- Three pre-settable 24-bit counters
- 1.2 MHz Quadrature input pulse rate
- Selectable sample clock frequency (up to 10 MHz)
- Interrupts on index pulse, and overflow/underflow, or compare value match
- · Interrupt masking
- STD 32® connector



4312C Quadrature Encoder Input



4323 Servo Motor Controller

Model 4323 and 4333 Servo Motor Controllers (1-2 Axes)

- · Position and velocity control
- · Programmable digital PID filter
- Programmable real-time interrupts
- On-the-fly change of target velocity and position
- 32-bit position, velocity, and acceleration registers
- Inputs for one incremental encoder per axis
- Three opto-isolated external interrupt inputs per axis
- Speed range of .045 to 1,000,000 encoder counts per second
- 12-bit ±10 Volt output (4323 only)
- 7-bit PWM plus sign output (4333 only)



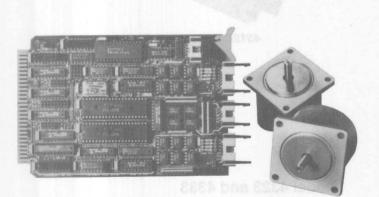
Telephone (800) 545-2980



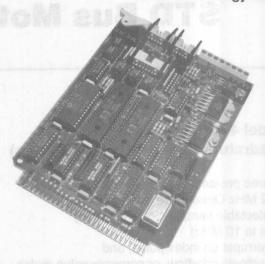
from Technology 80, Inc.

Model 4327B Servo Motor Controller (1-2 Axes)

- Position control
- Velocity control
- · Programmable velocity profiling
- · Programmable digital filter
- I/O mapped 8-, or 16-bit addressing
- Inputs and decoder for incremental encoder signals
- · 24-bit position counter
- · Programmable interrupt control
- On-board PWM amplifiers
- STD 32[®] connector



4335 High Performance Stepper Motor Controller



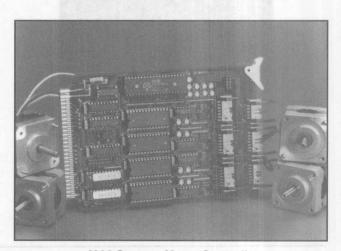
4327B Servo Motor Controller

Model 4335 High Performance Stepper Motor Controller (1-2 Axes)

- · Independent, intelligent controller each axis
- Programmable acceleration and deceleration (1 to 4,190,208 pulses/sec/sec)
- · Programmable velocity profiling
- · Opto-isolated drive outputs and limit inputs
- · Parameters may be changed on-the-fly
- Maximum pulse rate of 240,000 steps per second
- · 8-bit latched opto-isolated output
- Software driver routines and "Profile" demonstration software (optional)

Model 4336 Stepper Motor Controller (4 Axes)

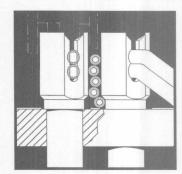
- Independent, intelligent controller each axis
- Maximum pulse rate of 150,000 steps per second
- Programmable acceleration and deceleration
- · Parameters may be changed on-the-fly
- Eight general purpose open collector outputs and four inputs
- Five inputs/axis (two end limit, two ramp limits, one home)
- On-board interrupt controller with three 16-bit counter/timers
- STD 32® connector



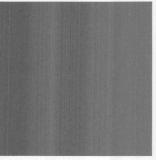
4336 Stepper Motor Controller



STD Bus Prototyping



12





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readwire Frototype
b Extender Card
a SEX Speedwire

12

Inside This Section

- ZT 8871 Wirewrap Prototype Card
- ZT 8970 STD 32 Speedwire Prototype Card
- ZT 8971 STD 32 Bus Extender Card
- ZT eSBX70 Extended SBX Speedwire Prototype Card



STD 32 Developer's Kit

Toolkit for STD 32® Developers

STD 32 Developer's Kit speeds the design of STD 32-compatible CPU and I/O boards

The STD 32 Developer's Kit provides useful information and resources for developers of STD 32 products.

The STD 32 Developer's Kit Contents

The Developer's Kit provides specifications, licenses, and a software diskette with several Computer Aided Design (CAD) diagrams to simplify STD 32 board design. A copy of the license agreement is included for STD 32 manufacturers and users*.

The Developer's Kit includes:

- The STD 32 Bus Specification (and applicable addendums)
- STD 32 License Agreement
- STD 32 Design Kit Software Package, including an OrCAD schematic, AutoCAD mechanicals, STD 32 finger pattern Gerber files, a design example, and PAL equations
- STD 32 finger pattern film (1X and 2X)
- STD 32 manufacturer data sheets
- STD 32 fabrication drawing

Design Kit Software Package

The software package provides useful information for CAD environments, including an OrCAD schematic file. This file represents an actual design example in the specification and may be used as a template for new designs, or for reference.

AutoCAD Mechanicals

The mechanical figures found within the STD 32 Bus Specification are in AutoCAD format for design reference. These files can be used as templates for mechanical dimensioning of specific boards.

STD 32 Finger Pattern Gerber Files

The films included with the design kit were generated from "Gerber" (.GBR) files on the Design Kit software diskette and represent the STD 32 finger pattern. The Gerber files directory includes a .GAP file and a design file for use with the popular PCGERBER and ECAM products from CAD Solutions. The Gerber files are useful for design verification or for incorporating the STD 32 finger pattern into existing designs.

Design Example PAL Equations

Source and documentation files for the design example PAL files are also included. Source files are formatted as "Minc" compatible and the equations may be adapted for different compilers.

STD 32 Manufacturer Data Sheets

All available data sheets for STD 32 products are included for reference. Contact the STD 32 Special Interest Group (SIG 32) at (800) 733-2111 for new product data sheets.

Ordering Information

STD 32 Developer's Kit

STD 32 Bus Specification, license, design software package, finger pattern film, data sheets, mechanical drawings



^{*}A manufacturer builds STD 32 boards and offers them for resale. A user designs application-specific STD 32 boards that are not intended for resale.

STD 32 Developer's Kit



STD 32 Developer's Kit speeds the design of STD 32-compatible CPU and I/C mounds

AutoCAD Mechanicals

The mechanical figures found within the CD32 Bus Specification are in AutoCAD format for a sign reference. These titles can be used as its cylates for

mechanical dimensioning of specific box STD 32 Finger Pattern Gerher Files

from "Gerber" (GBR) files on the Design 10 software diskette and represent the STD 92 finger in term. The Gerber files directory includes a GAP file for use with the popular PCGERBE and ECAM.

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Ordaring Information

STD 32 Developer's Kit STD 82 But specification, license sign colleges as una flor

software palling de ligo, fin pation film, data shed medisoloat crowings The STDE 2.0 syeloper's lidt provides useful information and rescuruse for developers of STD 32 products.

The STD ::: Developer's Kit

The Develop at a Kitprovides specifications, iconses, and a software siskette with several Computer Aided Design (CAD) displaces to simplify STD 32 board design. A good of the license agreement is included for STD 32 manufacturers and users*.

The STD 32 Bus Specification (and

• STD 32 Leanse Agreement

 STD 32 Design l'OtSoftware Package, including an Or CAD achiement, AutoCAD machanicals, STD 32 littorer boulem Gedner files, a design example, and

STD 32 Inger patient film (1X and 2X

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Design Kit Software Package

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A manufacier ce cultiff \$10.32 boards and offers from for resele. A ser designs most silentespecific \$70.32 boards that are not interced at respire.

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ZIATECH

ZT 8871

STD Wirewrap Prototype Card

Prototype card's convenient features make I/O interface design simpler and more efficient for STD Bus users

The ZT 8871 STD Wirewrap Prototype Card provides system designers with an efficient means for developing their own STD I/O boards.

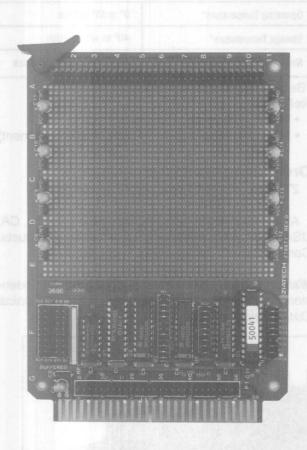
For user convenience, wirewrap posts are preinstalled on all 56 STD signals. Traces connect components directly to wirewrap posts, eliminating the cumbersome task of soldering wires onto leads.

The user's design work is further reduced through an on-board wait-state generator and I/O decoding

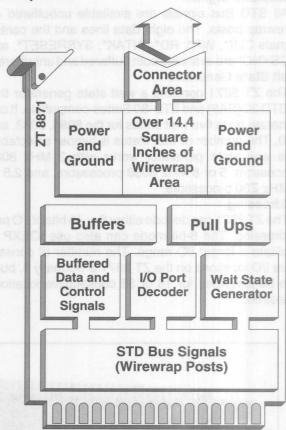
circuitry compatible with 8088/8086, 8085, and Z80 processors.

The prototype card gives system integrators more flexibility in implementing their designs because all STD signals are unbuffered, while data lines and certain control signals are available both buffered and unbuffered.

Other features further simplify the design of custom I/O boards, which are found in an estimated 50% of all STD systems.



- Processor-independent
- Over 14 square inches (over 36 square cm) of wirewrap area
- · Decoupled power and ground bus
- All STD Bus signals available unbuffered
- Data lines and control signals available buffered and unbuffered



- Pre-installed wirewrap posts
- On-board wait state generator (STD 32[®] [SA8], STD-80 Series and Z80 compatible)
- Buffers, pull-ups, and open-collector gates
- Special connector area for discrete components and connectors
- Burned in at 55°C and tested for reliability



Wirewrap Area

The ZT 8871 provides over 14 square inches (over 36 square cm) of wirewrap area surrounded by a decoupled power and ground bus. The bus layout is symmetrical for improved current flow. The wirewrap area is sized for 0.025 inch (0.6mm) square posts on a 0.1 inch (2.5mm) by 0.1 inch (2.5mm) grid.

Connector Area

One end of the wirewrap area has a special layout for discrete components and connectors. The first two rows of holes are open for installation of these discretes and connectors. The next two rows have preinstalled wirewrap posts configured to match the first two rows on a hole-for-hole basis, eliminating the need to solder wires to the part leads. The user can simply solder in components and then wirewrap to them.

Backplane Signals

All STD Bus signals are available unbuffered on wirewrap posts. The eight data lines and the control signals CLK*, WR*, RD*, INTAK*, SYSRESET*, and MCSYNC* are available both buffered and unbuffered.

Wait State Generator

The ZT 8871 contains a wait state generator that is STD 32 (SA8) and STD-80 Series-compatible. It can generate up to five wait states for the 8085, 8088, and Z80. The number of wait states is jumper selectable. The wait state generator works with 3 MHz 8085 processors, 5 or 8 MHz 8088 processors, and 2.5 or 4 MHz Z80 processors.

Addressing

The ZT 8871 can decode either 8 or 16 bits of I/O port addressing. The 8-bit mode can also use IOEXP to facilitate a larger I/O range. The number of consecutive I/O locations on the ZT 8871 is normally 8, but it can be jumpered for 16 or 32 consecutive locations if desired.

On-board Devices

Several devices are provided by the ZT 8871 to aid in prototyping, including non-inverting buffers, open-collector gates, and pull-ups.

Specifications

Electrical

Processor-independent

Power Req.	Min.	Тур.	Max.
Supply Voltage, VCC	4.75V	5.00V	5.25V
Supply Current, VCC = 5.0V	alsnpla (II	0.26A	0.40A

Mechanical

Size- and backplane-compatible with STD-80 mechanical specification

Environmental		
Operating Temperature*	0° to 65° Celsius	
Storage Temperature*	-40° to +85° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

*Before loading user components

Reliability

MTBF: 176 years

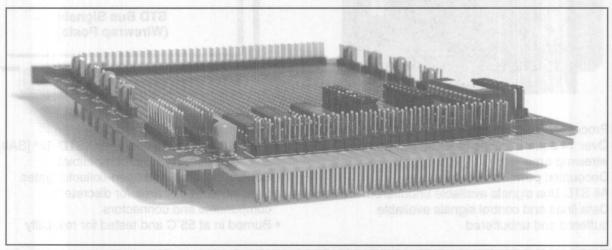
MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8871 STD Wirewrap Prototype Card

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for some products. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.



Ziatech's ZT 8871 STD Wirewrap Prototype Card features pre-installed wirewrap posts.



STD32°

ZT 8970

STD 32® Speedwire Prototype Card

A reusable, high-capacity, double-length Speedwire™ prototyping card that provides easy access to STD 32 and STD Bus backplane signals for simple and complex designs

The ZT 8970 Speedwire Prototype Card provides system designers with a high-capacity, double-length board to implement STD 32 and STD Bus designs.

The reusable benefits of Speedwire, along with speed improvement over wirewrap implementations, provide system designers with a cost-effective means for prototyping I/O and memory designs for the STD Bus.

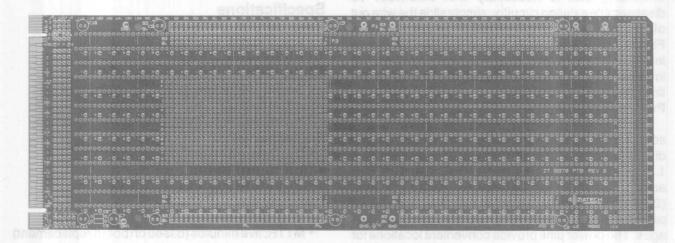
The base board does not include Speedwire pins and can be used for one-time designs where wirewrap or solder connections are acceptable. The board with Speedwire pins installed is recommended for those doing several designs.

For user convenience, Speedwire locations are available for all backplane signals, power supplies, frontplane interface, as well as optional interboard connectors.

Traces connect all backplane signals to Speedwire locations on a one-to-one basis to eliminate the cumbersome task of soldering wires onto leads.

For designs that require more than one board, the ZT 8970 is stackable with another ZT 8970 board by utilizing four 64-pin connector areas, for a total of 256 interboard signals. The reversible feature of the interboard connectors enables the top and bottom boards to be switched, allowing access for diagnostic devices.

Other features include: seven ground turret post locations for probe grounding; bulk capacitor locations for +5V, +12V, and -12V; bypass capacitor locations for +12V and -12V; frontplane access to +12V, -12V, and AUX GND; 126-pin frontplane connector area with corresponding Speedwire locations, and a convenient row-column matrix for wire-list notation.



- Efficient BICC-VERO Speedwire option
- Reusable
- · Double-length capacity
- 11.3" (28.7cm) x 3.6" (9.1cm) Prototyping area (41 square inches [261.2 square cm])
- 1.9" (4.8cm) x 3.4" (8.6cm) Pin Grid Array (PGA)
- · Stackable with other ZT 8970 prototype cards
- Bulk capacitor locations

- Decoupling capacitor locations
- · One-to-one backplane Speedwire locations
- 126-pin frontplane connector area with corresponding Speedwire locations
- +5V and ground Speedwire locations within prototyping area
- STD 32- and STD-compatible
- Frontplane access to +12V, -12V, and AUX GND
- · Row-column matrix for wire-list notation



Speedwire

The Speedwire terminals used on the ZT 8970 were developed by BICC-VERO as an alternative to cumbersome wirewrap posts. The terminals are pressfit into the ZT 8970, allowing standard IC leads to be inserted from the component side. On the circuit side, the terminal accepts 30 AWG wire, making contact via insulation displacement. An optional wiring pen allows simple point-to-point connection by pressing the tip down over the exposed Speedwire terminal.

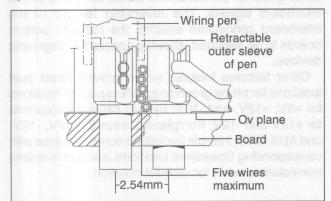


Figure 1. Speedwire terminal

Speedwire terminals are easily reusable, without the unwinding that is necessary with wirewrap. To disassemble existing circuitry, simply slide the wire out of the insulation displacement connection (see Figure 1). Existing circuitry can be modified by tagging into a net with an additional wire. With practice, the initial wiring and modifications can be done five to ten times faster than wirewrap.

Prototyping Area

The ZT 8970 provides 41 square inches (261.2 square cm) of prototyping area, with +5V and ground distributed on 0.3" (7.6mm) centers for easy access. A 1.9" (48.3mm) by 3.4" (86.4mm) Pin Grid Array (PGA) area is provided with Speedwire locations on 0.1" (2.5mm) centers. This allows an easy interface to PGA packages, EPROM, RAM, and other non-DIP packages. The power pins provide convenient locations for bypass capacitors for each IC. The backplane signals and frontplane connector signals are available at Speedwire locations for solderless interfacing. Three rows of 42 pins are available for frontplane connections.

Bulk Capacitor and Bypass Capacitor Locations

The ZT 8970 provides locations for bulk capacitors for +5V (seven locations), +12V (one location), and -12V (one location). These, in addition to +5V and ground power planes, ensure a stable voltage supply throughout the prototyping area. Bypass locations for +12V and -12V for high-frequency decoupling are provided near the backplane and at the frontplane access locations. Standard 0.3" (7.6mm) DIP capacitors may be used in these locations.

High-frequency +5V bypass is accomplished by utilizing the Speedwire locations for +5V and ground within the prototyping area. This provides close bypass for each IC at its power connection. The above features help provide stable power for high-performance applications with fast edge rates.

STD 32 and STD Signal Support

The ZT 8970 provides full backplane access to all STD 32 signals. STD signals are a subset of STD 32. This means that the ZT 8970 can be used to design applications for either bus architecture. Contact Ziatech for information regarding the powerful benefits of STD 32.

ZT 8970-B1

The ZT 8970-B1 supports all STD 32 and STD Standard Architecture (SA) designs and STD 32 Extended Architecture (EA) I/O designs. Designers of STD I/O boards (EA or SA) will use the ZT 8970-B1. This board does not have the EA memory extension fingers. The STD 32 Specification fully describes the differences between SA and EA transfers.

ZT 8970-B2

The ZT 8970-B2 has the EA memory extension fingers for CPU and memory designs that take advantage of the higher performance STD 32 EA memory transfers. CPU designs that utilize just SA transfers can be implemented using the ZT 8970-B1.

Specifications

Electrical

Power supply requirements depend on the prototype application

Mechanical

- Double length form factor (13.0" [33cm] x 4.5" [11.4cm])
- Pin-compatible with STD 32 Bus and STD-80

Environmental

• Dependent on prototype application

STD 32 Compliance

Supports all compliance possibilities

Reliability

• MTBF: 85 years

MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8970 STD 32 Speedwire Prototype Card
-B1 114-pin STD 32 (most applications)
-B2 CPU and memory board designs

(Contact Ziatech for further information)

Must choose from the following pins:
P1 No Speedwire pins

P2 Speedwire pins installed

Accessories

ZT 98036 Interboard connectors (Eight 64-pin

stackable connectors)

ZT 98037 Speedwire Prototyping Pen with

59.1' (18m) of 30 AWG wire





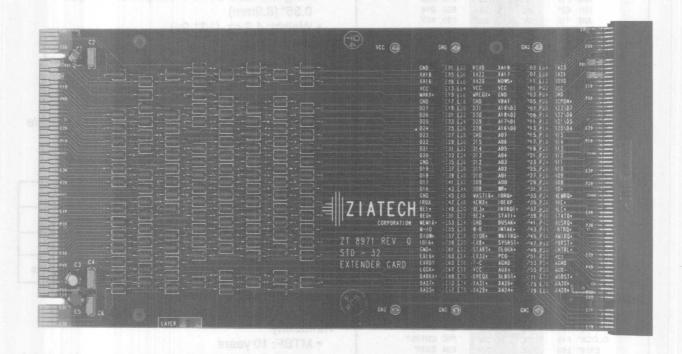
ZT 8971

STD 32® Bus Extender Card

Versatile, high-quality extender card provides system designers with simple and complete access to board-level products

The ZT 8971 provides system designers with a high-quality, four-layer extender card compatible with both STD 32® and STD Bus card cages, and board-level products. The extender card edge connector contains address extensions for the STD 32 Bus which can be

easily removed for use in STD backplanes. Features include terminated signal paths, power and ground turret posts for connecting logic probes, logic analyzers, and oscilloscope probe grounds.



- Four-layer construction assures minimum signal degradation
- 136-pin, STD 32-compatible backplane connector with address extensions
- Backplane decoupling and bypass capacitors
- 136-pin, STD 32- and STD-compatible frontplane connector allows both new and old card formats
- · On-board series ferrite terminations
- All backplane signals available at posts for logic analyzer or oscilloscope attachment; all posts are labeled with signal name and pin number
- V_{CC} and ground available at turret posts



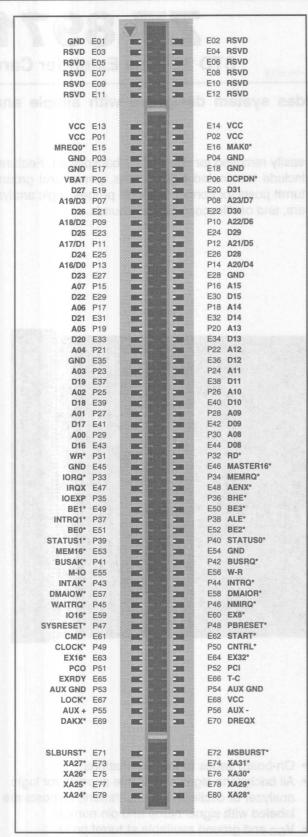


Figure 1. ZT 8971 Frontplane connector showing STD 32 pinouts

The ZT 8971 meets all STD 32 Extended Architecture and STD Standard Architecture compliance levels. Thus, it supports all properly designed STD board-level products.

It extends a single card 8.7" (22.1cm) beyond the normal seating plane.

Specifications

Signal Interface

 All active signals are inductively coupled with ferrite beads to reduce overshoot and dampen high frequency noise.

Electrical

• The ZT 8971 consumes no power

Mechanical

- STD form factor
- Measures 4.5" (11.4cm) x 9.0" (16.5cm)
- Height measured from component surface: 0.35" (8.9mm)
- Weight: 4.3 oz. (121.9g)
- Connectors

E/P: 136-pin STD 32-compatible card

edge connector on 0.625" (15.90mm) centers

This connector attaches to STD 32 address extensions and can be modified to be compatible with STD-80 compatible connectors.

Cables

Requires no cables

Environmental		
Operating Temperature	-40° to +85° Celsius	
Storage Temperature	-55° to +105° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

STD 32 Compliance Levels

• Meets all STD 32 compliance levels

Reliability

· MTBF: 10 years

MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8971 STD 32 Extender Card

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.



ZT eSBX70

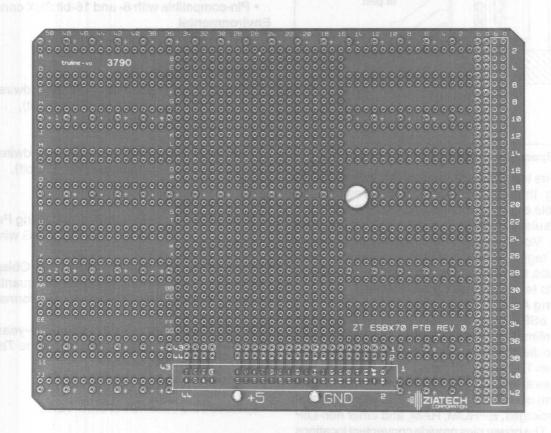
Extended SBX Speedwire Prototype Card

A reusable, high-capacity, full-size STD Speedwire™ prototyping card that provides easy access to SBX signals for simple and complex designs

The ZT eSBX70 Speedwire Prototype Card provides system designers with a high-capacity, full-size STD card to implement SBX designs. The reusable feature of Speedwire, combined with the speed improvement over wirewrap implementations, provides system designers with a cost-effective means for prototyping SBX I/O designs for the STD Bus.

For user convenience, Speedwire locations are available for all SBX signals, power supplies, and frontplane locations.

Other features include: turret post locations for $V_{\rm CC}$ and ground, bypass capacitor locations for +5 Volt, an 86-pin frontplane connector area with corresponding Speedwire locations, and a convenient row-column matrix for wire list notation.



- Efficient BICC-VERO Speedwire implementation
- Reusable
- Full STD card capacity
- Two 1.9" x 1.5" (4.8cm x 3.8cm) Pin Grid Array (PGA) Speedwire locations
- · 8- or 16-bit support
- Decoupling/bulk capacitor locations

- One-to-one backplane Speedwire locations
- Access to all SBX signals
- 86-pin frontplane connector area with corresponding Speedwire locations
- +5V and ground Speedwire locations within prototyping area
- · Row-column matrix for wire list notation



Functional Considerations Speedwire

The Speedwire terminals used on the ZT eSBX70 were developed by BICC-VERO as an alternative to cumbersome wirewrap posts. The terminals are pressfit into the ZT eSBX70, allowing a standard IC lead to be inserted from the component side. On the circuit side, the terminal accepts 30 AWG wire, making contact via insulation displacement. An optional wiring pen provides a simple point-to-point connection mechanism by simply pressing the tip down over the exposed Speedwire terminal.

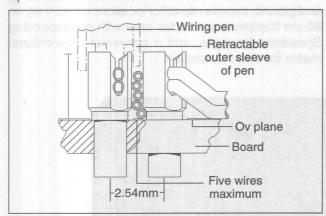


Figure 1. Speedwire terminal

Speedwire terminals are easily reusable, without the unwinding that is necessary with wirewrap. To disassemble existing circuitry simply slide the wire out of the insulation displacement connection (see Figure 1). Modifications to existing circuitry are as simple as tagging into a net with an additional wire. With practice, the initial wiring and modifications can be done five to ten times faster than wirewrap.

Prototyping Area

The ZT eSBX70 provides 25 square inches (161 square centimeters) of prototyping area, with +5 Volt and ground distributed on 0.3" (0.8cm) centers for easy access. Two 1.9" x 1.5" (4.8cm x 3.8cm) Pin Grid Array (PGA) areas are provided with Speedwire locations on 0.1" (0.3cm) centers. This allows for an easy interface to PGA packages, EPROM, RAM, and other non-DIP packages. The power pins provide convenient locations for bypass capacitors for each IC. The SBX signals are available at Speedwire locations for solderless interfacing. Two rows of 43 pins are available for frontplane connections.

Bulk Capacitor and Bypass Capacitor Locations

The ZT eSBX70 provides locations for bypass capacitors for +5 Volt. Bulk capacitors may also be used at these locations. These, in addition to +5 Volt and ground power planes, will ensure a stable voltage supply throughout the prototyping area. Standard 0.3" (0.8cm) DIP capacitors may be used in these locations. SBX Signal Support

Full connector access to all SBX signals is provided.

Specifications

Electrical

Power Supply Requirements:
 Dependent on prototype application

Mechanical

- STD card size of 5.75" x 4.5" (14.6cm x 11.4cm)
- Pin-compatible with 8- and 16-bit SBX connectors

Environmental

Dependent on prototype application

Ordering Information

ZT eSBX70-B1 Extended SBX Speedwire

Prototype Card (8-bit), manual included

ZT eSBX70-B2 Extended SBX Speedwire

Prototype Card (16-bit), manual included

Accessories

ZT 98037 Speedwire Prototyping Pen with

18 meters of 30 AWG wire

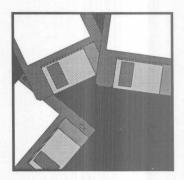
All products are shipped FOB San Luis Obispo, CA, USA.OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.

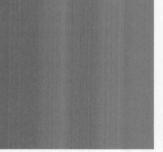
Speedwire is a trademark of BICC-VERO.



STD Bus Software



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Inside This Section

- · STD ROM
- Application Note #7: Developing a ROM-based System
- · STD DOS
- Application Note #12: Developing STD DOS-based Control System Applications
- STD Device Driver Package (STD DDP)
- DOS Multiprocessing Extension (DOS MPX)
- STD 32-QNX: QNX Real-Time Multitasking Operating System on STD 32 Computers
- STAR-QNX: The Multitasking QNX Operating System on the Multiprocessing STD 32 STAR SYSTEM



STD ROM

Development System



STD ROM[™] provides user-friendly programming and debugging tools for embedded STD Bus development

STD ROM is designed for users who want to develop an STD ROM-based application on their PC using high-level languages like C, but don't want the cost and overhead of an operating system in their final application.

STD ROM combines Paradigm DEBUG/RT™, which provides a user-friendly environment, and a Ziatech PDREMOTE/ROM EPROM, which allows remote debugging of an STD system from a PC.

The development system does not require extra STD peripheral and

memory cards because it uses the PC for its DOS services. This lets the user program in the exact configuration of the final application.

Included in this package are Paradigm DEBUG/RT and LOCATE™, a Ziatech PDREMOTE/ROM EPROM, support software, and RAM. (Additional memory can be added if necessary.) Also included are STD DDP (STD Device Driver Package) and start-up modules which eliminate MS-DOS requirements in a compiled program.

- Fast Development of "non-DOS" STD Target Systems
- Supports Ziatech Single Board STD Bus Computers
- Complete Debugger and Locator
- Friendly User Interface
- Compatible with High-level Languages, such as C, C++, and Assembly
- C Device Driver Included
- Allows Remote STD Programming and Debugging on a PC
- Hardware-resident EPROM



A Tool for Embedded Systems

STD ROM is designed for users who want to develop an STD "native" application on their PC using high-level languages. It allows application code to be debugged and targetted to EPROM quickly and easily. STD ROM Features

A typical STD ROM Development System includes:

- A Ziatech Single Board Computer
- Paradigm's DEBUG/RT and LOCATE
- PDREMOTE/ROM EPROM
- Compiler Startup Modules
- · STD DDP
- RAM
- Serial Cable
- Full Hardware and Software Documentation

The STD ROM package links the single-board computer to Paradigm DEBUG/RT through the use of PDREMOTE/ROM and simplifies the actual "ROMing" process while maintaining compatibility with many development tools. Development efforts are assisted by the make files and configuration files provided with the system. Example software is also included to build the application in a minimal amount of time.

High-level Language Support

Support is provided for high-level language development on several popular compilers including:

- Microsoft C®/C++ and Assembler
- Borland Turbo C®, Turbo C++®, and Assembler
- · Borland C++

The use of the Paradigm DEBUG/RT package on a host PC linked to an STD Target System via PDREMOTE/ROM provides a user with full debugging features, including:

- Source-level debugging
- Single stepping
- Complex breakpoints with multiple conditions and actions
- Pull-down menus
- Easy-to-use data views including watches, inspectors, dynamic operation, and more
- Log windows to record and save all or part of the debugging session
- Memory boundary detection

The debugger also supports high-level math coprocessor debugging down to the register level. STD ROM requires little user training because it is based on Paradigm DEBUG/RT. Paradigm Systems has licensed Borland's award-winning Turbo Debugger and enhanced it to create custom implementations exclusively for embedded system debugging.

The entire STD ROM package is well-documented for efficient implementation.

PDREMOTE/ROM Interface

The link to the Ziatech line of STD Bus-based single board computers is provided through the PDREMOTE/ROM EPROM. This interface provides a high-speed

STD ROM - The Need

For many years, control system development for ROM-based embedded applications was a relatively simple exercise. These systems consisted of straightforward I/O control and monitoring tasks, requiring only Assembly language and simple tools to convert an application into a "ROMable" image.

Today, the complexity of embedded systems has risen dramatically. Many now require the use of high-level languages, graphics support packages, networking, and even complex numerical processing capabilities.

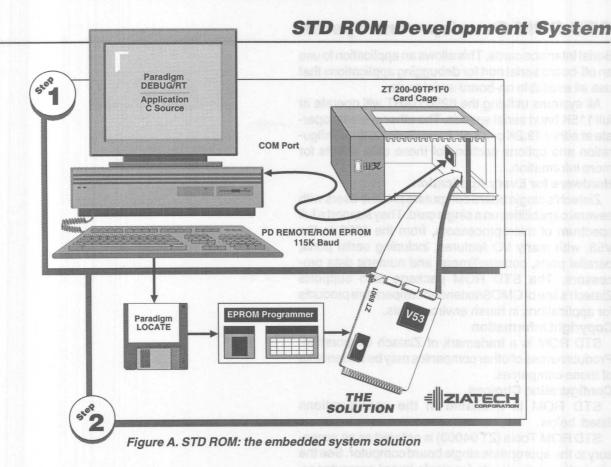
The simple tools of the past no longer support the development of these complex systems. Ziatech's STD ROM meets the need for more sophisticated ROM tools.

(up to 115K baud) RS-232 link back to the host computer with interrupt capabilities. This allows for fast file transfers, debugger updates, and control/break interruption, should a program go astray. The PDREMOTE/ROM EPROM requires a minimal 8 Kbytes of EPROM space and 2 Kbytes of RAM storage for operation, leaving the remaining areas for the user application. This system provides the closest simulation of a final target environment.

After completing a debugging session, the application code is processed with Paradigm LOCATE. This locater allows the executable code to be targetted to ROM and the variable information to be copied into available RAM areas on power-up. Paradigm LOCATE utilizes a configuration file that specifies which segment areas are to be targetted to the ROM or RAM areas. Options include a power-on boot vector, Paradigm DEBUG/RT support, output existing files, Intel OMF-86 output file format, or the Intel hex output formats. The Intel OMF-86 file option supports most standard incircuit emulators on Ziatech's single board computers. The final output of the locater is copied to the user EPROM programmer or the emulator of choice for final system checkout.

No DOS Dependence

IBM PC-based software is found in most engineering development labs throughout the world. This has led to an abundance of high-tech solutions to many of the real-time problems encountered today. Unfortunately, most of the software written for use on the IBM PC is



tied to this environment through its dependence on MS-DOS.

A high-level language program compiled in an MS-DOS environment assumes that it can be loaded at any location in RAM. The language program also assumes that the operating system will allocate it whatever RAM is required. In the initial invocation of a standard .EXE file produced by a high-level compiler (such as Turbo C), all of these issues are resolved automatically by the operating system and by code inserted in front of an application. These operations need to be modified before an application written in Turbo C, for example, can be committed to ROM. The STD ROM package eliminates this dependence.

STD ROM includes start-up modules which eliminate the MS-DOS requirements in a compiled program. Tools are supplied to link the target STD Bus computer of choice to the host PC running the Paradigm DEBUG/RT program. This modification is allowed by linking the start-up module to the application code in the final stages of program development. The startup module can be assembled for application debugging with Paradigm DEBUG/RT, or for locating to the final EPROM image. STD ROM is also available as an option to STD DOS systems. This allows the user to apply all the features of DOS for development and prototyping, and then port to a non-DOS environment for the production version.

High-level Development with C

The language "C" is one of the most productive tools available for embedded system development. C allows quick and easy development with many familiar constructs and data formats. Support of I/O port and bit manipulation capabilities is an important requirement for embedded development. In addition, the ability to target data items anywhere in a system's absolute memory map is sometimes required in embedded systems. C provides both of these features, as well as several other productivity enhancers. C produces very efficient code, allowing the embedded programmer to use minimal RAM and ROM. The STD ROM package supports two of the most popular C compilers, Microsoft and Borland, as well as the Turbo Assembler and Microsoft Assembler.

Target Systems

The STD ROM package supports the following Ziatech Single Board Computers (SBCs) and I/O Control Processors:

- ZT 8801 and ZT 8802 V40 SBCs
- ZT 8809A V20 SBCs
- ZT 8830 I/O Control Processor
- ZT 8832 I/O Control Processor
- ZT 8932 I/O Control Processor
- ZT 8901 V53 SBC

STD ROM also supports Ziatech's ZT 88CT75 Centronics and Serial Interface and ZT 88CT41 Quad



Serial Interface cards. This allows an application to use an off-board serial port for debugging applications that use all available on-board serial ports.

All systems utilizing the 8250 UART will operate at full 115K baud serial speeds. The other systems operate at either 19.2K or 38.4K baud. Refer to the configuration and options sections of these data sheets for more information.

Hardware for Every Application

Ziatech's single board computers provide users with several capabilities on a single card. They support a full spectrum of microprocessors, from the 8088 to the V53, with many I/O features, including serial ports, parallel ports, counter/timers, and numeric data processors. The STD ROM package also supports Ziatech's line of CMOS/extended temperature products for applications in harsh environments.

Copyright Information

STD ROM is a trademark of Ziatech Corporation. Product names of other companies may be trademarks of those companies.

Configuration Choices

STD ROM is available in the configurations listed below.

STD ROM Tools (ZT 94003) is ordered as an accessory to the appropriate single board computer. See the respective data sheets for single board computer ordering information.

STD ROM Development Environment:

ZT 8801	order ZT 94002
ZT 8802	order ZT 94029
ZT 8809A	order ZT 94005
ZT 8901	order ZT 94008
ZT 8830	order ZT 94020
ZT 8832	order ZT 94023
ZT 8932	order ZT 94032

For other configurations, please contact Ziatech.

Manuals for hardware are free with the purchase of an STD ROM development environment.

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.



System Designer's Guide Management American Amer

A ROM-BASED SYSTEM

November, 1993

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Developing a ROM-based System

A ROM (Read-Only Memory)-based system, as we define it here, runs an application without the use of an operating system to initialize and configure the system hardware. This application note will discuss the process of developing a ROM-based STD Bus system, using highlevel languages and ROM-based utilities. We will examine the benefits and difficulties of "ROMing," and compare these to the development of operating system-based STD Bus systems. We will review the compilers, device driver software, and development tools available for developing ROM-based systems, and provide examples of how these software products can speed the ROM development process. Some of these programs are intended for use in an operating system environment, and some are intended for use only in ROM-based applications. We will show how some of the operating systembased tools can be used very productively to develop ROM-based systems.

Why ROM?

A programmer designing an STD Bus system for an Original Equipment Manufacturer (OEM) product is a good candidate for ROMing a system. OEM products are usually produced in large quantities, so the STD Bus final target system is duplicated many times over. These large volumes, in effect, spread engineering costs over a larger installed base, making the development cost-per-unit much more reasonable.

On the other hand, STD applications designed with an operating system incur the overhead and licensing fees of that operating system for each target system. A ROM-based system avoids these recurring licensing costs. Even with the possible cost advantages, the potential difficulty of ROMing an application requires the programmer to ask himself some key questions before undertaking the project.

To ROM or Not to ROM?

The cost advantage of placing your system code in ROM can be significant for an OEM, but the development disadvantages are equally substantial. The decision to ROM or not to ROM involves several key considerations. The first, touched on above, involves how many final target systems will be developed. If the number is large, the costs and difficulties of ROMing make more sense. If the number of target systems is smaller, the speed and ease of developing an operating system-based application often make this latter approach more cost-effective.

Time, Money, and Understanding

One of the strong reasons for including an operating system, such as DOS, is the large amount of software available for peripheral support. If a programmer has these software tools available, his task is reduced to only

DOS Development Benefits

The use of the STD DOS product line from Ziatech can add some enhanced capabilities to the embedded system development cycle. With the STD DOS system, the user can support local storage devices such as rotating, BRAM, and Flash disks. Also, the addition of a local video product will allow the use of screen-based editors, compilers, and debuggers such as the Turbo products from Borland. All of these features will assist the user in getting an embedded application up and running as fast as possible. Once the system is debugged and ready to run, the user can employ the optional STD ROM Tools to provide the proper start-up code and Locator facilities to embed the application into ROM.

his application-specific programming. If these tools are not available, the programmer must be concerned with the initialization of all his peripheral support hardware, plus the software for his application. In certain applications, this can amount to hundreds of hours of engineering time, delaying the project considerably. This is especially true when disks or video devices are involved.

A third item to consider is the programming language available for a ROMable application. If a software engineer is only familiar with IBM BASIC, for example, he will have to learn a new language in order to port his software to ROM, since BASIC is not typically a ROMable language. The learning curve involved in understanding a new language can be quite extensive and costly.

DOS Tools for ROMing

Despite the cost advantage of ROMing an OEM application, demanding development schedules lead many programmers to use operating systems, particularly Microsoft's MS-DOS or IBM's PC DOS, during the development cycle.

DOS has become an incredibly popular engineering development tool. The familiarity and low cost of DOS have made it the standard development environment for both hardware and software engineers. The popularity of this operating system is complemented by a wide selection of development tools based on the personal computer environment. These tools, ranging from powerful word processing packages specially designed for software programmers, to high-level source code debuggers, assist the programmer through the completion of his project.

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The programmer who recognizes the advantages of ROMing his application need not struggle without the benefits of these DOS-oriented development tools. There are a few tools that, although designed primarily for development in a DOS environment, can also be used to boost the productivity of developing a ROM-based system. One such example is the Borland Turbo Debugger. This debugger is very reliant on DOS and will not run without it. However, Turbo Debugger can be used for preliminary debugging on an IBM PC or STD DOS system. Once the application is debugged, it can be separated from DOS and downloaded to the target system for final debugging.

Ziatech's STD ROM package includes the Paradigm DEBUG/RT debugger. Paradigm Systems has licensed Borland's award-winning Turbo Debugger and enhanced it to create custom implementaions exclusively for embedded system debugging. The STD ROM package allows development of ROM-based systems on a PC using a high-level language. It combines the DEBUG/RT user-friendly environment with the customized PDREMOTE/ROM EPROM on the target STD Bus CPU, which allows remote debuggging of STD systems from a PC.

ROMing: What Does it Take?

In the ROM development process, three important steps are required. The first step involves compiling or assembling a program. This generates the object files which will be used in the next step of this procedure. The second step requires linking object files together to form a single executable (.EXE) or Intel Object Module Format (OMF) file. In the DOS environment, the .EXE file can be executed directly from the command line. This .EXE file can also be run through some target debuggers such as Microsoft's Codeview and Borland's Turbo Debugger. The final step in the ROMing process is to locate the application code. The location process involves placing code and initialized data at absolute addresses to prepare for the target EPROM. This step also takes care of assigning fixed addresses for any relocatable items stored in the program. There are several programs available for these three steps and the next section will cover a brief sampling of these programs.

Compilers

There are hundreds of compilers on the market today which are capable of producing efficient code for industrial applications. The interactive compilers such as Microsoft's QuickBASIC and Quick C, and Borland International's "Turbo" line of compilers can help the programmer by bringing the editing, compiling, and debugging processes together into one screen-driven package. This eliminates the need for separate programs for each of the development functions, shortening the learning curve and speeding the development schedule.

These quick compilers are written to perform in the DOS environment and are firmly attached to it. Input/ Output (I/O) functions such as video, keyboard, serial, and disk support are almost inseparable from DOS, and in most cases would not be used without it. By avoiding these DOS-type functions and writing start-up code, these interactive compilers can be used in a ROMed environment. The support for this process is limited; however, there are some other compilers created for the DOS environment that are well supported and provide the information necessary to place code in ROM.

C: A Popular Language for Embedded Systems

The use of C code has become tremendously popular in the development of embedded systems. There are a number of reasons for this popularity. C code is tight and fast, exactly what is needed for today's powerful microprocessors. The small size and efficiency of C makes it a great choice for embedding into ROM.

The high-level features of C let the programmers understand their code more easily, catch mistakes more easily, simplify program maintenance, and generally increase productivity.

With C code, there is also a greater proximity to assembler code than with other high-level languages. This gives the software engineer the greatest flexibility when directly manipulating hardware.

Borland C++ and Turbo C++

The Borland C++ packages are complete compilers which can utilize an interactive mode of operation. Both Turbo C++ and Microsoft's Quick C provide the same editing and compiling features for application development, but Turbo C++ is very popular because of its low cost. All of the Borland C++, Turbo C++, and Turbo C packages are well suited for ROMed applications.

The Borland Turbo C version 2.0 and above compilers are compatible with Microsoft libraries. This is an important point because of the universal acceptance of Microsoft C as an industry standard compiler. Any libraries that were written to support the Microsoft C compiler should now be usable with Borland C++ and with Turbo C. The start-up code required for porting C++ and Turbo C to a ROMed environment is slightly different than that of Microsoft C, however. Because of these minor differences between the Microsoft and Borland compilers, Ziatech's STD ROM development system has separate subdirectories with slightly different start-up code for each compiler and version. Also included with the STD ROM system is Paradigm's DEBUG/RT. The debugging information included in the files is processed by LOCATE utility prior to debugging with DEBUG/RT. Because of its low cost and ease of use, the Borland C++ or Turbo C packages are recommended for use with Ziatech's STD ROM development system. Figure A shows a sample C



Developing a ROM-based System

```
CLIGHTS.C
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// This simple program outputs to the LED
  port on the ZT 8809 once for each 256
// outputs to the ZT 7502 relay card. The
// LED port is toggled on and off.
// Microsoft C programmers should change
   "outportb" to "outp" function.
#include <dos.h>
#define LEDPORT 0x37A /* ZT 8809 LED port */
#define RELAYBD 0x80 /* ZT 7502 address */
  unsigned int i. i. k:
  k = 0:
     Embedded system:
     Never exit outer loop!
  k = k ^ 2:
    outportb(LEDPORT, k);
       Output to ZT 7502
       and delay
    for (i = 0; i \le 255; i++) {
      outportb(RELAYBD, i);
      for (j = 0; j < 1000; j++);
```

Borland C++ example instructions:

1. Compile the CLIGHTS.C program:

bcc -c -ms -f- clights.c

The compiler options disable the automatic running of the linker (-c), select the memory model (-ms for small model), and does not include floating point (-f-). The -v option should be added if debugging information is to be included.

2. Link the C application to the start-up module and any required libraries:

tlink /c bcpp30 clights

The object module ordering guarantees that the startup code is linked first, ahead of the application module. The /c option enables case-sensitivity.

3. Use LOCATE to create the absolute image of the application:

locate -cclights.rm clights

The -cclights.rm option directs the locator to use the configuration file clights.rm to locate the application. The configuration file includes instructions for mapping and ordering the code segments, as well as options for output files (documentation, hex, binary, etc.).

4. The final step is to download the output image to a PROM programmer and create a PROM for the target Ziatech processor board.

Microsoft C example instructions:

- 1. Write your application. Take care to avoid the specified calls listed in the Microsoft C manuals, which make use of DOS or BIOS calls. For this example we will use the clights.c sample program. Note that the program never returns from the main loop, as there is no operating system in a ROM system.
- 2. Compile your application. Using the Microsoft C v6.0, use the cl command as follows: CL/c/AL/Fs/Zd/Od/Oi/Gs clights.c; The switches used in this example are defined as follows:

/c This tells the compiler/linker to just compile without linking.

/AS This switch controls the memory model to be used in the compiling process. This example uses the small memory model

/ZI Creates an object file for use with the Microsoft SYMDEB symbolic debug utility. This is used by both the CodeView debugger and the Systems & Software debugger.

/Oi This switch tells the compiler to generate intrinsic functions instead of function calls for certain functions.

/Gs This causes the normal stack checking to be turned off. This eliminates the stack size error warnings generated when a function is entered. This switch may be omitted if the chkstk.c routine provided w/ STD ROM is linked.

(Note: Some switches may be dependent on release versions.)

3. Link your C application to your start-up module. This module is used to initialize your segment registers, data areas, and stack pointer. The link command line is as follows:

link msc60.obj+clights.obj,clights,clights; The output of the Linker will be a Clights.exe file.

- 4. At this point you are ready for debugging. This procedure can be performed with Paradigm DEBUG/RT. This debugger will allow direct downloading of the clights.exe file to the target system RAM. For more information on either of these packages, refer to the corresponding section in this application note.
- 5. The final function to perform is to run your program through a locator package. Ziatech's STD ROM includes Paradigm LOCATE which can be used for this function. The LOCATE program uses a configuration file and is automatically invoked by the included Makefile. For more details on this program, refer to the LOCATE section of this application note.

Figure A. Sample Program in C, and example instructions to build the program with STD ROM.

program and also shows the steps necessary to compile, link, and locate the code using Borland C++ and STD ROM.

Microsoft C

Microsoft C is a well supported compiler that is a popular choice for many programmers. It includes a list of the library function calls dependent on the DOS operating system. By avoiding these calls and doing some modification to the Microsoft start-up routines, code generated by Microsoft C can easily be placed in ROM. These modified start-up routines will take care of the initialization of segment registers and the copying of initialized data areas from ROM to RAM before passing control to the main C code. The user must also initialize applicationspecific hardware before passing control to the main C program. Several third party vendors, such as Systems and Software, Inc. and DataLight, also provide start-up code for Microsoft C but no support for additional hardware is included. Ziatech's STD ROM system provides the required Microsoft C start-up code. Microsoft provides a minimal amount of support for these ROMed applications, but with a small amount of work the compiled language can be ported into any environment. Microsoft provides a list of functions which are not reliant on the DOS system, and also will provide the source code for all library functions. This allows modification to eliminate any DOS calls in the target code.

In addition to the start-up code, another required feature in a ROMed environment is a good locator and debugger. There are several locator packages available on the market that are compatible with the Microsoft C compiler. Two of these are Paradigm LOCATE (available as part of the STD ROM package from Ziatech) and LINK & LOCATE++ from Systems and Software. Both of these suppliers provide target debuggers that are capable of source-level debugging. These packages will be discussed further in the following sections. **Figure A** lists the actual steps required to produce a ROMed application using Microsoft C and Ziatech's STD ROM package.

iAPX-86 Assembly Language

The IBM MASM macro assembler is the standard tool used to assemble code written in Assembly language. Assembly language is the easiest language to port to a ROMed environment because of the ultimate control of the machine environment. Assembly language also gives the application direct control of the interrupt system, allowing direct interrupt vector programming and interrupt service routine generation. Since the programmer is required to initialize all of the processor registers before beginning his actual application code, only hardware initialization code is required at start-up. The Ziatech STD ROM package provides start-up code for Assembly language but it is not required for system operation. Once developed, this code can be debugged on an IBM PC with the use of the Microsoft Codeview debugger, which has

some expanded capabilities even when debugging Assembly language. Other debuggers are available for the target environment. These include the Softprobe debugger and Ziatech's STD ROM package with Paradigm DEBUG/RT.

Turbo Assembler

The Borland Turbo Assembler comes standard with the Turbo Debugger package and offers the usual speed increase found in Borland's compilers. This assembler is compatible with the Microsoft MASM assembler and also adds some nice features. Assembly language is very easily ported to the ROMed environment and gives the user complete control of his hardware. This direct hardware control gives the programmer added flexibility in programming interrupt service routines and I/O configurations. Both Turbo Debugger and Paradigm DEBUG/RT allow increased productivity in debugging Assembly language programs by allowing symbolic information data to be viewed by the programmer. Code utilizing the Numeric Data Processor (NDP) is also supported by both the Turbo Assembler and these debuggers. Figure B shows a sample development scenario using the Turbo Assembler.

Device Driver Software Development Tools

Another important tool for developing ROM-based systems is the software device driver. Device drivers allow system designers to integrate I/O functions into their applications by providing routines for initializing and driving a variety of I/O cards.

The Greenleaf-supplied package is a library of device drivers made up of two distinct components: the Functions package, which is dependent on the DOS environment, and the COMM package, which is capable of operating independently of DOS and is therefore ROMable.

The Greenleaf Functions package provides a user with many services, including video effects, graphics, disk functions, keyboard functions, etc. Most of these functions utilize the DOS system and can only be linked into an application which is targeted for the DOS environment. These functions are designed for use with Microsoft C and can be used for many of the tasks an application may need to perform. The Greenleaf Functions package can save the user many hours of engineering time, but cannot be easily ported to the non-DOS environment.

The Greenleaf COMM package is designed to access serial ports directly and therefore can be separated from the DOS environment. A popular C package for use with RS-232 communications, the COMM package provides 125 separate functions that can be linked directly to application code without a great deal of trouble. The functions are independent of DOS and are supplied with source code, making it easy to customize them for a ROMed environment.



STD Device Driver Package

The STD Device Driver Package (STD DDP) produced by Ziatech consists of a collection of software drivers for various types of hardware interfaces. This group of drivers, which accesses the hardware directly, has been written exclusively for the hardware products listed in Figure C. This direct access leaves the software interfaces with no reliance on the DOS operating system. The drivers are distributed with complete C source code and can be used with the Microsoft and Borland C and C++ compilers, the Microsoft QuickBASIC environment, and Assembly language. To utilize the STD DDP package in a ROM environment, a user simply links his application code to the supplied routines and provides the start-up code required by the compiler used. Once a hex file is created for this application code, the application may be burned into EPROM.

Developing a ROM Application The Brief Editor

When the development process begins, many engineers utilize any available tool to help them in the code writing process. If the word processor that they regularly use is available, they will use it to write their program whether or not that word processor is the best tool for the job. The Brief Editor is well suited for the software engineer. Brief has many features which make the programming job much simpler no matter which language is used. Some of these features are:

- The ability to use macros to simplify repetitive tasks
- Automatic looping instruction generation
- Automatic file saving capability
- Powerful search and replace capability
- Windowing capability for viewing multiple files
- Compile capability while still residing in Brief
- 1. Create and/or edit your application code (e.g. appl.asm).
- Assemble your Assembly language program using the standard Borland TASM Assembler as follows: TASM appl.asm,,,; The output of the assembler will be an object file (e.g. appl.obj).
- 3. Link your application module to any other object modules or libraries to be used in the final program. This is done as follows: TLINK appl.obj+other.obj,appl.exe,appl.map,other.lib; The output of the linker will be an executable file (e.g. appl.exe).
- 4. Once the executable file has been generated, you may begin the debugging sessions. For this function you can utilize Paradigm DEBUG/RT, included with STD ROM. The Turbo Debugger program will be run on the host PC/AT while the target system will be running the PDREMOTE/ROM program. This will allow downloading of the program to the target system RAM.
- 5. Once debugged, the program can be placed into ROM. This is accomplished using the Paradigm LOCATE program included with STD ROM. Simply supply the configuration file then invoke LOCATE. The LOCATE program output is an Intel Hex-compatible file which can then be downloaded to your EPROM programmer and includes a boot strap vector.

Figure B. Turbo Assembler Development Procedures

These and other features make the programming operation faster and much easier for the software and hardware engineer. The automatic looping instruction generation can be used with most high-level languages available today.

The Brief package can be used on all IBM PC/XT/ATs and most compatibles, including Ziatech's STD DOS systems with a video/keyboard controller. With the use of the Brief Editor on the STD DOS system, the entire application can be developed on the target system beginning with the editing process. Once this first step is complete, the user can proceed to step two, the compiling and assembling process. When the compiling process is complete, the resulting object file is linked with the required start-up code in preparation for the debugging process.

DOS Debugging with Microsoft Codeview

When it comes to debugging a high-level program written in any one of the many languages now available, many engineers wonder how they will ever correlate the Assembly language mnemonics to the actual high-level source code. This problem has been solved with many products now on the market. One of these software packages, Codeview from Microsoft, comes standard with most compilers sold by Microsoft. The Codeview facilities include:

- · High-level source code debugging
- Disassembly in either high-level source or Assembly language
- Breakpoint and watchpoint in high-level data structures
- Register manipulation
- String search capability
- Windowed operation enabling multiple screen viewing

The Codeview program will operate with all IBM PC/XT/AT computers and most compatibles, as well as Ziatech's line of STD DOS computers. When running Codeview with one of the STD DOS computers, a video/keyboard controller is required because of the direct accesses to the video RAM. This video facility is dependent on the DOS system and will not operate in the ROMed environment. Codeview is useful in the DOS environment for eliminating many software bugs. This DOS-based debugging can reduce the debugging task when the application is finally ported to a ROMed environment.

DOS Debugging with Borland Turbo Debugger

The Borland Turbo Debugger is a high-level source code debugger allowing the most advanced features of any software debugger available today. This debugger comes standard with the "Professional" series of Borland compilers. Turbo Debugger includes the following features:

I/O Supported by the STD Device Driver Package (STD DDP)

Interrupt Driven Serial Drivers for 8250-, V40-, V50-, V53, and 486-type ports (All ZT processor boards and ZT 8840, ZT 88CT41, ZT 88CT75 boards)

Serial I/O Drivers using DMA (ZT 8901)

Relay Board Drivers for ZT 7502

Parallel I/O Board Drivers for ZT 8845, ZT 89CT61, ZT 88CT72

Event Sense Interface Drivers for ZT 8846 and ZT 88CT46

Real-Time Clock Drivers for all ZT processor boards

Analog I/O Drivers for Versalogic, Matrix, and Analog Devices 1225, 1226, 1260, 1262, 1265, and compatible boards

Motion Control Drivers for Technology 80 4312, 4323, 4335 boards

Figure C. I/O Supported by STD DDP

- · Source-level debugging
- · Single-stepping
- Pull-down menus
- Full breakpoints
- · Watchpoints on all data types
- Pointer watch capabilities
- · Memory boundary detection

When running in the DOS environment, the Turbo Debugger gives the user the ultimate in software debugging capabilities. These capabilities can be used with any of the Borland products or the Microsoft C and Macro Assembler products. This DOS-compatible version can be run directly on the Ziatech STD DOS line of computers when a video/keyboard controller is included. This can speed an STD Bus development process dramatically by allowing DOS initializations and capabilities to be used in the prototype while allowing the user to extract these capabilities for the target systems.

The Borland Turbo Debugger package also includes a remote development capability called TDREMOTE. This remote program allows a user to maintain the full Turbo Debugger program on a host computer while debugging a remote DOS-based system. This is accomplished through a high-speed RS-232 datalink which eliminates the need for disk or video functionality on the remote system. This technique also reduces the memory requirements of a target system since the 220 Kbyte Turbo Debugger program is resident on the host PC/AT and only a 20 Kbyte program is required on the target system.

Paradigm DEBUG/RT

Paradigm Systems has licensed the Borland Turbo Debugger and enhanced it to create custom implements exclusively for embedded system debugging. In addition to the standard features of Turbo Debugger, Paradigm DEBUG/RT is customized to include:

- Complete processor support, including custom peripheral register views, assembler, and disassembler
- Complex breakpoints with multiple conditions and actions
- Easy-to-use data views including watches, inspectors, dynamic operation, and more

The Ziatech STD ROM development system includes a remote debugging EPROM for the Ziatech CPU board. The EPROM is used during the development process to communicate between the STD Bus system and the Paradigm DEBUG/RT program running on a PC/AT host computer.

Start-up Code

In most DOS-compatible compilers today, there are inherent ties to the DOS operating system. These ties come in the form of calls to allocate memory, calls to initialize memory and stack areas, and calls to initialize hardware such as the Numeric Data Processor. When a programmer attempts to transfer these programs into the ROMed environment, these needs remain unmet unless special start-up code is linked to the application.

The STD ROM Tools include start-up code for the Microsoft C and C++ compilers, the Borland Turbo C and C++ compilers, and Microsoft and Borland assemblers. Other compilers and assemblers may be used to create ROMable images, but the start-up code necessary to allow the application to run independently of the DOS operating system must be provided by the user.

The startup code modules provided with STD ROM are necessary because the segment registers and stack pointer must be initialized, constant data copied from EPROM to RAM, and interrupts enabled before the function main() is called. A simplified description of the startup code explains that the module is designed to get the Ziatech single board computer from the hardware reset event to the first line of the function main() in the C application.

At reset, the startup code must take care of the following chores in order to "jump start" the application.

- 1. stack initialization
- 2. initialized data
- 3. uninitialized data
- 4. initializers/constructors
- 5. call main()

Steps 1 and 5 should be obvious and need no further comment. Steps 2 and 3 handle the initialization of the classes DATA and BSS that are defined by Borland C compilers to contain the initialized and uninitialized data for the application. (Microsoft C compilers also require



initialization of the classes CONST and MSG during these steps.) Since initialized data can exist in EPROM only when power is first applied to the system, Step 2 copies any initialized data from its position in EPROM to its position in RAM. The term "uninitialized data" is misleading because the C language specification guarantees it to be initialized to zero, which is what Step 3 accomplishes. Step 4 can be rather complicated; the startup code will perform the work required for initializers and constructors used for C++ development or the floating point and stream I/O functions supported by the run-time libraries.

If your C application requires additional hardware device initialization before passing control to the main program, this may be added directly to the start-up code since all start-up source code is provided.

STD ROM Development Systems

The STD ROM Development System from Ziatech is provided with the Ziatech CPU of choice, Paradigm DE-BUG/RT, a PDREMOTE/ROM EPROM for remote debugging, STD ROM Tools development disks, RS-232 cables, and complete hardware and software documentation. With the addition of RAM and card cage options, the user can power up and run upon receipt of this development system.

The STD ROM Tools diskettes include start-up code for the Borland and Microsoft C compilers as well as makefiles, math emulation, and some simple DOS emulation support.

The Paradigm LOCATE program included with STD ROM provides the user with the capability to place application code into EPROM. This program uses a unique configuration file which controls the operations of targeting code and data areas via key words. This allows the user maximum flexibility when converting code into a ROMable image. The LOCATE program also includes such key words as the "reserved" key word which allows the user to check his C code for inadvertent accesses to non-existent memory areas. The output of the LOCATE program may be modified by several command line switches which enable features such as compatibility with the Paradigm DEBUG/RT program, Intel Hex format, and Tektronics Hex format.

The development of an embedded system is never complete without thorough design documentation. For this purpose, Paradigm LOCATE can also provide the user with a printable output file. This document allows the checking of variables to optimize performance or to verify their location on the stack. If needed, a complete detailed record is produced, allowing patching of the application code without rebuilding the original source. **Figure E** shows a sample document file that displays the mapping of an embedded application.

In-circuit Emulator Support

One output option of the LOCATE program is the Intel

OMF86 format. This format allows full hardware debugging support through the use of In-circuit Emulators (ICE). Some of the more popular ICE machines compatible with this OMF86 format are produced by Intel, Sophia, ZAX, and Applied Microsystems. The use of the ICE for hardware-based debugging is rarely required with the powerful software debuggers available today. Their use will simplify debugging, though, and in cases of an extremely complicated program, their use may eliminate many hours of frustration.

Suggested Debugging Techniques

When targeting a system into an EPROM, special debugging techniques may be required. These techniques are in contrast to the "brute force" method of burning an EPROM, plugging it in, waiting and watching while nothing happens, and having to start the whole process over again.

One technique for avoiding this scenario involves the use of output instructions to the physical hardware in a system. The hardware may consist of parallel I/O, serial I/O, or merely an LED on the system CPU.

This particular technique utilizes the available I/O facilities in a target system to provide a direct correlation to the application code. By embedding these I/O instructions in the code at strategic points and outputting to the I/O to perform tasks such as turning off the LED, etc., it can

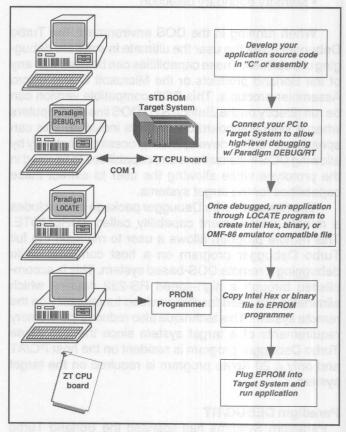


Figure D. STD ROM Development Procedure

Start	Stop	Length	Segment	Class
000400H	000400H	00000H	BEGDATA	DATA
000400H	000403H	00004H	_DATA	DATA
000404H	000404H	00000H	_BSS	BSS
000404H	000405H	00002H	_BSSEND	BSSEND
000410H	000410H	H00000	STACK	STACK
000410H	00080FH	00400H	_STACK	STACK
0F0000H	0F0000H	H00000	BEGTEXT	CODE
0F0000H	0F00D1H	000D2H	_TEXT	CODE
OFO0E0H	0F00E0H	00000H	_INIT_	INITDATA
OFO0E0H	OF00E0H	00000H	_INITEND_	INITDATA
OFO0E0H	OF00E0H	00000H	_EXIT_	EXITDATA
OFO0E0H	0F00EFH	00010H	_EXITEND_	EXITDATA
OFOOFOH	0F00F0H	00000H	_BFD	FAR_DATA
OFOOFOH	0F00FFH	00010H	_EFD	ENDFAR_DATA
0F0100H	0F0100H	00000H	ROMDATA	ROMDATA
0F0100H	0F0100H	00000H	BEGDATA	ROMDATA
0F0100H	0F0103H	00004H	_DATA	ROMDATA
0F0110H	0F011FH	00010H	ERDATA	ENDROMDATA
OFFFFOH	0FFFF4H	00005H	??B00T	(ABSOLUTE)

Figure E. Memory Address Map for Program CLIGHTS

be determined at what points in the code things go awry. This method can also be customized to output byte patterns of integer variables to an 8-bit parallel port or to send the corresponding character to a serial port in much the same way as the "printf" statement is used in conventional debugging on the PC.

Conclusion

In this application note we have discussed the reasons for ROMing an application, and the compilers, linkers, locators, and debuggers which all play important roles in the development of ROM-based systems. We have attempted to provide the information necessary for choosing ROMing tools wisely, and to help programmers in porting their target program to EPROM with minimal problems. If any additional assistance is required, please contact the Ziatech Technical Support Department. West Coast: (805) 541-0488, East Coast: (215) 524-9070. A Bulletin Board Service (BBS) is available at (805) 541-8218, 24 hours-a-day.

Developing a ROM-based System

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"C Contenders", Marty Franz, *PC Tech Journal*, Feb. 1985, pp. 53-67.

"From EXE to ROM," Robert Scott, Embedded Systems Programming, Sept. 1989, pp. 70-82.

"Emulating DOS Calls," Rick Naro, *Embedded Systems Programming*, June 1989, pp. 20-29.

References and Addresses:

- Applied Microsystems Corporation 5020 148th Ave. NE P.O. Box 97002 Redmond, WA 98073 (800) 426-3925 (206) 882-2000
- Borland International
 4585 Scotts Valley Drive
 Scotts Valley, CA 95066-9987
 (408) 438-8400
- Microsoft Corporation 16011 NE 36th Way Box 97017 Redmond, WA 98073-9717 (800) 638-3030
- Paradigm Systems
 3301 Country Club Road, Ste. 2214
 Endwell, NY 13760
 (800) 537-5043
 (607) 748-5966
- Sophia Systems
 3337 Kifer Road
 Santa Clara, CA 95051
 (800) 824-9294
 (800) 824-6706 (CA)
- Systems & Software, Inc. 3303 Harbor Blvd., C-11 Costa Mesa, CA 92626 (714) 241-8650
- ZAX Corporation 2572 White Road Irvine, CA 92714 (800) 421-0982 (800) 233-9817 (CA)

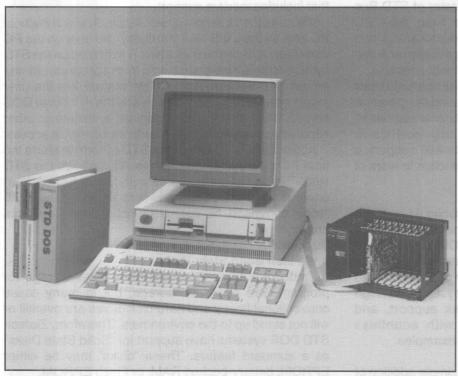
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STD DOS

Development and Operating Systems



STD DOS industrial computers combine DOS operating system utilities and special features for embedded and control applications

Ziatech's STD DOS systems give the system designer a head start by providing an STD Bus system capable of executing and using the large selection of software and development tools available for personal computers. This dramatically improves productivity, making the control oriented STD Bus computer accessible to the large number of users familiar with the PC environment.

Ziatech systems include a special BIOS that tailors the desktop-oriented operating system to address the special requirements of embedded and control environments.

In addition to its impact on desktop computing, the IBM PC has influenced

the industrial market, creating many new development tools and standard software packages designed for control systems.

Ziatech's STD DOS systems allow industrial users to take maximum advantage of these developments and use them in systems expressly designed for the factory and machine, not for the desktop.

The STD Bus and the PC Bus look exactly alike from the software perspective, because they have similar architectures and are based on Intel microprocessors. This means that an STD BUS system can run all PC-based software.

- For embedded and control applications
- Supports single board systems and complete STD-based industrial PCs
- Industrial BIOS removes desktop BIOS deficiencies
- Bootstrap Diagnostics
- Boots up with or without keyboard
- Operates with or without video, keyboard, or disks
- RAM, ROM, and Flash EPROM support built-in
- Unique Virtual System
 Console (VSC)
 development environment
 provides a powerful
 diagnostic and
 maintenance tool
- Multiprocessing support
- Optional device driver library for integrating industrial STD I/O cards



STD DOS Features

Ziatech STD DOS systems contain many features, not available on PCs, that allow the STD DOS system to perform better in industrial applications. These features are detailed below.

Intrinsically Rugged Hardware

The small size and compact form factor of STD Bus boards makes them more reliable than their PC counterparts. Its small board area reduces stress and flexing on the boards, while the card cage design ensures that the boards are firmly retained in the connector.

In addition, Ziatech carefully designs its boards to meet specifications across the entire operating temperature range. All boards are designed to industrial standards, burned-in, and tested to guarantee reliability. Most boards include industrial features such as RS-485 support, a watchdog timer, and AC power-fail detection to warn of an impending system shutdown.

Modular System Design

STD DOS systems allow the user to configure a system precisely, without "extra baggage." For example, a single board solution with the application in ROM eliminates the overhead of disk controllers, video cards, or superfluous RAM, which can reduce the reliability of an embedded application. On the other hand, STD systems with high resolution VGA graphics, hard disk support, and networking, are possible along with countless configurations that fall between these examples.

Industrial BIOS

Ziatech's Industrial BIOS allows the simple addition of components, without special factory configuration. All Ziatech STD DOS systems boot without a keyboard plugged in, even if a video card is installed. A keyboard can typically be connected after boot up and still be recognized. A ROM-based, full-screen setup program allows configuration of memory, disks, boot source, diagnostics, and other system parameters.

Link to a Host with VSC

Ziatech's unique Virtual System Console (VSC) facility provides a tight link between a host PC or laptop computer and an embedded STD DOS system without a video interface. This is useful as a low-cost development aid but is also a powerful diagnostic and maintenance tool that includes modem support.

VSC provides a serial console facility in which the host PC acts as the DOS user interface. The user on the PC can enter DOS commands that are executed on the STD system and view program output from a program running on the STD system. A "Hot Key" feature lets the user toggle between the STD screen and the PC's own DOS screen. VSC also supports regular terminals or other serial devices as well as STD modems for remote access.

Additionally, VSC allows the STD system to share the host PC's file system and drives. This allows the STD system to load an application directly from the host's hard drive, making transfers as simple as using the DOS "copy" command. No complex function key sequences are required.

Support for ROM, RAM, and Flash Solid State Disks

Embedded applications still need mass storage for program load and data storage, but in many cases conventional floppy and hard disk drives are overkill or will not stand up to the environment. Therefore, Ziatech STD DOS systems have support for "Solid State Disks" as a standard feature. These "disks" may be either EPROM, battery-backed RAM, or Flash EPROM.

The BIOS writes out diagnostic codes during boot up so hardware fault can be easily located. These codes are displayed on an optional BIOS diagnostic card.

In fact, all Ziatech STD DOS systems contain the DOS operating system in EPROM or Flash memory so that there is never any problem at the critical boot time. The STD DOS development option includes a utility called

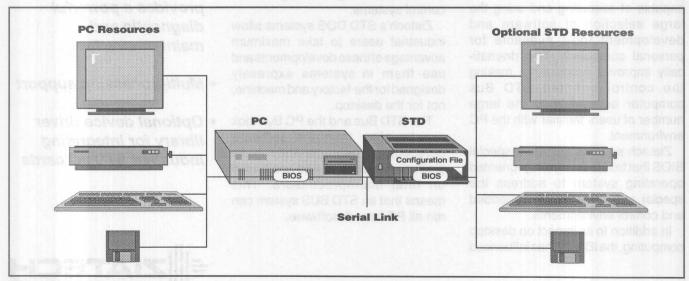


Figure 1. Remote Resource Access

PROMPREP that makes it easy for a user to create PROM disks for any Ziatech processor or memory board. RAM and Flash disks are easily configurable by the user and do not need to be sent to Ziatech for changes.

Solid-state Configuration Files

Other PROM-based systems usually include the two DOS configuration files CONFIG.SYS and AUTOEXEC.BAT in the EPROM. This makes development and maintenance tedious. Ziatech remedies this problem by providing a battery-backed RAM or a writeable Flash drive as part of the standard STD DOS configuration. The BIOS will cause DOS to read the CONFIG.SYS and AUTOEXEC.BAT files from this drive if they are present. If not, it will revert to the defaults in the EPROM. This solid state disk can be used to store other files if required.

Configuration of solid state drives is extremely flexible and simple. Capacities of up to 2 Mbytes on a single board are possible.

Setup

With the screen-based setup program, the user can configure hardware options, memory sizes, as well as the boot source, (PROM, floppy, hard disk or network). It will even let the memory diagnostics be turned off for a fast system boot. The final configuration may be saved into a file for efficient configuration of production target systems (*See Figure 2*).

Multiprocessing Support

A special version of the Ziatech BIOS supports multiple processor in a system. See the STD 32 STAR SYSTEM™ data sheet for more details.

The Development Process

A typical STD application begins with a development phase where code is written and tested. The system used in this process is called the "Development System." In some cases, the system is then installed and the process is ended, apart from any maintenance that may be needed as features are added. In this case, the development system becomes the "Target System." In many cases, however, the target system needs to be duplicated for more machines, test stands, etc. Ziatech software tools speed the development process as well as provide increased functionality and maintainability in the target systems.

A development system can be comprised of a complete STD system such as a ZT 200, ZT 250, or ZT 300 with video and hard drive, or it may be a simple STD single board computer connected to a host PC with VSC. Both allow the application code to be tested on the actual target hardware, but the complete system will provide faster program loading and allow the use of integrated environments such as Turbo C or QuickBASIC directly on the STD system.

SETUP Version 4.00 Copyright 1992 Ziatech Corporation

Floppy Disk A:1.44M	Execute BIOS In Shadow RAM YES
Floppy Disk B:N/I	Power On DiagnosticsON
	Boot DiskPROM
Fixed Disk 0120M	
Fixed Disk 1N/I	Amount Of System RAM640K
	Amount Of Extended RAM3072K
RAM Module Size4M	
Number Of RAM Modules1	Flash Disk LetterP:
RAM Speed70ns	Flash Disk Size768K
Number Of Bus Wait States0	RAM Disk Drive LetterN/A
RAM Disk Drive SizeN/A	
On-Board COM PortsCOM1&2	
On-Board Printer PortLPT1	Erase Flash DiskNO
Shared Printer PortNO	Update System ConfigurationYES

Use ^ and v to select a parameter, < and > to change the value, F10 to accept the current parameters or ESC to quit.

Figure 2. The Configuration Set-up Screen



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Ordering Information Development Systems

The DOS Development system includes VSC, FLASH Support, PROMPREP, the Device Driver Package (STD DDP), serial cables, and a BIOS diagnostic card. See CPU data sheets for specific order numbers.

Manuals for hardware are free with the purchase of an STD DOS development environment.

Target Systems

Order software option S1 for the respective processor board.

NOTE: All development options carry a one-time charge and allow for unlimited use of the software for target systems. This charge does not allow for the unlimited distribution of the development software for development, or unlimited distribution of the operating systems, which must be licensed on a per CPU basis.

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

System Designer's Guide

DEVELOPING STD DOS-BASED CONTROL SYSTEM APPLICATIONS

January, 1994

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Svetem Decigner's Guide

DEVELOPING STD DOS-BASED CONTROL SYSTEM APPLICATIONS

APRIL MELLISI



Introduction

The widespread use of the personal computer and the enormous increase in software based on its operating system (PC DOS or MS-DOS®), has created a demand for this software environment in the design of control systems.

Yet, while the software environment may be similar to desktop PC applications, the physical environment of control systems is often vastly different. The demands of reduced space, harsh environments, unattended operation, and real-time response create problems far beyond the design goals of the PC and its software.

This application note describes the particular features of STD DOS systems that best suit the embedded and control environment, and discusses issues that arise in the design of a DOS-based control application.

Why Use DOS in a Control System?

The main reason for using DOS in a control system is the wealth of software available to help get the job done. Yet, what exactly does DOS provide in the way of services?

Unlike minicomputer operating systems, DOS does not hide the hardware from the programmer. Rather, it is a collection of services that can be used by the application program if required. These services include:

- 1. Program load services to get a program running
- 2. Memory management to keep track of how much memory is used
- 3. Console I/O services for putting output on the screen
- 4. Keyboard service for getting input
- 5. File management services for disk support
- 6. Printer services
- 7. Communication port services
- 8. Real-time clock services

In addition, DOS can be extended with device drivers to add support for other devices such as networks, tape drives, communication boards, etc.

What Are the Disadvantages of Using DOS?

DOS does have some restrictions that may be a concern to some users and of no consequence to others. The main disadvantages are:

- 1. Recurring license fees It is necessary to pay for DOS for each system that uses it. This cost is usually small compared to total system cost.
- 2. Memory usage The operating system requires some ROM and RAM memory. Again the cost of this is usually small compared to the total system cost.
- 3. DOS is not reentrant This means that DOS itself is not designed as a multitasking environment. However, through the use of multitasking kernels that run on top of DOS (such as VRTX32 from Ready Systems), a DOS-based system can be a platform for multitasking.

Real-time Issues

A common misconception is that a DOS-based system cannot be a real-time control system. DOS itself must deal with non real-time devices such as disk drives that may have an unpredictable response time (depending on head location, etc.), but this need not limit the DOS-based control application. Unless the control program actually calls a DOS service (such as a diskaccess), DOS will never gain control of the processor, and the programmer can always have a guaranteed response. In addition, the processor's interrupt system can be used to provide rapid response to any event.

In this case, the only issue to worry about is whether DOS has interrupts disabled for any appreciable length of time. Ziatech has taken great care in the design of its BIOS to minimize these interrupt latencies and has measured those latencies caused by DOS. The maximum latency period was found to be less than 200 microseconds for an 8 MHz V20 processor, and considerably less for faster processors.

The only background activity that takes place in a DOS system is the timer tick that occurs every 55 milliseconds (ms). Although there are no appreciable interrupt latencies associated with the timer tick, it can be disabled by the user in systems that do not require time of day or floppy disk support. In fact, some programmers may wish to disable the timer tick for time-critical code, and re-enable it for floppy disk access.

What to Look for in an Embedded DOS System

An embedded DOS system should have a number of features in common with a PC, as well as some important differences.

An embedded DOS system should have the following characteristics, *in common with a PC:*

- 1. 100% DOS and BIOS compatibility This means it should use MS-DOS or PC DOS to provide complete compatibility for all DOS calls. The BIOS should be 100% compatible with the IBM AT.
- 2. A complete set of peripherals available This should include display adapters, disk controllers, and network interfaces. These peripherals should also be 100% PC-compatible so that existing PC software can port directly to the STD system.

An embedded DOS system should have the following characteristics, *in contrast to a PC:*

- 1. Modularity—Components should be easily separable so the exact configuration can be selected. Maintenance and troubleshooting is improved if the system is designed for modularity.
- 2. Flexibility It should be easy to add or remove components without factory reconfiguration or the need to reburn EPROMs for each configuration.
- **3. Reliability** Reliability is more critical to control applications than to ordinary desktop PC applications. The costs of a failure in a control system can be much



greater than failure in a desktop dydtem (i.e. a lost spreadsheet file). (Reliability can be measured in Mean-Time-Between-Failure [MTBF] rates.)

- 4. Support for solid state disks Floppy and hard disks are the least reliable components in a system and most susceptible to harsh conditions. Solid state disks, including battery-backed RAM, PROM, Flash ROM, and "credit card" (PCMCIA) memory eliminate the need for rotating disks, while increasing performance.

 5. An Industrial BIOS The BIOS firmware controls the initial operation of the system and the boot requirements of a control system are usually different than a desktop PC. An industrial system should be able to start quickly, boot up with or without a keyboard, and recover from system errors if encountered. Additionally, an industrial BIOS allows the user several boot options.
- **6.** The ability to operate without a display This requires the availability of good software tools for development, and the ability to quickly change system configuration parameters and to load new files into the embedded system.

Other important features are:

- Portability to other processors if upgrades are necessary
- · Quality technical and sales support
- Commitment to continuous supply from the manufacturer

Development and Target Systems

A typical STD application begins with a development phase in which code is written and tested. The system used in this process is called the "Development System." In some cases, the system is then installed and the process is complete except for any maintenance that may be needed if more features are added. In this case, the development system eventually becomes the "Target System." However, in many cases the target system will need to be duplicated for integration into several machines.

A development system could comprise a complete, "stand-alone" STD system with CPU board, video/keyboard controller, and hard and floppy drives in an STD Bus enclosure such as the ZT 200, ZT 250, ZT 300, or ZT 1000, or it may be a "PC-assisted system" comprised of an STD CPU board and enclosure connected to a host PC.

Both allows testing of the application code on the actual target hardware, but the stand-alone system provides faster program loading and allows the use of integrated environments such as Turbo C or QuickBASIC directly on the STD system.

Many users develop on a complete stand-alone development system even though their target system is an embedded CPU card.

It is usually best to define the target system before defining the development system even though configurations may change as the project progresses.

Defining the Target System

In selecting a target system there are some high-level parameters to be considered. The main ones are:

- 1. The type and speed of the processor
- 2. The amount of RAM, ROM, flash ROM, or "credit card" memory the application will use
- 3. The peripherals required (video, disk, etc.)
- 4. The type of system enclosure
- 5. How the software will be maintained and upgraded

Processor Choice

Figuring out what type and speed of processor to use can be one of the hardest tasks, especially if the requirements are vague. Ziatech currently offers processors ranging from a 8 MHz V20 to a 66 MHz 80486 DX2. *Figure 1* provides a comparison between these processors and benchtop PCs. Contact Ziatech for information about its latest high-performance processor boards.

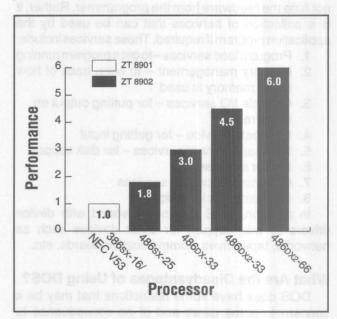


Figure 1. Processor Performance Comparison

The level of performance that can be achieved with an 8 MHz processor is often surprising, but sometimes the higher performance processors are good insurance. When recurring cost is an important factor, it is usually better to aim at the lower end and invest more time in optimizing software for speed. On the other hand, if development time is the driving force, a higher performance processor will provide a lot more headroom and remove the need for time-consuming code analysis.

One of the benefits of the standard DOS architecture is that code developed on one processor will run on another, which keeps upgrading or downgrading simple. It is best to use the performance guide to determine approximately the performance level required and adjust up or down depending on the cost or time demands of the project.

Memory Required

The next step involves estimating how much RAM the system will need, remembering that the RAM requirements of target systems are usually much less than those of development systems. Embedded systems that do not have graphical user interfaces are unlikely to require more than 384 Kbytes of RAM, with 256 Kbytes being typical.

Graphics-based systems may easily reach the 640 Kbyte DOS limit and beyond if using expanded or extended memory techniques. Memory beyond 1 Mbyte is usually necessary only for storing large amounts of information in RAM disks or when using 386- or 486-based programs with sophisticated memory managers (e.g. Microsoft WindowsTM, Desqview, etc.).

In addition to the memory required to execute the program, space is needed to store the program. On a PC, this space is usually found on disk. In an embedded system, space might need to be allocated in PROM, flash, or battery-backed RAM to hold the program. A glance at the CPU specifications will indicate total capacity.

In Ziatech systems, the relative allocations of system versus storage memory is usually flexible. If more is required, it can be obtained by adding another STD memory board, such as the ZT 8825 Expanded Memory System. This board supports RAM, ROM, and flash and uses the expanded memory technique to provide large amounts of system and "solid state disk" memory. Another option is the ZT 8921 PCMCIA 2.0 Interface. This board supports PC CardTM-based memory cards. The ZT 8921's low power "credit card" memory is a rugged, easy-to-expand solution for STD systems.

Display Decisions

Display options are relatively easy to select. Choose the ZT 8842 to support monochrome, or VGA displays. To add Super VGA or flat panel capability, use the ZT 8982 Super VGA/FPD and Keyboard Interface with any processor board, or the zVID2 Local Bus Super VGA/FPD Adapter for the ZT 8902 processor board. Each video board also has an AT-compatible keyboard interface. *See Figure 2* for a summary of the video interface boards.

Disks, Network Interface

High-density floppy disks and hard disks, available separately or with integrated controllers, are standard

items in the Ziatech product line. A SCSI-2 interface is available for interfacing to CD-ROMs, tape drives, and other SCSI devices. Ethernet, ARCNET, and LonWorks™ network interfaces are also available.

Serial Selection

All Ziatech CPUs have on-board serial ports and support RS-232 or RS-485 serial protocols. Additional ports can be added with the ZT 88CT41 Quad Serial Interface, or ZT 88CT75 Centronics and Serial Interface (two), and up to four serial ports (COM1 through COM4) can be supported as DOS devices. However, if high-performance serial communication is required, the optional STD Device Driver Package (STD DDP) is recommended. It provides linkable device drivers that support fully buffered, interrupt-driven serial drivers for on-board and off-board serial ports, and includes Clanguage source code for all drivers.

	Modes	CPUs	Multiple Adapters
ZT 8982	VGA, Super VGA, Flat Panel Support, EL, Plasma & LCD	All	Yes *
ZT 8842	MDA, VGA	All	Yes *
zVID1	VGA, Super VGA	350	1 per CPU
zVID2	VGA, Super VGA, Flat Panel Support, EL, Plasma & LCD	ZT 8902	

* Can have more than one card in a system, switched using software control, but only from one CPU. Multiple cards can not be assigned to multiple CPUs.

Figure 2. Video Interface Board Summary

Software Maintenance Issues

Software maintenance should also be considered in system design. Will the software be right the first time it's placed in the field? Will it change over time? How critical is downtime to the application, and are qualified service personnel available? If the software is going to be extensively tested before release, and is not likely to change, then a PROM disk configuration is the cheapest and most reliable. If not, there are a number of alternatives. Software can be stored in batterybacked RAM disks, flash memory disks, "credit card" memory modules, or even on floppy or hard disks. Upgrades can be installed by connecting a laptop PC to the STD system directly or via a telephone modem, and running the Virtual System Console (VSC) utility. It is also possible to plug an integrated floppy disk drive into the system for upgrades, or to download a new application over a network. These decisions impact the size of the card cage as well as the choice of peripheral boards.

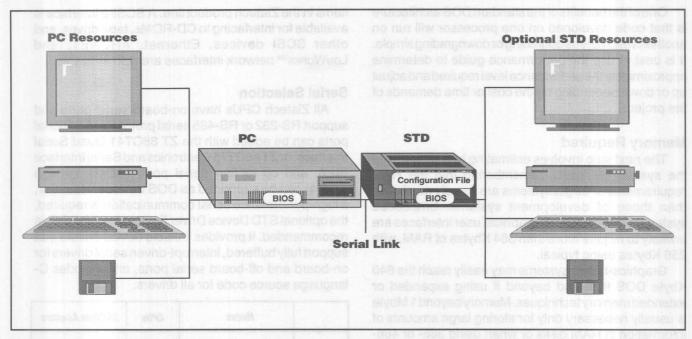


Figure 3. The PC-Assisted Development System allows a PC to act as a host to the STD DOS system.

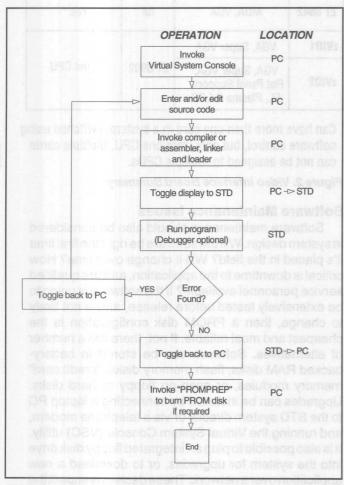


Figure 4. PC-Assisted Development Process

Development Environment Options

As mentioned, there are two basic development environments for a DOS-based STD Bus application.

The PC-assisted Development System depends on a user-supplied PC to support the development process with its keyboard, display, and disks (see Figure 3). This is supported with Ziatech's Virtual System Console (VSC) facility. The PC and STD systems exchange files through a serial cable. Because the two systems operate concurrently, they can execute programs independently of each other.

A program can execute on the PC while another program is running on the STD DOS system. Thus, the host PC is not tied up in terminal emulation mode when the STD DOS system is executing its program.

Connected together over a 115K baud serial line, the PC and the STD DOS system cooperate to develop and debug applications for use in a target system. With its familiar user interface, the PC can be used for editing, compiling, and linking the application program. Once this process is complete and the executable file has been prepared, the program can be tested on the STD Bus computer.

To test the program on the STD Bus computer, the VSC facility is invoked on the PC (**see Figure 4**). This lets the STD DOS system use the PC screen as its user interface.

A "hot key" feature allows the user to "toggle" between viewing the PC screen and the STD screen. Programs can be executed on the STD system in the same manner as on a PC. The STD DOS system, which recognizes files on the PC, loads and executes

13

a PC-based program just as if they were local. VSC also provides the ability to copy the application file to the STD DOS file system.

This feature can be used to take advantage of the battery-backed RAM (BRAM) disk by transferring the file via the DOS standard **COPY** command. Once in the BRAM disk, the program can be loaded at any time since the BRAM drive is non-volatile. (Note that this process is also useful for software maintenance of target systems.)

In a typical PC-assisted system, the A: drive and the C: drive on the host PC will be accessed as drives T: and U: on the STD DOS system. Thus, typing: dir U: on the STD DOS system displays the directory contents of the hard disk C: on the IBM PC. (Note that this works whether the STD system has a local video board or not.)

VSC also allows the user to configure which communications ports to use on both the PC and STD systems, and to program the toggle key. It even supports a modem link between the STD system and the host personal computer.

The PC-assisted system handles video and remote disk requests by actually sending the function calls over to the host for execution. The results are then transmitted serially back to the target. VSC must be installed on the host PC, and the VSC.SYS device driver must be installed on the STD system to implement the link. The communications link uses error checking and checksum information to ensure data integrity. Data checking is performed, and in the case of a data error, retries are done by VSC. Console, disk, and printer requests are handled locally, just as in a PC.

Debugging a program in a PC-assisted system takes place on the STD Bus hardware with the actual I/O configuration used in the final application. This process may be enhanced with one of the many debugging aids available for PCs. Most programs that operate on a PC will also run in the STD DOS environment. Programs that access video memory directly (without using the DOS BIOS) must be used in conjunction with a PC hardware-compatible STD Bus video interface (ZT 8842, ZT 8980, ZT 8981, zVID1). These are usually graphics-based programs.

Video, keyboard, and disk support options are also available in the PC-assisted system by adding Ziatech video and integrated disk boards. In fact, the console, keyboard, and disk can be installed on the local system to facilitate debugging and program development. These options can be added to the PC-assisted system at any time after the original purchase. This is an important advantage if upgrading is an option for OEM systems.

The Stand-Alone Development System operates like a PC except that it also includes the STD I/O used in the control application. When used in conjunction with local disk storage, a CRT terminal, a keyboard, and

an STD bus video card, this configuration performs all of the programming functions required for development or target operation. The advantage of a "standalone" system is that the code can be developed and tested directly in the STD Bus environment. It also allows the use of high-level development tools, such as Borland's Turbo Debugger, directly on the target system.

User programs can be burned into PROM disks or stored in battery-backed RAM or flash EPROM disks in both the stand-alone and PC-assisted systems. The DOS application can also use integrated disk drives to log data or provide floppy disk support in target applications. Another benefit of STD DOS is that the floppy disk drives are IBM PC-compatible and can read and write to files and/or disks created on a PC.

Choosing a Software Development Environment

The developer of a control application must choose a software environment. One of the major benefits of DOS is its ability to meet "most" needs. It is possible, for example, to find standard software packages that are already written for factory control. These are usually expensive and often support many unnecessary features. They usually shorten the development time if they happen to meet the need at hand. Otherwise, the developer must write new code.

High-level languages speed code development and are easily understood by other programmers. The most common language for machine control is "C", usually compiled with the Microsoft or Borland C/C++

I/O Supported by the STD Device Driver Package (STD DDP)

Interrupt Driven Serial Drivers for 8250-, V40-, V50-, V53, and 486-type ports (All ZT processor boards and ZT 8840, ZT 88CT41, ZT 88CT75 boards)

Serial I/O Drivers using DMA (ZT 8901)

Relay Board Drivers for ZT 7502

Parallel I/O Board Drivers for ZT 8845, ZT 88CT49, ZT 89CT61. ZT 88CT72

Event Sense Interface Drivers for ZT 8846 and ZT 88CT46

Real-Time Clock Drivers for all ZT processor boards

Analog I/O Drivers for Versalogic, Matrix, and Analog Devices 1225, 1226, 1260, 1262, 1265, and compatible boards

Motion Control Drivers for Technology 80 4312, 4323, 4335 boards

Figure 5: I/O Supported by STD DDP



```
void main (void)
    /* Initialize the ZT 8841 J2 serial channel */
    ercode = Ser8250InitHw (chan, uart, buffer, buf-
              size, mode vector, cpu_type, eom_value);
    /* Check for errors */
    if (ercode ! = 0) error_handler (ercode);
    /* Get character from DOS console and
      transmit */
    printf ("Input character to send:);
    ch = getch ();
    ercode = Ser8250Xmit (chan, ch. timeout) :
    / * Check for errors * /
    if (ercode! = 0) error handler (ercode);
    /* Wait for 10 characters in serial buffer, then
      receive */
    nbytes = 0;
    while (nbytes < = 9) {
        ercode = Ser8250RecvChk (chan, &nbytes);
        / * Check for errors * /
        if (ercode ! = 0) error_handler (ercode);
    for (i = 0; i < 10; i++) {
      ercode = Ser8250Recv(chan,
        &serial_string [i], timeout);
      / * Check for errors * /
      if (ercode ! = 0) error_handler (ercode);
   /*Flush buffers */
   ercode = Ser8250BuffFlush (chan, flush_in,
      flush out):
    / * Check for errors * /
   If (ercode! = 0) error_handler (ercode);
```

Figure 6. Code fragment showing use of selected STD DDP serial routines.

compilers. "C" is reasonably well structured, but also allows the programmer to get close to the hardware to control what is going on. Pascal is more structured and easier to understand, but not as flexible. BASIC is understood by most people who have done any programming, but is very inefficient and slow in execution. There are many other high-level development tools that are less widely used, including Forth, Modula II, PLM, and others.

Software Development Aids

Developing an STD DOS application is simplified by using device drivers and debugging tools. The Ziatech STD Device Driver Package (STD DDP) supports all popular I/O boards (see Figure 5), including an interrupt-driven serial driver which can be used with up to 32 serial ports. STD DDP drivers are written in C (source code is included) and do not have operating system dependencies. This means that programmers using STD DOS and STD DDP for development will not need to modify STD DDP code, if they later wish to strip out the DOS operating system and "ROM" the application.

The STD DDP drivers can be accessed from BASIC, C, and Assembly languages and come complete with C source code. *Figure 6* shows a C language code fragment using the STD DDP serial driver. Other STD Bus vendors also provide device driver support for their industrial I/O boards to simplify the software development process.

Ziatech also supports the use of Borland's Turbo Debugger on both STD DOS and STD ROM development systems. This powerful, source-level debugger supports all Borland and Microsoft 5.1 and 6.0 compilers with an easy-to-use, interactive environment. Single-step instruction tracing is possible at both the source code and assembly level, including complete event logging and back trace capabilities. Microsoft C/C++ version 7.0 and later users can also run the Codeview debugger on STD Bus systems that support protected mode operation.

Turbo Debugger can be run on Ziatech STD DOS systems in either stand-alone or remote operation. The remote debugging feature lets programmers debug very large programs on a host PC (running Turbo Debugger) and communicate with the target system (running the program being debugged). This unique capability allows programmers to use minimal memory requirements even during the development and debugging stage.

Move DOS Out If Necessary!

Some applications may be so cost- or memory-sensitive that their designers do not want DOS present in the target system. Does DOS make any sense in developing such a system? In some cases it might. DOS, with battery-backed RAM, may be useful for prototyping the initial systems when time, rather than cost, is important. If the code follows a few simple rules, it is then simple to remove DOS and burn a PROM for the final application. Ziatech provides a powerful development system for such applications, called STD ROM. This development system is described in Ziatechniques #7 and the STD ROM data sheet.

STD ROM also uses Turbo Debugger as its "front end," but still requires the user to locate the program and burn a PROM for prototyping. This can be time-

SETUP Version 4.00 Copyright 1992 Ziatech Corporation Execute BIOS In Shadow RAM...... YES Floppy Disk A:.....1.44M Power On Diagnostics..... ON Floppy Disk B:.....N/I Boot Disk.....PROM Amount Of System RAM...... 640K Fixed Disk 1.....N/I Amount Of Extended RAM...... 3072K RAM Module Size.....4M Flash Disk Letter.....P: Number Of RAM Modules..... 1 RAM Speed......70ns Flash Disk Size......768K Number Of Bus Wait States..... 0 RAM Disk Drive Letter.....N/A RAM Disk Drive Size.....N/A On-Board COM Ports..... COM1&2 On-Board Printer Port.....LPT1 Erase Flash Disk......NO Shared Printer Port.....NO Update System Configuration...... YES Use ^ and v to select a parameter, < and > to change the value, F10 to accept the current parameters or ESC to quit.

Figure 7. Configuration Set-up Screen

consuming for many prototypes, where the code may change frequently.

Other Features of Ziatech STD DOS Systems Dynamic System Configuration

The Ziatech STD DOS system has many separate configurable features. These features are selected by editing the system files contained on the battery-backed RAM disk R:, or by running the **SETUP** utility. SETUP is a BIOS-resident system-configuration utility similar to that of an AT personal computer. This utility allows the system configuration to be saved in battery-backed RAM (**see Figure 7**). After executing the hardware diagnostic routines at boot time, the BIOS reads the configuration to determine the various system parameters.

The configuration parameters are protected by a "checksum" word for system integrity. If the checksum is invalid, the system will use BIOS-embedded default parameters. SETUP allows for configuration of hardware options and memory sizes as well as the boot source (PROM, floppy, hard disk, or network). It even lets the memory diagnostics be turned off for a fast system boot. The results of the configuration can be saved into a file for fast configuration of production target systems.

When the system boots from PROM disk, the Ziatech BIOS causes DOS to search for the system files CONFIG.SYS and AUTOEXEC.BAT first on the battery-backed RAM drive R:. If they are not found there, it searches PROM disk P:. This search sequence achieves two goals—easy modification during development, and permanent, unalterable storage for the final target system. During development, the files should be copied from the P: drive to the R: drive so

they can be modified with an editor such as EDLIN. The non-volatile RAM holds that configuration even when power is turned off. When development is complete, these configuration files can be burned into a new PROM drive P: to prevent them from being altered.

100% PC/AT-compatible BIOS

The BIOS (Basic Input and Output System) is the software interface between the industry standard DOS operating system and STD hardware. The Ziatech Industrial BIOS is 100% compatible with the IBM PC/AT DOS BIOS, thereby allowing existing PC software to operate correctly on the STD DOS system. The BIOS entry points (software interrupts) define the interface to system resources such as video, real-time clock, disk drives, and COM ports. Software that uses this interface instead of writing directly to hardware will derive benefits in portability, programming ease, and device independence.

Packaging

Several STD 32 packaging options are available from Ziatech. These include ZT 200 Series Card Cages which are open frame card cages without power supplies. ZT 210 Series provides pluggable AC and DC power supply modules. The ZT 220 Card Cage is for compact systems. The ZT 250 and ZT 300 Industrial Computer Enclosures are sealed units with I/O plates, and the ZT 1000 is an Industrial Workstation. Other enclosures, such as those from Kinetic Computer Corp. offer extreme performance for STD 32 systems in the harshest environments.

ZT 200 Series

The ZT 200 Series card cages are available in 9-, 12-, 15-, 18-, 21-, and 24-slot STD 32 backplane widths. The card cages come without power supplies

Developing STD DOS-based Control System Applications

(except the 24-slot). A number of mounting options are available including table, wall, and 19-inch rack mount. Forced-air cooling is an optional feature of ZT 200 Series card cages. Please refer to the price list or *Technical Data Book* for ordering information.

ZT 210 Series

The ZT 210 Series of card cages are open frame cages like the ZT 200 Series, except they can contain removable power supply modules. AC power supplies in 80 and 150 watt ratings are available as well as a number of different DC power supplies with various input ranges. The power supply modules plug into the backplane like an STD 32 card, yet are firmly attached with screw and heavy duty backplane connectors. Features include front panel access to DC output levels, power indicators, reset switch, power switch, and power input.

ZT 220 Card Cage

The ZT 220 is designed for very small applications (three slots or less) that do not require Slot X functionality. They are available in table and wall configurations and are ideally suited for embedded applications requiring just a few cards. The ZT 88CT85 DC to DC Power Supply card can be used in the ZT 220.

ZT 250 Industrial Computer

The ZT 250 is a completely enclosed, very rugged unit with a 15-slot STD 32 backplane, 80W power supply, and a hinged front panel with integral I/O plates. Several different I/O plates are available with various I/O connectors, or, if desired, the I/O plates can be removed. An additional I/O cable port is located on the right side of the unit. The ZT 250 is designed for panel mounting but can also be table mounted. Smaller backplanes (9- and 12-slot) can be ordered, and forcedair cooling is available.

ZT 300 Industrial Computer

The ZT 300 is a completely enclosed, ruggedized enclosure designed for 19-inch RETMA rack mounting. It incorporates a 24-slot STD 32 backplane, 150W power supply and forced-air cooling. The ZT 300 also features a hinged front panel with individually removable I/O plates like the ZT 250. A cable channel inside the unit allows I/O cables to be routed to the back of the unit also. The ZT 300 can also be ordered with 12- and 15-slot backplanes, and an open-frame version without forced-air cooling is available for 19-inch racks that already have air flow.

ZT 1000 Industrial Workstation

The ZT 1000 is an STD Bus workstation enclosure with a NEMA 4/12 front panel for use on the factory floor and in harsh environments. The system is designed for mounting in NEMA-rated enclosures and incorporates a 14-inch color VGA monitor, 10-key function pad, keyboard port, 15-slot STD 32 backplane, and a 150W power supply. A wide range of processor boards, mass storage devices, and I/O boards can be ordered with

the ZT 1000. A touch screen option, and various types of mass storage in several capacities are also available. Please see the price list and data sheet for ordering information.

Summary

DOS-based embedded or control applications have many requirements different from those of desktop PC applications. These requirements should be carefully considered when choosing an embedded system. When designing a system, an engineer must consider processor speed and features, RAM capacity, peripherals required, and maintenance and expansion needs.

STD DOS Ordering Information

Refer to the STD DOS Data Sheet for additional information when ordering STD DOS development systems and target systems.

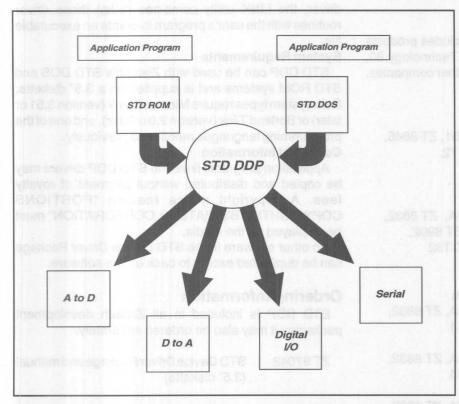
For additional technical assistance on Ziatech's STD DOS products, contact the Ziatech Technical Support Department. Western U. S.: (805) 541-0488, Eastern U. S.: (215) 524-9070. A 24-hour Bulletin Board Service is also available by calling (805) 541-8218.

STD 32 is a registered trademark, and STD DOS, STD ROM, and VSC are trademarks of Ziatech Corporation. Other product names are trademarks of their respective companies.



STD DDP

STD Device Driver Package



Device driver library for STD Bus I/O cards simplifies STD Bus system integration

Easy Integration

Ziatech's STD Device Driver Package (STD DDP) allows system designers to quickly and easily integrate I/O devices into STD Bus control applications. This driver package contains routines for initializing and driving a variety of I/O devices, including serial, parallel, relays, analog to digital, and digital to analog.

Hardware/Software Support

STD DDP supports a wide variety of STD Bus I/O as well as most of the

common peripherals found on Ziatech CPU cards. Hardware devices supported by STD DDP include products manufactured by Ziatech, VersaLogic, Technology 80, Robotrol, Matrix Corporation, Analog Devices, and other companies. Application programs written in Assembly Language, C, C++, and QuickBASIC have complete system access to the I/O hardware when linked to these driver subroutines. All STD DDP drivers conform to a Ziatech specification and therefore provide users with a consistent interface.

Device Driver Package for STD Bus I/O

- Shortens development time
- Simplifies programming
- C source code provided
- Supports C, C++,
 Assembly Language,
 and QuickBASIC
- Provides complete access to I/O hardware
- Operating system independent
- No I/O redirection necessary
- Provides direct and fast device access
- Ziatech supported



Functional Considerations

Product Description

STD DDP is a software package containing device drivers for selected STD Bus I/O devices. The drivers are supported by comprehensive documentation on disk. All drivers conform to a Ziatech specification which is supplied with STD DDP.

Hardware Support

Hardware supported by STD DDP includes products manufactured by Ziatech, VersaLogic, Technology 80, Robotrol, Matrix, Analog Devices, and other companies.

Relay Output

Ziatech ZT 7502

General Purpose Parallel I/O

Ziatech ZT 14CT72/14CT73, ZT 8801, ZT 8845, ZT 88CT49A, ZT 88CT62, ZT 88CT72, ZT 88CT73, ZT 8901, ZT 8902, ZT 8911, ZT 89CT61, zSBX CT31

Serial I/O

Ziatech ZT 8801, ZT 8802, ZT 8809A, ZT 8832, ZT 88CT41, ZT 88CT75, ZT 8901, ZT 8902, ZT 8910, ZT 8911, ZT 8932, zSBX CT32

Event Sense

Ziatech ZT 8846

Programmable Interrupt Controllers

Ziatech ZT 8801, ZT 8802, ZT 8809A, ZT 8832, ZT 8901, ZT 8902, ZT 8910, ZT 8911

Counter/Timers

Ziatech ZT 8801, ZT 8802, ZT 8809A, ZT 8832, ZT 8901, ZT 8902, ZT 8910, ZT 8911

Real-time Clocks

Ziatech ZT 8801, ZT 8809A, ZT 8901, ZT 8902, ZT 8910, ZT 8911

Analog Input

VersaLogic VL-1226, VL-1260, VL-1295, Matrix ADC-12, Analog Devices RTI-1226, RTI-1260

Analog Output

VersaLogic VL-1262, Matrix DAC-12M, Analog Devices RTI-1262

Analog I/O

VersaLogic VL-1225, Analog Device RTI-1225, Robotrol RBX-388

Motion Control

Technology 80 Te4312, Te4323, Te4335

Language Support

STD DDP drivers support applications written in the following languages:

Microsoft C - version 5.1 or later

Microsoft C/C++ version 7.0 or higher

Borland Turbo C - version 2.0 or later

Borland Turbo C++ - version 1.0 or later

Borland C++ - version 2.0 or later

Microsoft QuickBASIC - version 4.5 or later

80x86 Assembly Language

Device Driver Architecture

The device drivers consist of driver modules. These modules are collections of C language routines callable from various high-level languages. Each module relates to a specific I/O device, card, or family of cards.

When a compiled application program is linked to the driver, the LINK utility combines (links) these driver routines with the user's program to create an executable file

System Requirements

STD DDP can be used with Ziatech's STD DOS and STD ROM systems and is supplied on a 3.5" diskette. Both system types require Microsoft Link (version 3.51 or later) or Borland Tlink (version 2.0 or later), and one of the programming languages mentioned previously.

Copyright Information

Application programs linked to STD DDP drivers may be copied and distributed without payment of royalty fees. A copyright notice reading "PORTIONS COPYRIGHTED BY ZIATECH CORPORATION" must be displayed on the media.

No other software in the STD Device Driver Package can be duplicated except to back up the software.

Ordering Information

STD DDP is included in all Ziatech development packages: it may also be ordered separately.

ZT 97042

STD Device Driver Package and manual (3.5" diskette)

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for some products. Contact Ziatech for additional information.





DOS MPX

DOS Multiprocessing Extension

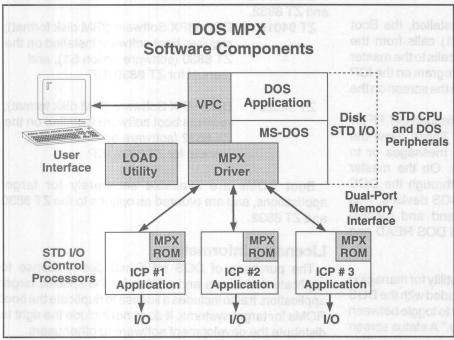


Figure 1. The DOS MPX operating and development environment

An extension to the DOS software environment that supports multiprocessing using Ziatech's I/O Control Processors (ICPs)

The Ziatech DOS Multiprocessing Extension (DOS MPX) provides an operating and development environment that supports multiple ICPs as DOS devices. It supports both the ZT 8830 and the ZT 8832 I/O Control Processors (ICPs).

The DOS MPX system is comprised of a "Boot ROM" for the ICP, an installable device driver for the master processor, and a utility for downloading programs to ICPs. The Virtual Processor Console (VPC) program, another DOS MPX utility, provides a flexible user interface to the ICPs (see **Figure 1**).

Development Environment

Software development for the ICPs is simplified by the use of DOS MPX. Programmers can develop applications in a high-level language (C is recommended) and download them to the ICP without special modifications.

The ICP ROM supports DOS functionality by sending DOS level (INT21) calls to the master processor for execution. In fact, applications on the ICPs can even print to the screen of the master processor. Since the use of DOS calls within the ICP application program loop can slow the response time, full use of these functions is not recommended for time-critical applications. The DOS functions are best used for debugging and error handling situations.

Run Time Environment

Any or all of the components of DOS MPX can be used in the runtime environment. The LOAD utility can automatically load a program into the ICPs on system start-up. Interprocessor communication allows programs on ICPs to communicate directly with the master program without having to reference absolute memory locations.

DOS Multiprocessing Extension

- Simplifies software development
- Easy support for multiple I/O Control Processors (ICPs)
- Extension to DOS environment
- No new operating system to learn
- Supports downloading of programs to ICPs
- ICP applications can make calls to DOS
- Supports high-level languages for ICP programs ("C" preferred)
- Virtual Processor
 Console (VPC) provides
 a unique user screen for
 each ICP
- Master-to-ICP communication facility provided



ROM Functions

The Boot ROM on board the I/O Control Processor (ICP) handles the power-up initialization of the hardware. It also establishes communication with the resident driver on the host CPU via the dual-ported RAM. The Boot ROM handles program loading from the host and passes control to the application program.

Once the application program is installed, the Boot ROM can service most DOS (INT 21) calls from the application. It does this by sending the calls to the master processor to service. This allows the program on the ICP to read and write disk files and to print to the screen on the DOS master.

Additional functions are accessible through INT FF for process-to-process communications. These allow the ICP application to post and receive messages or to determine if a message is available. On the master processor side, messages are sent through the DOS I/O interface where ICPs appear as DOS devices. This enables a master application to send and receive messages to the ICPs using standard DOS READ and WRITE functions.

Virtual Processor Console

Virtual Processor Console (VPC), a utility for managing different ICPs and their screens, is included with the DOS MPX system. This allows the developer to toggle between individual ICP screens using a "hot key." A status screen provides an overview of the multiprocessing system. This resident ICP program can operate concurrently with an application on the DOS master processor.

The system status screen gives the user an overview of the system configuration and shows the frequency of DOS usage and messages from the ICPs (see **Figure 2**).

Ordering Information

DOS MPX environments are available for the ZT 8830 and ZT 8832.

ZT 94019 DOS MPX Software (IBM disk format); requires boot software installed on the ZT 8830 (software option S1), and manual for ZT 8830 ICP

ZT 94022 DOS MPX Software (IBM disk format); requires boot software installed on the ZT 8832 (software option S1), and manual for ZT 8832 ICP

Boot ROMs are available separately for target applications, and are ordered as options to the ZT 8830 and ZT 8832.

Licensing Information

The purchase of DOS MPX includes a license to duplicate the drivers and utilities for the specific target application. It also includes a license to duplicate the boot ROMs for target systems. It does not include the right to distribute the development software to other users.

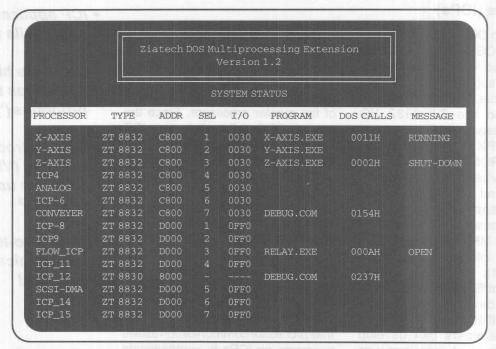


Figure 2. The system status screen in the Virtual Processor Console utility program





STAR-QNX

The Multitasking QNX Operating System on the Multiprocessing STD 32 STAR SYSTEM™



The STAR-QNX system merges multitasking software with multiprocessing capabilities.

The STAR-QNX system combines the advantages of Ziatech's multiprocessing technology with the multitasking and networking capabilities of the QNX® Operating System.

The STAR-QNX system supports up to seven 486-based processors in a single card cage, each running QNX. Each processor has its own local memory (RAM and flash) and shares the STAR SYSTEM's backplane memory. This configuration takes advantage of the message passing

features built into QNX and the shared memory architecture of the STAR SYSTEM to build a tightly coupled network of processors that can share backplane I/O.

Both Ziatech's ZT 8911 Scalable Processor Board and the ZT 8902 Single Board 486 Computer operate in a STAR-QNX configuration. Each of these processors has on-board flash memory that can contain both the CPU BIOS and the QNX operating system image.

- Transparent support of interprocessor communications via QNX network services
- Support for diskless operation
- Multitasking, multiuser, multiprocessor operation
- Communication
 between processors is
 the same whether in
 the same computer or
 over a network
- Very powerful processing in a small and rugged format
- Access to STD 32 ® industrial I/O
- All processors in a system can access I/O cards
- Boot from flash memory removes dependence on a central boot server
- · Fast start-up



STAR-QNX Applications

QNX is a UNIX-like operating system for use in demanding control applications where real-time multitasking performance is an important criterion. Combining QNX features with Ziatech STD 32 hardware produces a compact, rugged, and reliable solution for embedded systems. QNX Software Systems has updated the initial release of QNX to provide POSIX capabilities and a scalable architecture, two features often required for embedded applications.

Initially designed for the desktop platform, QNX has become quite popular in industrial environments. Because Ziatech STD 32 systems are PC architecture-compatible, QNX can operate on a Ziatech STD 32 system the same way it does on a desktop PC. Ziatech STD 32 systems, however, offer size, reliability, and sourcing advantages over desktop PCs. This makes STD 32 systems ideal for industrial, mobile, medical, and other specialized applications.

Ziatech's STD 32 systems also support multiprocessing on the STD 32 B

us. This allows a network of QNX applications to be condensed into a small, rugged computer while maintaining performance and the ability to share I/O systems among processors. The STAR-QNX system easily connects to wider QNX networks with the same transparent communications that is a hallmark of the QNX Operating System.

STAR-QNX Features

Interprocessor Communications

To further enhance the synergy between the STAR SYSTEM and the QNX operating system, Ziatech and QNX Software Systems have collaborated to provide extra features for QNX that fully utilize the STAR SYSTEM architecture.

In the STAR-QNX system, communication between processors is implemented via a QNX network driver (Net.Star). This driver appears to the operating system like any other network driver (e.g., ARCNET or Ethernet) and has the same seamless communication characteristics and transparent system support. Net.Star allows programs on any processor to fully utilize the networking cabilities of QNX and to access files anywhere on the network. It also allows them to connect to any peripheral device, and to launch applications on other processors, if necessary. Applications can still access the system common memory directly, but communication through the network driver is far easier.

STAR-QNX Disk Support

Only the bootserver CPU in a STAR-QNX system can access the disk drives. All other CPUs send requests through the bootserver's disk manager. To enable each CPU to load its operating system image on boot-up, the

STAR-QNX system includes a QNX operating system image in flash EPROM on each CPU card. This includes the Net.Star driver that enables interprocessor communication.

If there are other disk drives on the system (fixed, floppy, or solid state), they are managed by device drivers on the bootserver CPU only. Other QNX tasks on other CPUs can access the disks via the QNX operating system. The CPU with access to the disks does not need the QNX image in flash memory and can boot directly from a disk if required. Once the QNX system image is loaded from flash memory, the rest of the system and application programs can be loaded from the bootserver node.

Solid State Disk (SSD) support is available with the Ziatech ZT 8825 Extended/Expanded Memory System Board. The bootserver processor contains a QNX image stored in the on-board CPU flash memory which includes the QNX driver for the SSD.

A processor can also run independently, using only the QNX image stored in the on-board CPU flash memory. At startup, this image is loaded from flash to the CPU's on-board RAM, from which the application is executed. This can be useful for quickly starting tasks at bootup that cannot be delayed until the entire bootup sequence has been completed.

Development Tools

The QNX operating system supports the Watcom™ C compiler, an ANSI-compatible, highly optimized compiler. QNX also fully supports Assembly language object modules generated by standard PC assemblers and the WATCOM VIDEO symbolic debugger.

The latest version of QNX includes the components necessary to operate with the Ziatech STAR SYSTEM. The software is ordered directly from QNX Software Systems and must include a license for each CPU that will be running QNX.

QNX operates in a STAR SYSTEM on a ZT 8911 Scalable Processor Board or a ZT 8902 Single Board 486 Computer. These can be ordered as STAR SYSTEM components and combined with other Ziatech peripherals and STD 32 I/O cards to meet the needs of the specific application. Each CPU that requires a bootable QNX image in flash memory should be ordered with Software Option S3. This requires a corresponding CPU license that can be ordered from QNX Software Systems. One CPU can be ordered with DOS if that CPU will boot QNX from a hard disk, but DOS is not required. CPU node IDs are set in Ziatech's STAR BIOS setup program, which is accessible at boot time.

Once an application has been generated and is ready to be loaded into a target machine, a QNX image is easily generated using the **buildqnx** utility, which is included with the QNX operating system. In QNX, the image can then be quickly programmed into the CPU's on-board flash memory using Ziatech's **Qflash** utility.

The Ziatech STAR-QNX development system option (ZT 94030) is necessary for the first order. It includes the tools necessary to reprogram the flash memory on the CPU card and the ZT 8826 Boot-off board that is essential to recover from flash programming mistakes. The development option also includes the STD DDP device driver library that contains native "C" code for the most commonly used STD 32 cards. This code is a useful starting point for anyone wishing to build driver support into their QNX application.

The development option also includes all manuals for all products in the order.

Ordering Information

For Development:

- 1. Order the appropriate Ziatech CPUs and specify software option S3.
- Order the desired enclosure and peripheral cards and the ZT 94030 STAR-QNX Development Option.
- Order QNX with the appropriate number of licenses from QNX Software Systems in Kanata, Ontario, Canada at (613) 591-0931. Specify QNX for Ziatech Systems.

For Target Systems:

Ordering for the target system is the same as for the development system, except the ZT 94030 development option is not required.

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

For a copy of the warranty, refer to the *Technical Data Book* Appendix or contact Ziatech.

STD 32 ia a registered trademark of Ziatech Corporation.QNX is a registered trademark of QNX Software Systems. WATCOM is a trademark of WATCOM Systems, Ltd.



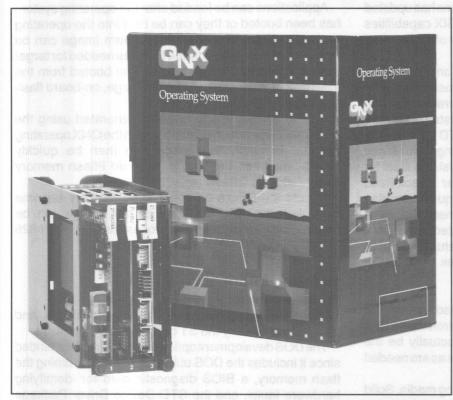
FAX (805) 541-5088 • Telephone (805) 541-0488





STD 32-QNX

QNX® Real-Time Multitasking Operating System on STD 32® Computers



STD 32-QNX combines the small industrial computer format of STD 32 with the real-time, multitasking features of the QNX operating system.

The STD 32-QNX system provides an operating and development environment for the QNX® operating system running on Ziatech STD 32® hardware

STD 32-QNX supports Ziatech's ZT 8911 Scalable Processor Board and ZT 8902 Single Board 486

Computer. Each of these processors supports the full range of 486 CPUs and has on-board flash memory that can contain both the CPU BIOS and an optional QNX operating system image. The processors can also be configured as industrial PCs with all the associated peripherals.

- Multitasking, multiuser operation
- Very powerful processing in a small and rugged format
- Access to STD 32[®] industrial I/O
- Fast start-up with on-board boot from flash memory
- Boot from flash memory removes dependence on a central boot server
- Support for diskless operation



STD 32-QNX Applications

QNX is a UNIX-like operating system for use in demanding control applications where real-time multitasking performance is an important criterion. Combining QNX features with Ziatech STD 32 hardware produces a compact, rugged, and reliable solution for embedded systems. QNX Software Systems has updated the initial release of QNX to provide POSIX capabilities and a scalable architecture, two features often required for embedded applications.

Initially designed for the desktop platform, QNX has become quite popular in industrial environments. Because Ziatech STD 32 systems are PC architecture-compatible, QNX can operate on a Ziatech STD 32 system the same way it does on a desktop PC. Ziatech STD 32 systems, however, offer size, reliability, and sourcing advantages over desktop PCs. This makes STD 32 systems ideal for industrial, mobile, medical, and other specialized applications. These applications often require operation without disks or rotating media. To meet the extra requirements of these applications, Ziatech and QNX Software have incorporated additional features into QNX that take advantage of the capabilities of STD 32 computers.

STD 32-QNX Features

Since the QNX operating system is used for both the development and target operating environments, the development and target systems can actually be the same. QNX accommodates as many tasks as are needed during the development process.

For applications that cannot have rotating media, Solid State Disk (SSD) support is available using the Ziatech ZT 8825 Extended/Expanded Memory System Board. This includes the ability to boot QNX from the SSD by using a QNX image that contains the SSD driver. This image is stored in the on-board CPU flash memory.

A processor can also run independently, using only the QNX image stored in the on-board CPU flash memory. At startup, this image is loaded from flash memory to the CPU's on-board RAM, from which the application is executed. This can be useful for quickly starting tasks at bootup that cannot be delayed until the entire bootup sequence has been completed.

Development Tools

The QNX operating system supports the WATCOM™ C compiler, an ANSI-compatible, highly optimized

compiler. STD 32-QNX also fully supports Assembly language object modules generated by standard PC assemblers, and the WATCOM VIDEO symbolic

debugger.

Ziatech hardware is ordered by choosing the appropriate components required. A development system usually consists of a card cage, processor board, video option, and a hard drive and floppy drive. The CPU card should be ordered with the S1 option, which includes DOS in

flash memory. This provides a reliable boot source and some development and diagnostic tools. This DOS in flash memory can be removed later and replaced with a customer QNX image if required. The Ziatech BIOS allows the user to designate the boot source as either floppy, fixed disk, or PROM.

Applications can be loaded after the operating system has been booted or they can be built into the operating system's image. The operating system image can be customized to include only the features needed for target system operation. This image can be booted from the fixed disk or floppy disk or from the large, on-board flash memory on the Ziatech CPU card.

A QNX system image is easily generated using the **buildqnx** utility, which is included with the QNX operating system. In QNX, the image can then be quickly programmed into the CPU's on-board Fflash memory using Ziatech's **Qflash** utility.

Should the CPU's on-board flash memory become corrupted, the CPU BIOS or a QNX image can be restored via a simple recovery process using the ZT 8826 Boot-Off-Board.

Ordering Information

For Development:

Order the appropriate Ziatech CPU, enclosure, and peripherals. Specify the S1 option for CPU software.

The DOS development option is strongly recommended since it includes the DOS utilities for reprogramming the flash memory, a BIOS diagnostic card for identifying hardware faults, and the STD Device Driver Package (STD DDP), which includes source code that can be used as a model for QNX drivers.

The ZT 8826 Boot-Off-Board is recommended if the user intends to reprogram the on-board flash memory with a QNX image.

Order QNX from QNX Software Systems in Kanata, Ontario, Canada at (613) 591-0931 and specifiy QNX for Ziatech Systems.

For Target Systems:

Order the appropriate QNX configuration or license from QNX Software Systems.

Ziatech processors can be ordered without DOS software in quantity orders (S0 Option) or with DOS (S1 Option) if MS-DOS in flash memory is required as a backup option.

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

For a copy of the warranty, refer to the *Technical Data Book* Appendix or contact Ziatech.

STD 32 is a registered trademark of Ziatech Corporation.QNX is a registered trademark of QNX Software Systems. WATCOM is a trademark of WATCOM Systems, Ltd.



STD 32[®] Enclosures

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STD 32° Enclosures Product Feature Guide

Product	Mounting Options	Number of Slots	Data Width (bits)	Card Centers	Power Supply Choices	Forced- Air Cooling
ZT 200 Series Card Cages for the STD 32 Bus	Table, Wall, 19" Rack	9, 12, 15, 18, 21, 24	8/16/32	0.625" 1.6 cm	None, 150W	Optional
ZT 210 Series STD 32 Card Cages with Removable Power Supplies	Table, Wall, 19" Rack	9, 12, 15, 18, 21	8/16/32	0.625" 1.6 cm	75W, 150W (AC) 55W, 75W (DC)	Optional
ZT 220 Compact STD 32 Card Cage without Slot X	Wall	3	8/16/32	0.625" 1.6 cm	None	None
ZT 250 Industrial Computer Enclosure	Table, Wall	9, 12, 15	8/16/32	0.625" 1.6 cm	75W	Optiona
ZT 300 Industrial Computer Enclosure	Table, 19" Rack	12, 15, 24	8/16/32	0.625" 1.6 cm	150W	Optional
ZT 1000 Industrial Computer Workstation	Panel, 19" Rack	15	8/16/32	0.625" 1.6 cm	150W	Included

Also Inside This Section

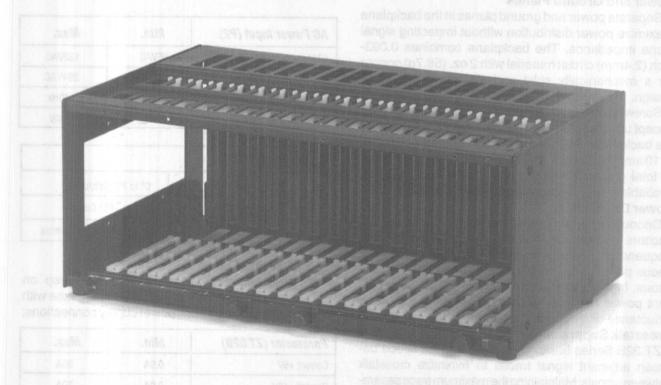
- ZT 2592 RS-232 to Isolated RS-422/485 Converter
- ZT 2595 RS-232 Transient Protection
- ZT 2500 Series Removable I/O Access Plates
- RCC-32 Rugged Card Cage
- ZT 88CT85 DC to DC Power Supply Board

Card cages designed for ruggedness and equipped with high-performance backplanes which provide 8-, 16-, and 32-bit data transfers for the STD 32 Bus

The ZT 200 Series of open frame card cages from Ziatech are designed for high-performance, STD 32® systems and for operation in electrically noisy environments. ZT 200 Series card cages are available in table, wall, or rack mount configurations. A 150 watt power supply is an option offered with the 24-slot model. Conforming to the STD 32 Bus Specification, these rugged, steel cages include an integral card-retainer bar, and are suitable for use in 19" equipment racks,

NEMA cabinets, or embedded machines. Their black, powder coated steel construction resists corrosion and withstands shock and vibration.

The integrated backplane design accommodates 8-, 16-, and 32-bit data transfers, while utilizing multilayer construction, controlled layer separation, and trace sizing for appropriate impedance characteristics. ZT 200 Series card cages are available in 9-, 12-, 15-, 18-, 21-, and 24-slot versions.



- 9-, 12-, 15-, 18-, 21-, and 24-slot versions, 0.625" centers
- 3-U EURO cage format; height: 5.22" (13.3cm)
- Five layer STD 32 backplane
- · 8-, 16-, and 32-bit data transfers
- STD 32- and STD Bus-compatible
- Steel powder coated construction

- Table, wall, and rack mount versions available
- Forced-air cooling optional
- Integral card restraint
- Multiple power connection screw terminals
- Power decoupling capacitors
- 150 watt power supply option for 24-slot version

Note: For embedded applications, the ZT 32B backplane is available without the card cage. Please contact Ziatech for details.



Functional Considerations

Mechanical

The ZT 200 Series of open frame card cages include Ziatech's ZT 32B backplanes, and are available with 9, 12, 15, 18, 21, or 24 STD 32 slots on 0.625-inch (15.9mm) centers. The steel construction with black powder-coated finish provides a rugged mechanical enclosure for the backplane and STD 32 system. These card cages are suitable for applications where shock and vibration is part of the operating environment.

Air Circulation

Airflow and accessibility are provided without compromising mechanical integrity. Ventilation openings above and below the cage allow ample air circulation. Forced-air cooling using bottom mounted 12V fans is available for all models providing 300 feet per minute airflow.

Power and Ground Planes

Separate power and ground planes in the backplane maximize power distribution without impacting signal plane impedance. The backplane combines 0.093-inch (2.4mm) circuit material with 2 oz. (56.7g) copper for a mechanically solid and electrically optimized design.

Screw terminals installed on back of the backplanes accept up to #16 AWG wire at periodic intervals across the backplane, and can handle up to 30 amps at +5V, or 10 amps at ±12V. In this configuration, up to 50 amps of total ground current is possible when utilizing all available power and ground connection terminals.

Power Decoupling

Decoupling is accomplished with high-quality capacitors chosen for their low ESR values at high frequencies. These capacitors provide the instantaneous power required by the system during simultaneous, high-current output switching. They also prevent power fluctuations caused by wiring and trace inductance or by power transients.

Crosstalk Suppression

ZT 32B Series backplanes maximize the space between adjacent signal traces to minimize crosstalk between signals. Maintaining the maximum trace separation over the entire backplane ensures signal integrity.

Slot X-compatible

For STD 32 applications, one card-edge connector slot is always designated as "Slot X," leaving the remaining slots for STD-80 Series or STD 32 cards. For example, a ZT 200-09 has nine slots, of which one is Slot X, and the eight remaining slots can be used for other STD boards.

Slot X gives the STD 32 Bus slot-specific addressing capability (for jumperless systems), high-performance DMA capabilities, multiple bus-master arbitration, and additional interrupt signals. These additional signals are located on one unique layer within the backplane.

Specifications Electrical

• P2 Unit (150 watt power supply, 24-slot only)

Output Voltage (P2)	Min.	Max.
DC Output Voltage +5V	4.75V	5.25V
DC Output Voltage +12V	11.40V	12.60V
DC Output Voltage -12V	-12.60V	-11.40V

Output Current (P2)	Min.	Max.
DC Output Current +5V*	0.0A	20.0A
DC Output Current +12V*	0.0A	6.0A
DC Output Current -12V*	0.0A	2.0A

^{*} Output power not to exceed 150 watts continuous. Derated 3.75 watts per degree C over 50° C.

AC Power Input (P2)	Min.	Max.
AC Voltage (low range)	85VAC	132VAC
AC Voltage (high range)	170VAC	264VAC
AC Frequency	47Hz	440Hz
Power Consumption		215W

Environmental (P2)		
Operating Temperature	0° to 70° Celsius	
Storage Temperature	-40° to +85° Celsius	
Non-Condensing Relative Humidity	5% to 95% at 40° Celsius	

ZT 32B Backplanes

The following ratings limit the voltage drop on any plane to below 0.05V on a ZT 32B backplane with evenly distributed loads and power supply connections:

Parameter (ZT 32B)	Min.	Max.
Current +5V	0.0A	30A
Current +12V	0.0A	10A
Current -12V	0.0A	10A
GND Current	0.0A	50A
Characteristic Impedance	55 ohms *	194 1709 h

^{*} With nominal loading of the backplane

Environmental (ZT 32B)		
Operating Temperature	0° to 70° Celsius	
Storage Temperature	-40° to +85° Celsius	
Non-Condensing Relative Humidity	5% to 95% at 40° Celsius	

Mechanical (ZT 32B)

- Connectors
 - Px: Dual screw terminals for power connections and push-button reset
 - Jx: Dual 136-pin STD 32 card-edge connectors rated at the following:
 - 5V @ 10A maximum current per card (2A per pin)
 - 30 milliohms maximum contact resistance
 - 2 pF/slot without cards at 1 MHz 200 insertions minimum

Environmental (ZT 200 Series Card Cages)		
Operating Temperature	-40° to +85° Celsius	
Storage Temperature	-55° to +125° Celsius	
Non-Condensing Relative Humidity	5% to 95% at 40° Celsius	
Non-Operating Shock *	30g for 6ms	
Operating Shock *	15g for 11ms	
Non-Operating Vibration *	5 to 300 Hz at 0.35mm (5g)	
Operating Vibration *	5 to 300 Hz at 0.35mm (5g)	

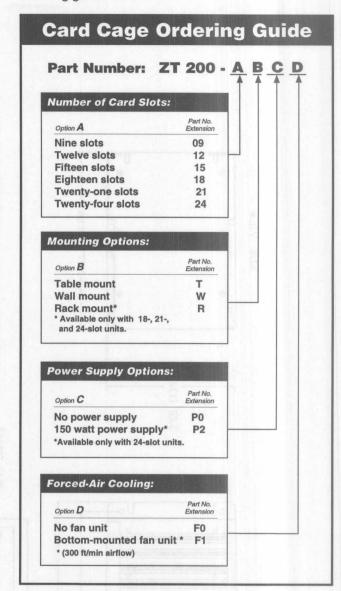
^{*} Meets or exceeds IEEE Specification P1156

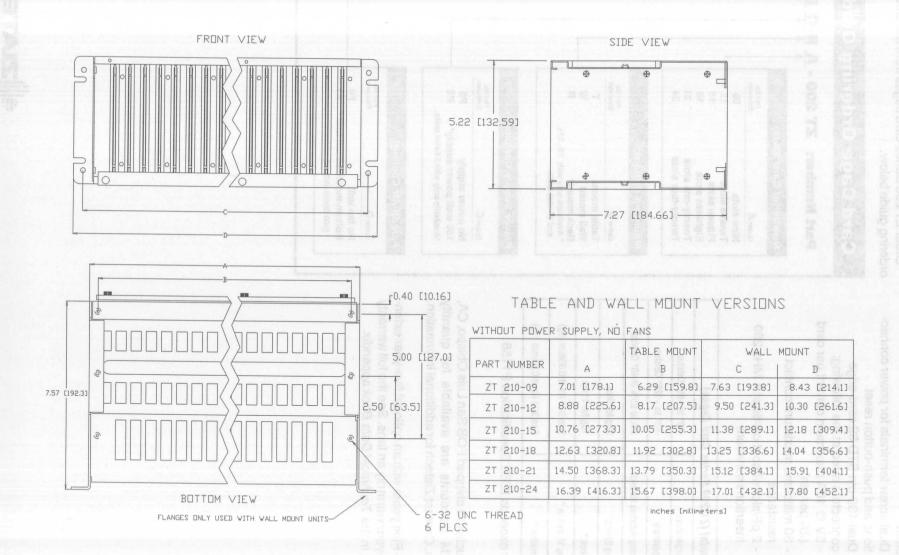
All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

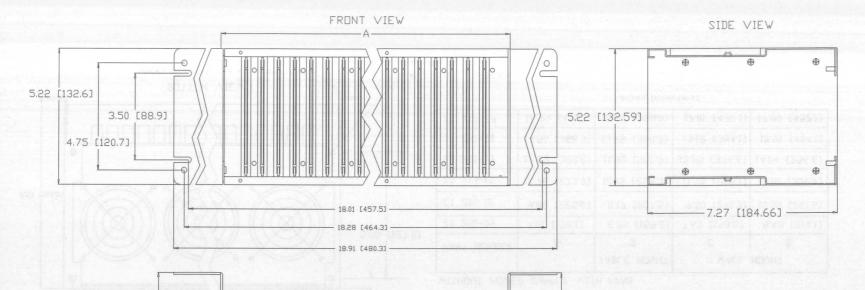
Warranty – Five years with an optional five-year extension. Two-year warranty on fans. See the full warranty statement in the *Technical Data Book* appendix.

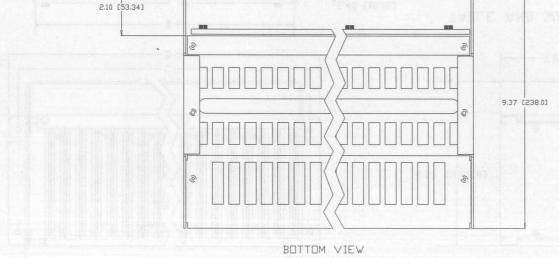
Ordering Information

Order ZT 200 Series card cages from the card cage ordering guide below.





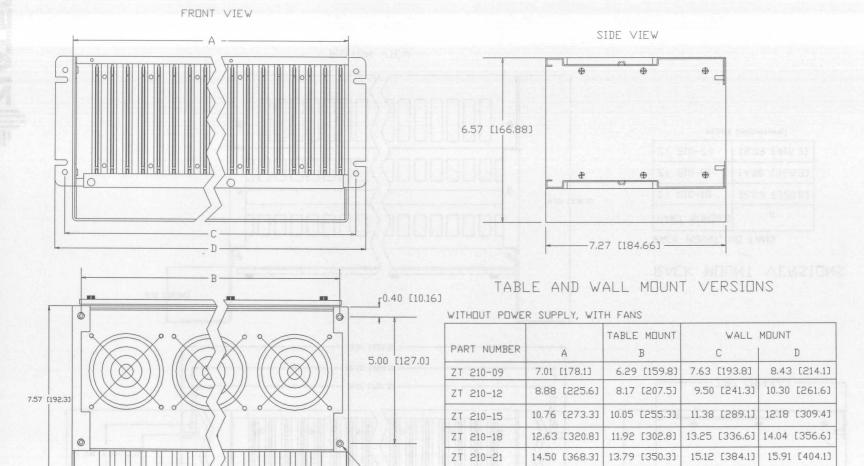




RACK MOUNT VERSIONS

RACK MOUNT, NO FANS

PART NUMBER	Α
ZT 210-18	12.63 [320.8]
ZT 210-21	14.50 [368.3]
ZT 210-24	16.39 [416.3]



ZT 210-24

6-32 UNC THREAD

4 PLCS

BOTTOM VIEW

FLANGES DNLY USED WITH WALL MOUNT UNITS-

16.39 [416.3] 15.67 [398.0]

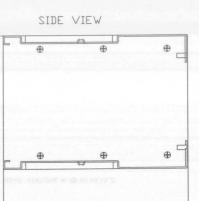
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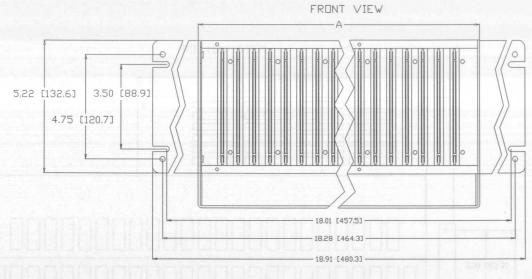
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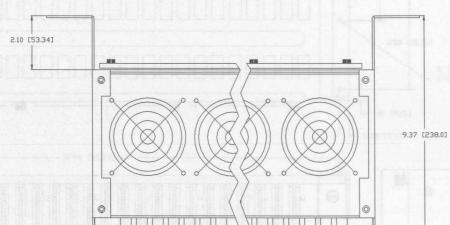
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STD

32® Bus







BOTTOM VIEW

RACK MOUNT VERSIONS

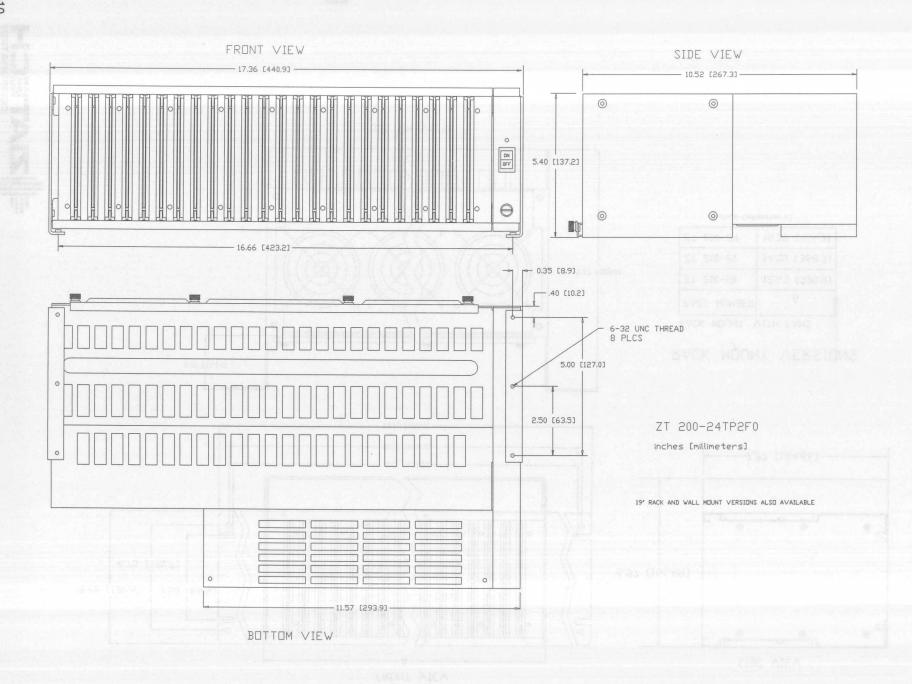
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RACK MOUNT, WITH FANS

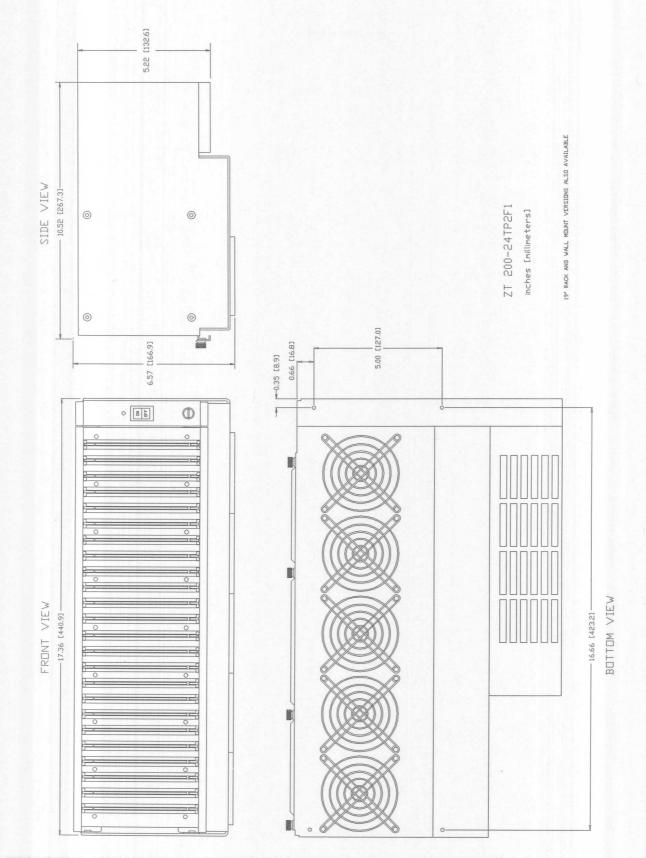
6.57 [166.88]

	PART NUMBER	А
The same	ZT 210-18	12.63 [320.8]
	ZT 210-21	14.50 [368.3]
	ZT 210-24	16.39 [416.3]





ZT 200 Series Mechanical Drawings (24-slot table mount shown, with P2 power supply and fans)



ZIATECH





ZT 210 Series

STD 32® Card Cages with Removable Power Supply Modules

Rugged card cages feature high-performance STD 32 backplanes for 8-, 16-, and 32-bit data transfers, and removable power supply modules

The ZT 210 Series of card cages for the STD 32 Bus offer the highest performance level available for STD 32 and STD Bus systems. These card cages are designed for rugged environments where shock and vibration, temperature extremes, and electrical noise are present. These card cages are available in 9-, 12-, 15-, 18-, and 21-slot widths using high-performance STD 32 backplanes supporting 8-, 16- and 32-bit data transfers. The backplanes utilize multilayer construction, controlled layer separation, and trace sizing for noise immunity and optimum signal integrity. The card cages can be ordered in table, rack or wall mount configurations and with optional forced-air cooling.

The removable power supply modules allow quick replacement of the power supply for servicing or adapting the system to changing power requirements. Power supply modules are available in AC and DC input configurations offering various input voltage and wattage ratings. Front panel access is provided on the modules for AC or DC input power, +5 and +12VDC output voltages, LED voltage indicators, and an on/off switch.

Both the card cages and power supply modules feature rugged steel construction with a durable black powder coat finish to minimize corrosion. ZT 210 Series card cages include a card retainer bar for operation in shock and vibration environments.



- Removable AC and DC power supply modules
- 9-, 12-, 15-, 18-, and 21-slot versions,
 0.625" centers
- 3-U EURO cage format; height: 5.22" [13.3cm]
- Five-layer STD 32 backplane
- 8-, 16-, and 32-bit data transfers
- STD 32- and STD Bus-compatible
- Steel powder coated construction

- · Table, wall, and rack mount versions available
- Forced-air cooling optional
- Integral card restraint
- DC input range: 10 to 72VDC
- AC input range: 90 to 264VAC, 47 to 440 Hz
- Front panel access to +5, +12VDC and GND
- Front panel power and reset switches



Functional Considerations Modularity

The ZT 210 Series of card cages allows quick power supply replacement with a selection of removable power supply modules in various AC and DC configurations. The power supply modules slide into the card cage in the same manner as an STD card. Retention screws and a sturdy backplane DIN connector lock the power supply module in place. Power input, +5 and +12 DC output voltages, +5, +12, and -12VDC power indicators, push-button reset, and a power switch are all located on the front of the power supply module for ease of access. Large DIN 41612 connectors provide up to 15 amps of current capability per pin on the connection between the power supply modules and the backplane.

Mechanical

ZT 210 Series card cages are available in 9-, 12-, 15-, 18-, and 21-slot widths on 0.625-inch (15.88mm) centers and feature a power supply bay location on the right side of the cage for a removable power supply. The height of the ZT 210 Series of card cages conforms to the European 3U standard (5.22-inches, 132.54 mm). Modular power supplies slide in and out of the power supply bay just like an STD card. Power supplies are restrained with captive thumb screws on the front of the cage while the STD cards are restrained with a locking bar. A stainless steel handle on the power supply modules assists removal from the card cage. The powder coated steel construction of the card cage and power supply modules provides corrosion resistance and performance under shock and vibration conditions.

In addition to the various slot widths available, the ZT 210 card cages can be ordered in table mount, wall mount and rack mount configurations. Table mounting allows the card cage to rest on a flat horizontal surface with rubber feet, or be firmly attached with screws. Wall mounting provides brackets on the back side of the card cage for mounting to a vertical wall with screws. The rack mount option provides brackets for 19-inch RETMA racks but is only available for 15-, 18-, and 21-slot models. The forced-air cooling option adds bottom mounted fans and is available for all slot widths. Forcedair cooling is recommended for high-speed 486 processors.

All ZT 210 Series card cages include a power supply bay for the removable power supply modules. Users who prefer card cages without integral power supplies should order from the ZT 200 Series of card cages. Please refer to the ZT 200 Series data sheet for more information.

Electrical

All ZT 210 Series models include a Ziatech STD 32 backplane with STD 32 connectors. This backplane also includes a heavy duty DIN connector (DIN 41612),

for making the modular connection between the backplane and removable power supply module. This connector provides large pins capable of 15 amps of current. The ground connections are first made mechanically on this connector when a power supply module is inserted. Backplanes used in ZT 210 Series card cages use separate power and ground planes to maximize power distribution without impacting signal plane impedance. The space between adjacent signal traces has also been maximized to minimize crosstalk between signals. For STD 32 applications that require the highest level of performance, the leftmost slot is designated "Slot X" for bus arbitration, DMA capability. and additional interrupt support in multiprocessing applications. The remaining slots provide standard address and data lines for any STD 32 or STD Bus card.

Both AC and DC power supply modules are available. AC modules provide an IEC 320 power receptacle on the front panel for AC input power. This receptacle includes a retaining feature that enables the cord to be firmly clamped in place. DC power supply modules are available in various DC input ranges. making the ZT 210 Series ideal for a wide range of applications where specific DC voltage levels are required. DC power supply modules provide pluggable screw terminals on the front panel for DC power input. A four-position connector is provided on both AC and DC power supply modules for two output voltages (+5 and +12VDC) and their grounds. This is useful for powering other circuits or peripherals in embedded systems such as flat panel displays or panel mounted disk drives. Three LED power indicators are also provided on the front panel for monitoring the +5, +12, and -12VDC output voltages. A toggle on/off switch for system power and a push-button reset switch is also found on the front panel.

Environmental

The ZT 210 Series card cages are designed to withstand the shock and vibration levels found in most industrial environments. Both card cages and power supply modules are tested to meet IEEE specification P1156 for shock and vibration.

All card cage models of the ZT 210 Series can operate in the extended temperature range of -40° to +85° C. Individual power supply modules have their own operating temperature ratings specified in the tables that follow. Individual STD or STD 32 cards also have their own operating temperature specifications. Ziatech offers "CT" (-40° to +85° C) and "LT" (-40° to +70° C) cards for extended temperature operation. The forced-air cooling option on ZT 210 card cages may be necessary for applications using 486 processor cards to keep the processor case temperature within its specified operating range. Refer to the operating manual of the processor card for air flow requirements.

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Specifications (Card cages) **Electrical**

 Compatible with ZTP100 Series AC Power Supply Modules and ZT P200 Series DC Power Supply Modules using DIN 41612 connector.

Mechanical

- Physical Dimensions (see attached mechanical drawings)
- Backplane Connectors
 - P1: Modular power supply connector: 15-pin female DIN 41612 (EPT#114-40080) rated at the following:
 - 15A maximum current per pin
 - 500 insertions minimum (DIN Class I)

Px: Dual 136-pin STD 32 card-edge connectors rated at the following:

- 10A maximum current per card (2A per pin)
- 30 milliohms maximum contact resistance
- 2 pF/slot without cards at 1 MHz 200 insertions minimum
- Forced-air cooling option provides 300 feet per minute of airflow over the cards within card cage.

Environmental (ZT 210 Series Card Cage Models)		
Operating Temperature	-40° to +85° Celsius	
Storage Temperature	-55° to +125° Celsius	
Non-Condensing Relative Humidity	5% to 95% at 40° Celsius	
Non-Operating Shock *	30g for 6ms	
Operating Shock *	15g for 11ms	
Non-Operating Vibration *	5 to 300 Hz at 0.35mm (5g)	
Operating Vibration *	5 to 300 Hz at 0.35mm (5g)	

^{*} Meets or exceeds IEEE Specification P1156

Specifications (Modular Power Supplies) ZT P100 Series (AC Power Supply Modules) Electrical

- Compatible with ZT 210 Series card cages
- Automatic selecting of low (90 to 132VAC) or high (175 to 265VAC) input range
- 75% efficiency
- · AC input line fuse protected, internally located
- Voltage indicator LEDs for +5, +12, and -12VDC output status

to the second second second second	Min.	Тур.	Max.
Total Continuous Output Power	OW	distance of a Te	75W
Peak Power Output (60 seconds)		atumae 🖼	110W
AC Input Voltage	90VAC	ta Greenio est	265VAC
AC Input Frequency	47Hz		440Hz
+5VDC Output Voltage	4.75V	5.00V	5.25V
+12VDC Output Voltage	11.40V	12.00V	12.60V
-12VDC Output Voltage	-12.60V	-12.00V	-11.40V
+5VDC Output Current	0A		8.0A
+12VDC Output Current **	0.5A	BUNGALON	3.0A
-12VDC Output Current	OA	Boxes to	1.0A

- * Total maximum DC output power not to exceed 75W.
- ** If +12V at 3A is used, maximum +5V current is 5A.

noto	Min.	Тур.	Max.
Total Continuous Output Power	0W	nebille	150W
Peak Power Output (60 seconds)	Bul youse	ibei spa	176W
AC Input Voltage (low range)	90VAC	110VAC	132VAC
AC Input Voltage (high range)	180VAC	220VAC	264VAC
AC Input Frequency Range	47Hz		63Hz
+5VDC Output Voltage	4.75V	5.00V	5.25V
+12VDC Output Voltage	11.40V	12.00V	12.60V
-12VDC Output Voltage	-12.60V	-12.00V	-11.40V
+5VDC Output Current	0A	V today	15.0A
+12VDC Output Current	0A	Attente C-1	5.0A
-12VDC Output Current	0A	A Secretary	1.0A

^{*} Total maximum DC output power not to exceed 150W.

Mechanical

- Physical dimensions (see attached mechanical drawings)
- Connectors
 - P1: Power input (AC power supplies): IEC 320 male connector
 - P2: DC output: four position AMP MATE-N-LOK #770827 mating connector (AMP MATE-N-LOK #1-480426-0)
 - P3: Backplane interface (H15 male DIN 41612 meets or exceeds IEEE specification P1156)



Environmental (ZT P100 Serie	s AC Power Supply Modules)		
Operating Temperature	0° to 65° Celsius		
Storage Temperature	-40° to +85° Celsius		
Non-Condensing Relative Humidity	5% to 95% at 40° Celsius		
Non-Operating Shock *	30g for 6ms		
Operating Shock *	15g for 11ms (100 50 18 18 18 18 18 18 18 18 18 18 18 18 18		
Non-Operating Vibration *	5 to 300 Hz at 0.35mm (5g)		
Operating Vibration *	5 to 300 Hz at 0.35mm (5g)		

*	Meets	or	exceeds	IEEE	SI	pecification	PI	1156	
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DC Power Supply Modules Electrical

- All DC modules provide:
 - reverse input voltage protection
 - short circuit protection
- 80% efficiency
- Voltage indicator LEDs for +5, +12, and -12VDC output status

PARS TO SHAME	Min.	Тур.	Max.
Total Continuous Output Power	OW	N region	55W
DC Input Voltage	10VDC	hugtu© 3	20VDC
Input Current (full load)	epallo	V JugjuO t	5.7A
+5VDC Output Voltage	4.75V	5.00V	5.25V
+12VDC Output Voltage	11.40V	12.00V	12.60V
-12VDC Output Voltage	-12.60V	-12.00V	-11.40V
+5VDC Output Current	0A	nixem te	5.00A
+12VDC Output Current	0A		1.25A
-12VDC Output Current	0A		1.25A

The starting management of the	Min.	Тур.	Max.
Total Continuous Output Power	OW	080	75W
DC Input Voltage	18VDC	OG :	36VDC
Input Current (full load)	#77082	LOK	3.86A
+5VDC Output Voltage	4.75V	5.00V	5.25V
+12VDC Output Voltage	11.40V	12.00V	12.60V
-12VDC Output Voltage	-12.60V	-12.00V	-11.40\
+5VDC Output Current	0A		7.50A
+12VDC Output Current	0A		1.56A
-12VDC Output Current	0A		1.56A

Service A. Commence A. C. Commence A. A. A.	Min.	Тур.	Max.
Total Continuous Output Power	OW	Silver and	75W
DC Input Voltage	36VDC	niac soli	72VDC
Input Current (full load)			1.90A
+5VDC Output Voltage	4.75V	5.00V	5.25V
+12VDC Output Voltage	11.40V	12.00V	12.60V
-12VDC Output Voltage	-12.60V	-12.00V	-11.40\
+5VDC Output Current	0A	beivh	7.50A
+12VDC Output Current	0A	amai .	1.56A
-12VDC Output Current	0A	rt 19-1	1.56A

Mechanical

- Physical dimensions (see attached mechanical drawings)
- Connectors
 - P1: Power input: Three position pluggable screw terminal with screw fasteners.

 Mating connector: (Phoenix #1777992)
 - P2: DC output: four-position AMP MATE-N-LOK #770827 mating connector: AMP MATE-N-LOK #1-480426-0
 - P3: Backplane interface: H15 male DIN 41612

Environmental (ZT P200 Serie	s DC Power Supplies)
Operating Temperature	-20° to +80° Celsius
Storage Temperature	-40° to +125° Celsius
Non-Condensing Relative Humidity	5% to 95% at 40° Celsius
Non-Operating Shock *	30g for 6ms
Operating Shock *	15g for 11ms
Non-Operating Vibration *	5 to 300 Hz at 0.35mm (5g)
Operating Vibration *	5 to 300 Hz at 0.35mm (5g)

^{*} Meets or exceeds IEEE specification P1156

Ordering Information

Order ZT 210 Series card cages from the card cage ordering guide below. Removable AC or DC power supply modules are separately as accessories.

Base Part Number:

ZT 210 - 09TF0

Card Slot Options (including Slot X):

09 Nine slots12 Twelve slots15 Fifteen slots

18 Eighteen slots

21 Twenty-one slots

Mounting Options:

T Table mount W Wall mount

R Rack mount (only available with 15-, 18-,

and 21-slot models)

Fan Options:

F0 No fans (convection cooling only)
F1 Bottom mounted fan units included

Power Supply Accessories:

ZT P101 75 watt AC Power Supply Module with AC power cord and locking bale

ZT P102 150 watt AC Power Supply Module with AC power cord and locking bale

ZT P201 10 to 20VDC Power Supply Module with pluggable screw terminals

ZT P202 18 to 36VDC Power Supply Module with pluggable screw terminals

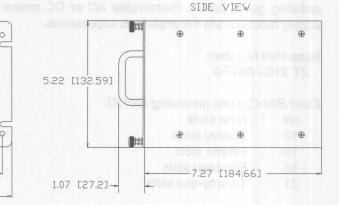
ZT P203 36 to 72VDC Power Supply Module with pluggable screw terminals

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. Two-year warranty on fans. See the full warranty statement in the *Technical Data Book* appendix.



FRONT VIEW



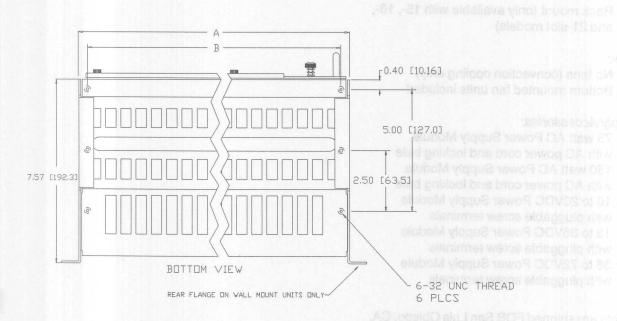
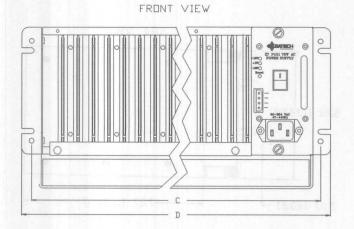
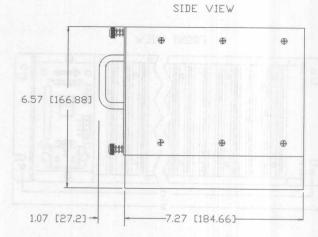


TABLE AND WALL MOUNT VERSIONS

WITH P101 OR P200 SERIES POWER SUPPLY, NO FANS

WITH P101 OR	P200 SERIES F	POWER SUPPLY,	NO FANS	Vinenaw II.
		TABLE MOUNT	WALL	MOUNT
PART NUMBER	А	В	С	D
ZT 210-09	8.88 [225.6]	8.17 [207.5]	9.50 [241.3]	10.30 [261.6]
ZT 210-12	10.76 [273.3]	10.05 [255.3]	11.38 [289.1]	12.18 [309.4]
ZT 210-15	12.63 [320.8]	11.92 [302.8]	13.25 [336.6]	14.04 [356.6]
ZT 210-18	14.50 [368.3]	13.79 [350.3]	15.12 [384.1]	15.91 [404.1]
ZT 210-21	16.39 [416.3]	15.67 [398.0]	17.01 [432.1]	17.80 [452.1]





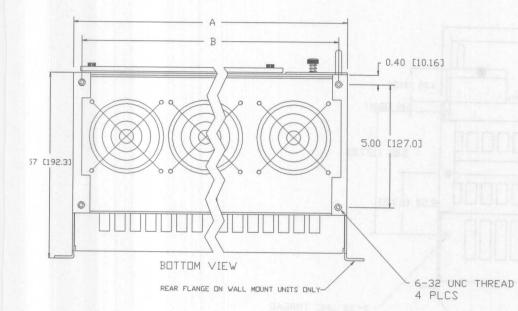


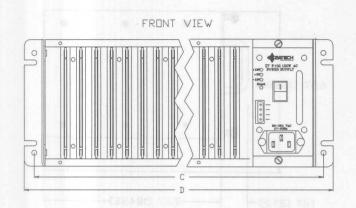
TABLE AND WALL MOUNT VERSIONS

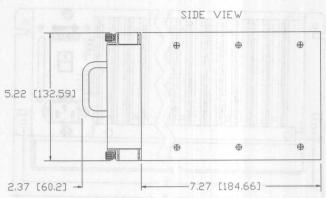
WITH P101 DR P200 SERIES POWER SUPPLY, WITH FANS

			TABLE MOUNT	WALL	MOUNT
PART	NUMBER	A	В	С	D
ZT	210-09	8.88 [225.6]	8.17 [207.5]	9.50 [241.3]	10.30 [261.6]
ZT	210-12	10.76 [273.3]	10.05 [255.3]	11.38 [289.1]	12.18 [309.4]
ZT	210-15	12.63 [320.8]	11.92 [302.8]	13.25 [336.6]	14.04 [356.6]
ZT	210-18	14.50 [368.3]	13.79 [350.3]	15.12 [384.1]	15.91 [404.1]
ZT	210-21	16.39 [416.3]	15.67 [398.0]	17.01 [432.1]	17.80 [452.1]

inches [millimeters]







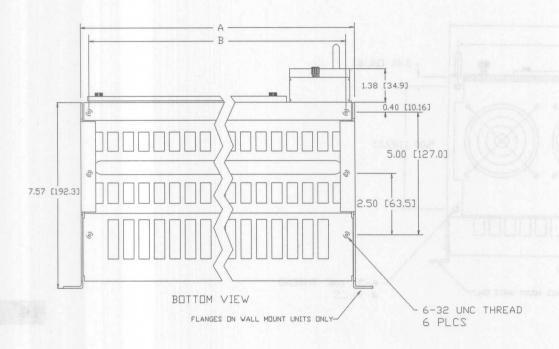
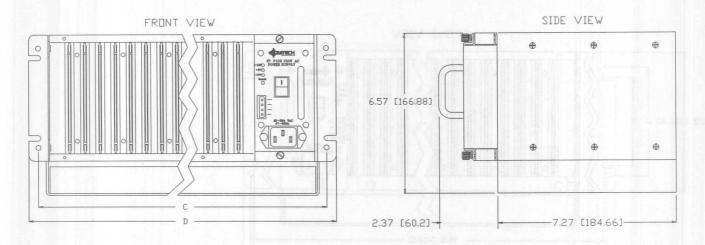
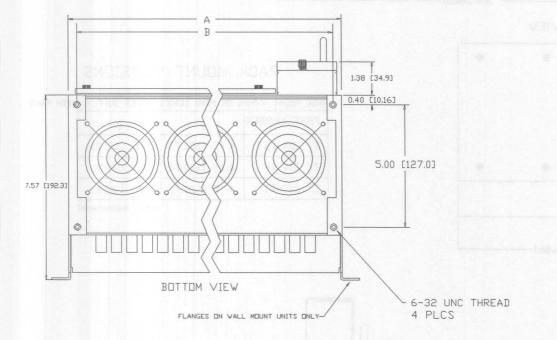


TABLE AND WALL MOUNT VERSIONS

WITH P102 POWER SUPPLY, NO FANS

				TABLE	MOUNT		WALL	MOUNT	
PART	NUMBER		A		В		С	1889	D
ZT	210-09	8.88	[225.6]	8.17	[207.5]	9.50	[241.3]	10.30	[261.6]
ZT	210-12	10.76	[273.3]	10.05	[255.3]	11.38	[289.1]	12.18	[309.4]
ZT	210-15	12.63	[320.8]	11.92	[302.8]	13.25	[336.6]	14.04	[356.6]
ZT	210-18	14.50	[368.3]	13.79	[350.3]	15.12	[384.1]	15.91	[404.1]
ZT	210-21	16.39	[416.3]	15.67	[398.0]	17.01	[432.1]	17.80	[452.1]





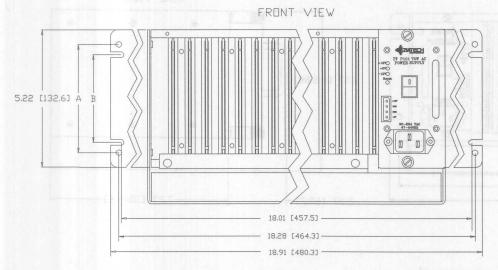
14

TABLE AND WALL MOUNT VERSIONS

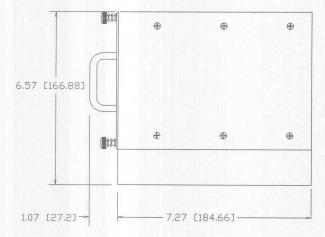
WITH P102 POWER SUPPLY, WITH FANS

		TABLE MOUNT	WALL	MOUNT	
PART NUMBER	А	В	С	D	
ZT 210-09	8.88 [225.6]	8.17 [207.5]	9.50 [241.3]	10.30 [261.6]	
ZT 210-12	10.76 [273.3]	10.05 [255.3]	11.38 [289.1]	12.18 [309.4]	
ZT 210-15	12.63 [320.8]	11.92 [302.8]	13.25 [336.6]	14.04 [356.6]	
ZT 210-18	14.50 [368.3]	13.79 [350.3]	15.12 [384.1]	15.91 [404.1]	
ZT 210-21	16.39 [416.3]	15.67 [398.0]	17.01 [432.1]	17.80 [452.1]	





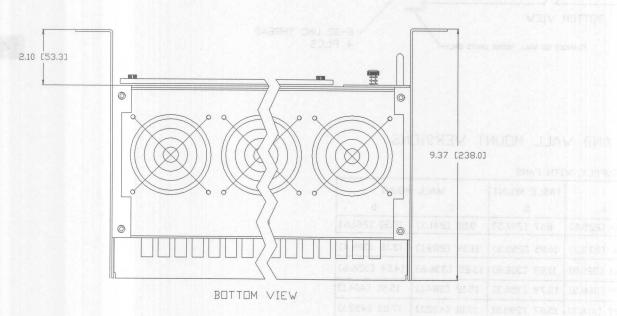
SIDE VIEW

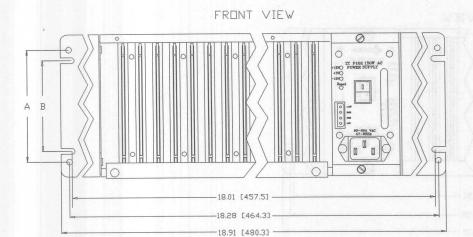


RACK MOUNT VERSIONS

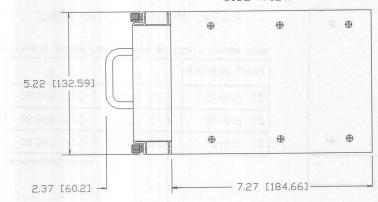
RACK MOUNT W/P101 OR P200 SERIES POWER SUPPLY, WITH FANS

PART NUMBER	2	A	В
ZT 210-15	4.75	[120.7]	3.50 [88.9]
ZT 210-18	4.75	[120.7]	3.50 [88.9]
ZT 210-21	4.75	[120.7]	3.50 [88.9]





SIDE VIEW

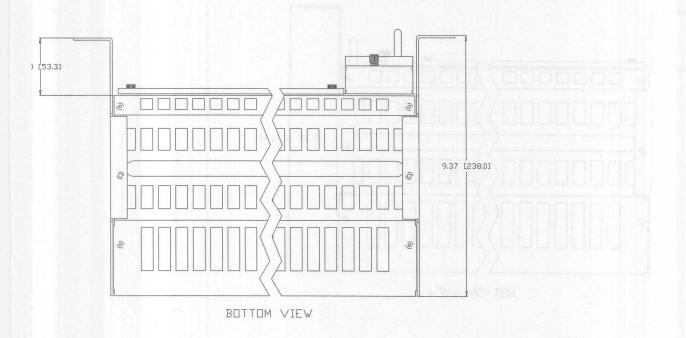


RACK MOUNT VERSIONS

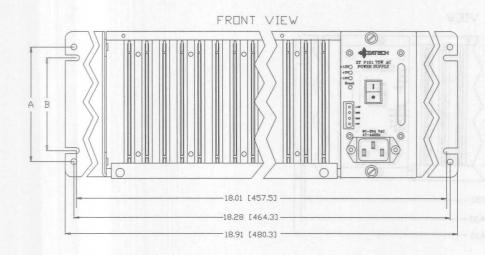
RACK MOUNT W/P102 POWER SUPPLY, NO FANS

		001121) 110 17
PART NUMBER	A I S	В
ZT 210-15	4.75 [120.7]	3.50 [88.9]
ZT 210-18	4.75 [120.7]	3.50 [88.9]
ZT 210-21	4.75 [120.7]	3.50 [88.9]

inches [millimeters]







SIDE VIEW 5.22 [132.59] • • • •

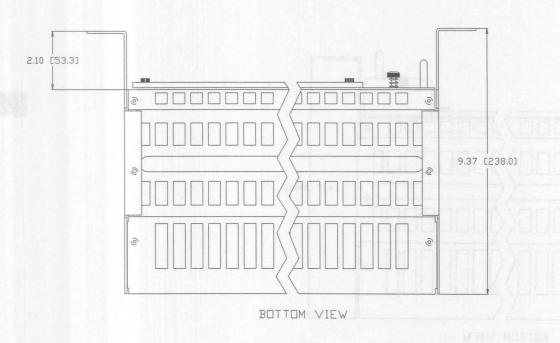
7.27 [184.66] —

1.07 [27.2]

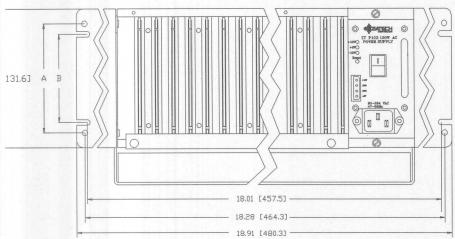
RACK MOUNT VERSIONS

RACK MOUNT W/P101 OR P200 SERIES POWER SUPPLY, NO

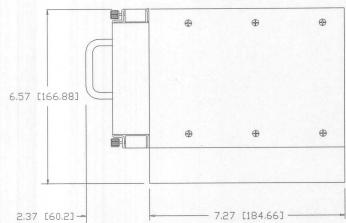
PART NUMBER	А	В
ZT 210-15	4.75 [120.7]	3.50 [88.9]
ZT 210-18	4.75 [120.7]	3.50 [88.9]
ZT 210-21	4.75 [120.7]	3.50 [88.9]







SIDE VIEW

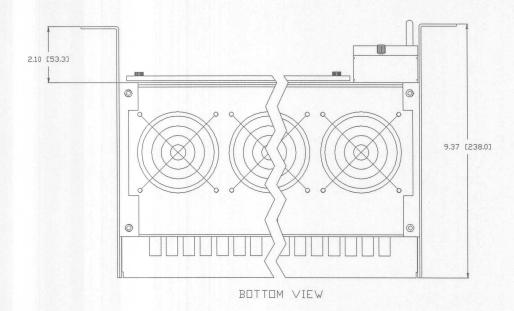


RACK MOUNT VERSIONS

RACK MOUNT W/P102 POWER SUPPLY, WITH FANS

PART NUMBER	А	В
ZT 210-15	4.75 [120.7]	3.50 [88.9]
ZT 210-18	4.75 [120.7]	3.50 [88.9]
ZT 210-21	4.75 [120.7]	3.50 [88.9]

inches [millimeters]

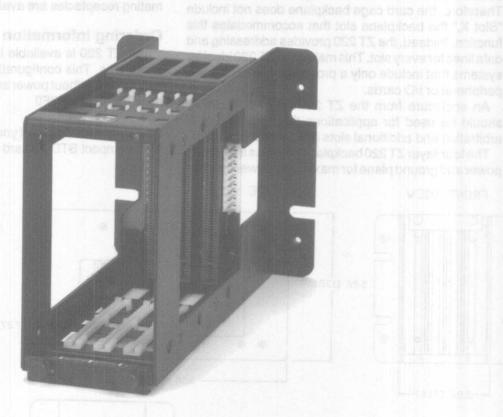




Small STD 32® card cage for embedded processor applications that don't require bus arbitration (Slot X)

The ZT 220 is an open frame card cage designed for embedded processor applications that require just a few STD 32 or STD Bus cards, and don't require Slot X. The backplane enables cards used in the card cage to make 8-, 16- and 32-bit data transfers. The ZT 220, in its 3-slot configuration, is 2.82 inches (7.2cm) wide,

excluding wall mount brackets. The ZT 220's rigid steel construction features a corrosion resistant, powder coated finish. Ziatech's removable DC to DC power supplies (ZT 88CT85) can power the card cage or power can be supplied from an external AC or DC power supply.



- 3-slot width available (0.625" [15.9mm] centers)
- 3-U EURO cage format; height: 5.22" (13.3cm)
- · 8-, 16-, and 32-bit data transfers
- STD 32-compatible (except Slot X functions) and STD Bus-compatible
- Four layer STD 32 backplane without Slot X
- Steel powder coated construction
- Integral card restraint
- · Power connector for external power supplies



Functional Considerations

Mechanical

The ZT 220's compact dimensions (see mechanical drawings) make it ideal for embedded applications. It easily wall mounts to any vertical surface using brackets on the rear of the card cage. While normally turned outward, these brackets can also be reversed so they extend inward and do not extend beyond the width of the card cage body.

The card cage is constructed of rigid steel. A locking bar on the bottom of the card cage retains cards in applications where shock and vibration exists. The card cage is finished in a corrosion-resistant black powder coating.

Backplane

The ZT 220 is designed to house extremely compact control systems that do not require bus arbitration. Therefore, the card cage backplane does not include "Slot X," the backplane slot that accommodates this function. Instead, the ZT 220 provides addressing and data lines for every slot. This makes the ZT 220 ideal for systems that include only a processor card and a few peripheral or I/O cards.

An enclosure from the ZT 200 or ZT 210 Series should be used for applications that require Slot X arbitration and additional slots (i.e., multiprocessing).

The four-layer ZT 220 backplane provides a separate power and ground plane for maximized power distribu-

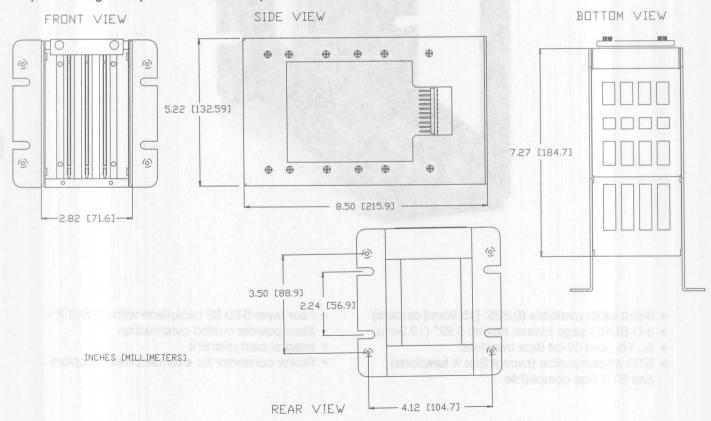
tion, noise immunity, and signal integrity. Maximum trace separation minimizes signal crosstalk. High quality power decoupling capacitors on the backplane prevent power fluctuations in the system due to high-current output switching or input power fluctuations.

The 136-pin STD 32 connectors used on the ZT 220 backplane are rated at 2 amps per pin, making them ideal for plug-in STD power supply cards like the ZT 88CT85, which uses five +5VDC power pins, one +12VDC power pin, one -12VDC power pin, and twelve ground pins. For connecting external power supplies to the ZT 220 card cage, the backplane includes an AMP MTA-156 post header (0.156" [4mm] centers). This is a 10-position friction lock, straight square post header (0.045" [1.1mm]), with polarizing notches (AMP part# 1-640445-0). This connector enables the ZT 220 to utilize DC power from an external source. Several mating receptacles are available from AMP.

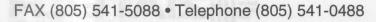
Ordering Information

The ZT 220 is available in one configuration as of press time. This configuration is a 3-slot backplane, wall mount, without power supply, or fans. It is ordered as: ZT 220-03WP0F0

Please contact Ziatech if you have other requirements for a compact STD 32 card cage without Slot X.



Mechanical dimensions of the ZT 220



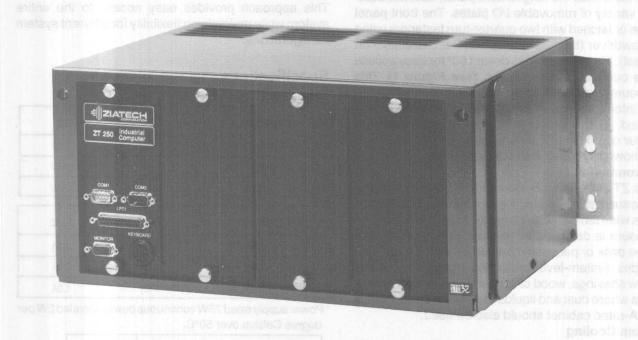


The ZT 250 Industrial Computer Enclosure is designed for STD 32 and STD Bus systems operating in rugged and electrically noisy environments. Inside the shock and vibration resistant enclosure is a 15-slot card cage with a low-noise backplane and a power supply. The integrated backplane design accommodates 8-, 16-, and 32-bit data transfers, and uses multilayer construction, controlled layer separation, and trace sizing for impedance control.

The ZT 250 enclosure is designed to wall mount to any vertical surface or inside a NEMA cabinet, but can

also be configured for table top (without fans) or pedestal mounting. The ZT 250 has space in front of the card cage for connecting I/O to the front panel or to I/O access plates, or extending I/O cabling out of the side of the enclosure. The front panel with removable I/O plates is designed to hinge down for easy access to STD cards.

The ZT 250 enclosure is UL approved and has an FCC Part 15, Class A certification.



- · Rugged, steel enclosure
- · Corrosion resistant, powder coated finish
- Shock and vibration resistant (IEEE P1156)
- Integral card restraint
- 9-, 12-, and 15-slot backplanes
- STD 32 connectors
- Accepts STD 32 and STD CPU and I/O cards
- 75W fused switching power supply
- UL approved

- FCC Part 15, Class A device certified
- 0° to 55° Celsius operating range
- Forced-air cooling option
- IEC power input socket
- Supports universal power input range
- Hinged front panel provides easy card access
- Removable I/O access plates
- Cable port on side for routing I/O cables



Functional Considerations

Electrical

The ZT 250 Industrial Computer Enclosure includes a Ziatech STD 32 backplane equipped with a choice of 15, 12, or 9 slots on 0.625" (15.88mm) centers. Steel construction provides maximum electromagnetic emission control. The backplanes protect signal integrity with multilayer construction, controlled layer separation, and trace sizing for impedance control. An IEC connector on the left side of the unit provides power to the unit. The power supply accepts inputs ranging from 90 VAC to 264 VAC while providing +5, +12, and -12V to the backplane. The ZT 250 is U. L. approved and FCC, Part 15, Class A certified. (Note: FCC certification was obtained using a specific configuration with all front plates mounted to minimize electromagnetic interference. Other configurations may differ.)

Mechanical

The ZT 250 Industrial Computer Enclosure consists of a card cage, front panel, and power supply. A sturdy bezel surrounds the hinged front panel, accommodating a variety of removable I/O plates. The front panel can be unlatched with two quarter-turn fasteners using a screwdriver (thumbscrew versions are available on request). The panel swings down 180° for easy access to the cards and power switch (see Figure 1). This enclosure is also designed to minimize electromagnetic interference and is FCC Part 15, Class A device certified. The entire unit has a corrosion resistant powder coat finish. The dimensions of this enclosure are shown in Figure 2 on the back page.

Environmental

The ZT 250 enclosure is intended for harsh environments susceptible to a high level of shock and vibration over a wide temperature range (0° to 55° Celsius). The enclosure is designed for vertical wall mounting, but can be desk or pedestal mounted as well. The ZT 250 provides system-level protection from falling debris (screw shavings, wood chips, etc.). In severe environments where dust and liquids may affect the system, a NEMA-rated cabinet should also be used.

System Cooling

The standard enclosure is convection cooled with slots in the forward bottom and louvres in the top rear. This ventilation induces air flow across the power supply and circuit boards. As an option the ZT 250 can be purchased with three bottom-mounted fans that provide up to 63 cubic feet per minute (CFM) of air flow. The ZT 250 cannot be table mounted if equipped with fans.

Input/Output

The ZT 250 has unique I/O accessibility. The front panel is hinged to provide access to the entire card cage, power switch, and fuse as illustrated in *Figure 1*. Many I/O access plates are available from Ziatech, providing front panel I/O connections for the STD cards within. I/O access plates can also be fabricated by the



Figure 1. Hinged front panel swings down from the ZT 250 chassis for easy accessibility and maintenance.

user. When ordering plates, a "system" plate should be ordered for placement on the far left side of the front panel, then a combination of plates equaling 15 slot widths should be ordered to complete the front panel. The ZT 250 also has internal space in front of the card cage for extending I/O cabling out the side of the unit. This approach provides easy access to the entire system while maintaining flexibility for different system configurations.

Specifications Electrical

Output Voltage	Min.	Max.
DC Output Voltage +5V	4.75V	5.25V
DC Output Voltage +12V	11.40V	12.60V
DC Output Voltage -12V	-12.60V	-11.40V

Output Current	Min.	Max.
DC Output Current +5V*	0.0A	8.0A
DC Output Current +12V*	0.0A	3.0A
DC Output Current -12V*	0.0A	1.0A

* Power supply rated 75W continuous power. Derated 2W per degree Celsius over 50°C.

AC Power Input	Min.	Max.
AC Voltage ·	90VAC	264VAC
AC Frequency	47Hz	440Hz
Power Consumption	22W	115W

Mechanical

See Figure 2 on the back page for dimensions.

Environmental		
Operating Temperature	0° to 55° Celsius	
Storage Temperature	-40° to +85° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

Mechanical (continued)

- · Non-operating shock: 30g for 6ms
- · Operating shock: 15g for 11ms
- Non-operating vibration: 5 to 300 Hz at 0.35mm (0.01") (5g)
- Operating vibration: 5 to 300 Hz at 0.35mm (0.01") (5g)
- Meets IEEE specification P1156

Ordering Information

The ZT 250 Industrial Enclosure is available in three STD 32 backplane widths. The external dimensions of the ZT 250 do not change with different backplane slot widths. A forced-air cooling option is available that mounts three fans on the bottom of the unit. The ZT 250 comes with wall mount brackets and mounting hardware. A ZT 250 with fans cannot be table mounted.

A ZT 250 with fifteen card slots and convection cooling would be ordered as: ZT 250-15F0.

ZT 250-xFx Industrial Computer Enclosure

Slot Options:

- 09 Nine slots
- 12 Twelve slots
- 15 Fifteen slots

Fan Options:

- FO Convection cooling (no fans)
- F1 Forced-air cooling (three bottom mounted fans)

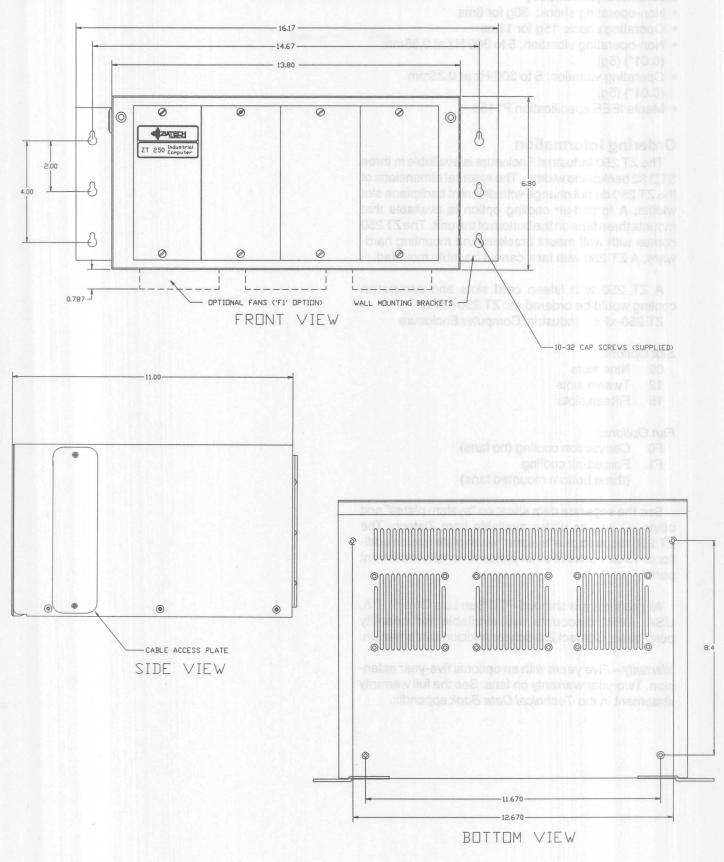
See the separate data sheet on "system plates" and other I/O access plates available from Ziatech. The ZT 250 requires one "system" width plate and an additional 15 slot-units of other plates to complete the front panel.

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. Two-year warranty on fans. See the full warranty statement in the *Technical Data Book* appendix.



Figure 2. ZT 250 Industrial Computer Enclosure mechanical dimensions

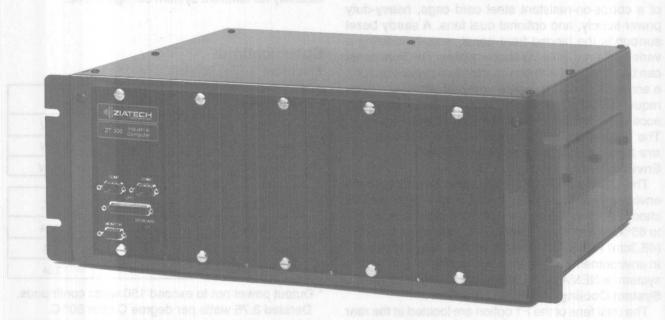


A 19" rack-mountable, rugged enclosure equipped with a high-performance backplane providing 8-, 16-, and 32-bit data transfers for the STD 32® Bus

The ZT 300 Industrial Computer Enclosure from Ziatech is designed for STD 32 and STD Bus systems operating in rugged and electrically noisy environments. Inside the shock and vibration resistant enclosure is a 24-slot card cage with a low-noise backplane, dual fans, and a heavy-duty power supply. The integrated backplane design accommodates 8-, 16-, and 32-bit data transfers, while utilizing multilayer

construction, controlled layer separation, and trace sizing for impedance control.

The ZT 300 is designed to fit into a 19" (48.3cm) RETMA rack or wall mount to any vertical surface. I/O cables can be routed through a channel to the rear of the unit for easy access. The front panel has removable I/O plates and is designed to hinge down. The ZT 300 is UL and FCC Part 15, Class A device approved.



- · Rugged, steel enclosure
- Corrosion resistant powder coated finish
- Shock and vibration resistant
- Integral card restraint
- 12-, 15-, 24-slot backplanes
- STD 32 connectors
- Accepts STD 32 and STD CPU and I/O cards
- 150W fused switching power supply
- · U. L. approved

- FCC Part 15, Class A device certified
- 0° to 65° Celsius operating temperature range
- Dual fan forced-air cooling or open-frame option
- Sized to fit all RETMA 19" (48.3cm) racks (4U)
- IEC power input socket
- · Supports universal power input range
- · I/O cables can be channelled to the rear of the unit
- Hinged front panel provides easy card access
- Removable I/O access plates



Functional Considerations

Electrical

The ZT 300 Industrial Computer Enclosure includes a Ziatech STD 32 backplane available in 12, 15, or 24 STD 32 slot widths on 0.625" (15.88mm) centers. Steel construction provides maximum electromagnetic emission control. The backplanes protect signal integrity with multilayer construction, controlled layer separation, and trace sizing for impedance control. Power is provided to the unit through an IEC connector on the back of the unit. The heavy-duty power supply accepts inputs ranging from 85VAC to 264VAC while providing +5, +12, and -12V to the backplane. The ZT 300 is UL and FCC, Part 15, Class A certified. (Note: FCC certification was obtained using a specific configuration with all front plates mounted to minimize electromagnetic interference. Other configurations may differ.)

Mechanical

The ZT 300 Industrial Computer Enclosure consists of a corrosion-resistant steel card cage, heavy-duty power supply, and optional dual fans. A sturdy bezel surrounds the hinged front panel, accommodating a variety of removable I/O access plates. The front panel can be unlatched with two quarter-turn fasteners using a screwdriver (thumb screw versions are available on request). The panel swings down 90° for simple, easy access to the cards and power switch (see Figure 1). The dimensions of this enclosure are shown in Figure 2 on the back page of this data sheet.

Environmental

The ZT 300 enclosure is intended for use in harsh environments that are susceptible to a high level of shock and vibration over a wide temperature range (0° to 65° Celsius). The enclosure is designed to fit all 19" (48.3cm) RETMA racks (4U vertical space required). In environments where dust and liquids may affect the system, a NEMA-rated cabinet should also be used. **System Cooling**

The dual fans of the F1 option are located at the rear of the unit and provide up to 42 cubic feet per minute (CFM) of air flow across the power supply and circuit boards. As an option, the ZT 300 can be purchased without the fans and top/bottom covers. This configuration allows heat dissipation in 19" racks that already provide some form of cooling.

Input/Output

The ZT 300 has unique I/O accessibility. The front panel is hinged to provide access to the entire card cage, power switch, and fuse as illustrated in *Figure 1*. Many I/O access plates are available from Ziatech, providing front panel I/O connections for the STD cards within. I/O access plates can also be fabricated by the user.

When ordering plates, a "system" plate should be ordered for placement on the far left side of the front panel, then a combination of plates equaling 20 slot-

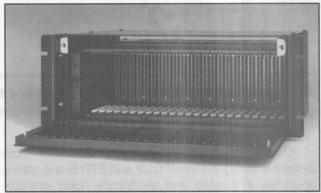


Figure 1. Hinged front panel swings down from the ZT 300 chassis for easy accessibility and maintenance.

widths should be ordered to complete the front panel. The ZT 300 also has a channel for extending I/O cabling to the rear of the unit. This approach provides easy access to the entire system while maintaining flexibility for different system configurations.

Specifications Electrical

Output Voltage	Min.	Max.
DC Output Voltage +5V	4.75V	5.25V
DC Output Voltage +12V	11.40V	12.60V
DC Output Voltage -12V	-12.60V	-11.40V

Output Current	Min.	Max.
DC Output Current +5V*	0.0A	20.0A
DC Output Current +12V*	0.0A	6.0A
DC Output Current -12V*	0.0A	2.0A

* Output power not to exceed 150 watts continuous. Derated 3.75 watts per degree C over 50° C.

AC Power Input	Min.	Max.
AC Voltage (low range)	85VAC	132VAC
AC Voltage (high range)	170VAC	264VAC
AC Frequency	47Hz	440Hz
Power Consumption	stelest honerd.	215W

Machanica

See Figure 2 on back page for dimensions

Environmental	
Operating Temperature	0° to 65° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

Mechanical (continued)

- · Non-operating shock: 3G for 6ms
- · Operating shock: 15G for 11ms
- Non-operating vibration: 5 to 100 Hz at 0.35mm (5G)
- Operating vibration: 5 to 100 Hz at 0.35mm (5G)

Ordering Information

The ZT 300 Industrial Enclosure is available with a choice of three STD 32 backplane widths. A forced-air cooling option is available that mounts two completely enclosed fans onto the rear of the unit.

A ZT 300 with fifteen slots and convection cooling would be ordered as: ZT 300-15F0.

ZT 300-xFx Industrial Computer Enclosure

Slot Options:

- 12 Twelve slots
- 15 Fifteen slots
- 24 Twenty-four slots

Fan/Sheet metal Options:

- FO Convection cooling (no fans, open-frame enclosure without top and bottom sheet metal)
- F1 Forced-air cooling (dual rear-mounted fans, completely enclosed top and bottom)

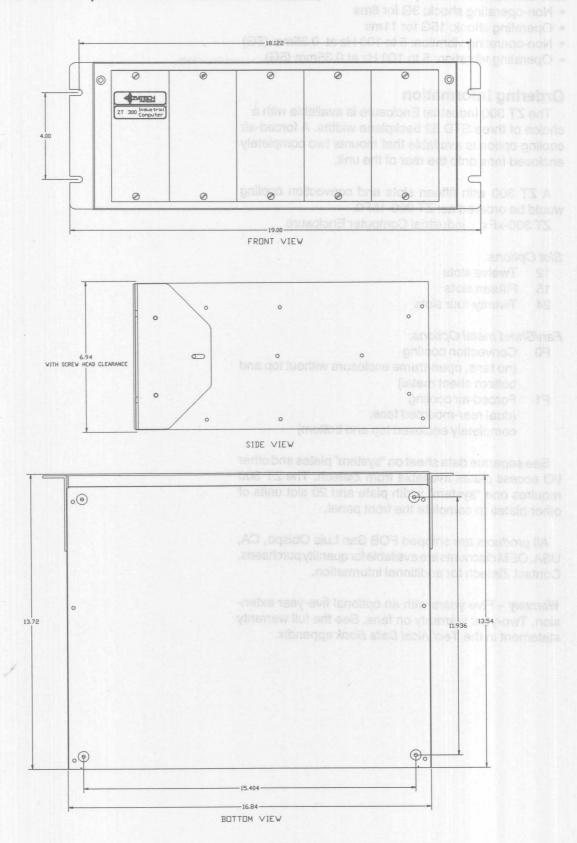
See separate data sheet on "system" plates and other I/O access plates available from Ziatech. The ZT 300 requires one "system" width plate and 20 slot units of other plates to complete the front panel.

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. Two-year warranty on fans. See the full warranty statement in the *Technical Data Book* appendix.



Figure 2. ZT 300 Industrial Computer Enclosure mechanical dimensions

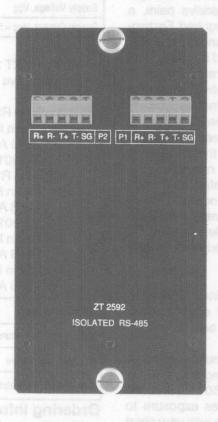


A five-slot plate that connects two RS-232 channels to optically isolated RS-422/485 channels for use in electrically noisy environments

The ZT 2592 is an I/O access plate for ZT 250 and ZT 300 Industrial Enclosures. Active circuitry on the back of the plate enables RS-232 ports on Ziatech's STD Bus processors to interface to RS-485 devices in industrial environments. Noise immunity and suppression are provided to protect the RS-422/485 interface as well as the CPU board.

The two separate RS-232 channels can interface to a wide range of connectors found on Ziatech boards. RS-232 connectors, in 5-, 10-, and 14-pin configurations, are provided for operation up to 64 Kbaud.

The two RS-485 channels can be utilized in a multidrop configuration with 2- or 4-wire systems. Multidrop termination resistors are also included. The ZT 2592 is available with or without optical isolation for both RS-485 channels.



- Mounts to front of ZT 250 and ZT 300 Industrial Enclosures
- Compatible with RS-232 ports on all Ziatech CPU cards
- Two optically isolated channels (optional)
- Supports baud rates to 64kHz
- RS-422/485 multidrop, 2- or 4-wire
- RS-232 loopback of unused signals
- Suppresses and survives up to 3kV spikes
- · Burned-in at 55° C and tested to guarantee reliability



Functional Considerations RS-232 Capability

When installed in a ZT 250 or ZT 300 enclosure, the ZT 2592 allows the user to access two RS-485 networks. The ZT 2592 must be connected via a cable to the system's RS-232 connector.

The ZT 90109 and ZT 90104 cables are available for 14- and 10-pin RS-232 connectors. Contact Ziatech for 3- and 5-pin cables.

The ZT 2592 is powered through separate +5V and ground pins on the RS-232 interface cable. Unused RS-232 signals, such as DSR and DTR, RTS, and CTS, can be looped back using jumpers on the ZT 2592. If RS-485 multidrop operation is desired, DTR can be jumpered to enable and disable the RS-485 transceivers.

RS-422/485 Capability

A user must build a twisted-pair cable to externally connect to an RS-422/485 network. For four-wire systems using separate transmit and receive pairs, a shielded two-pair cable with ground is required. For two-wire systems using the same transmit and receive pair, a shielded single-pair cable with ground is required. (In both system types, Belden 8102 is recommended.)

The ZT 2592 has provisions for network and high impedance terminations. Network terminators (typically 120 ohms) are located at either end of the RS-485 cable to reduce reflections. A jumper has been provided to install the termination resistor when the ZT 2592 is installed at the beginning or end of the network.

High impedance terminations are useful if an RS-485 transmitter is not currently driving the network. These terminations maintain a 200mV differential between signals to ensure that the network is in a known state. On the ZT 2592, these resistors are installed in a socket for easy removal if necessary.

Noise Suppression

The ZT 2592 is designed for continued operation when exposed to a wide variety of environmental stimuli. Ziatech uses several tests to assure that the ZT 2592 can withstand the stimuli.

The surge voltage test is used to simulate exposure to inductive or capacitive load switching and lightning strikes of nearby power lines. A 3kV, 50 microsecond pulse is used. A spark test simulates exposure to mechanical relay contacts and signals with very short rise times. This is accomplished with a 5kHz, 2kV burst with a rise time of five nanoseconds. The final test is a combination of both the surge and spark tests above.

All test stimuli are isolated from the computer by the optical and capacitive isolation techniques built into the ZT 2592.

The environmental stimuli used in these tests are derived from IEC 801.1-5, Electronic Equipment for Industry and Trade, and several Swedish and German standards.

Optical Isolation

Optical isolation for both channels may be ordered as an option. Optical isolation provides further protection for the computer in electrically noisy environments, or from different ground potentials.

An on-board DC/DC connector supplies power for the optical isolators and 125 422/485 drivers and receivers from the computer's +5V power source.

Specifications

Electrical

With optical isolation:

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	\$11 1 1.75 157	325mA	780mA

· Without optical isolation:

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, VCC = 5.0V	- 21	165mA	400mA

Mechanical

- Mounts in ZT 250 and ZT 300 enclosures
- · Occupies five slot units
- Connectors
 - J1: 3-pin RS-232
 - J2: 14-pin RS-232 vertical header mates with T & B Ansley 622-1430 (ZT 90109-compatible)
 - J3: 3-pin RS-232
 - J4: 14-pin RS-232 vertical header mates with T & B Ansley 622-1430 (ZT 90109-compatible)
 - J5: 10-pin RS-232 vertical header mates with T & B Ansley 500-1030
 - J6: 10-pin RS-232 vertical header mates with T & B Ansley 500-1030

Environmental	
Operating Temperature	0° to 65° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

Ordering Information

ZT 2592-A0 Dual-channel RS-232 to RS-485 converter in a five-slot plate. Requires one of the cables listed below for each channel.

ZT M2592 ZT 2592 manual

Optical Isolation Options:

A0 No optical isolation included
A1 Optical isolation for both channels

Accessories

Cables (see Data Book cable section for details):

ZT 90109 8" (20.3cm) cable for 14-pin RS-232 ports ZT 90104 13" (33cm) cable for 10-pin RS-232 ports



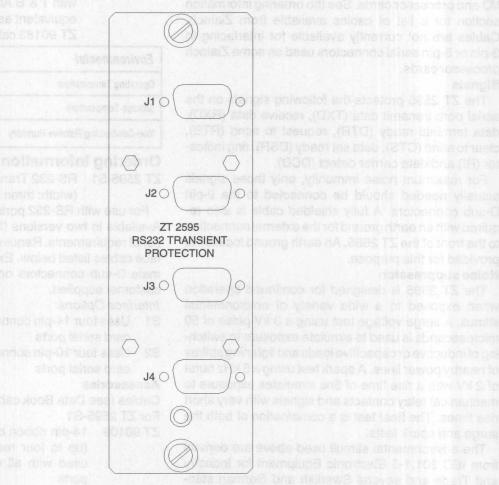
ZT 2595

RS-232 Transient Protection

A three-slot plate providing transient protection for up to four RS-232 channels in electrically noisy environments

The ZT 2595 is an I/O access plate for ZT 250 and ZT 300 Industrial Computer Enclosures. Circuitry on the ZT 2595 provides Ziatech systems with transient protection and noise immunity for up to four RS-232 serial interfaces. This protection is necessary to protect the serial ports and the computer, when used in areas where high voltage transients are possible and in electrically noisy environments.

The ZT 2595 interfaces to the 14-pin and 10-pin serial ports used on Ziatech serial I/O boards and most Ziatech processor boards. Four metal 9-pin D-subminiature connectors are provided on the front of this three slot-wide plate for external user connections to serial devices.



- Mounts to front of ZT 250 and ZT 300 Industrial Computer Enclosures
- Compatible with RS-232 ports on Ziatech's I/O and CPU cards
- Four transient protected RS-232 channels
- · Suppresses and survives up to 3 kV spikes
- Burned-in at 55° C and tested to assure reliability



Functional Considerations

When used on a Ziatech ZT 250 or ZT 300 Industrial Computer Enclosure, the ZT 2595 protects up to four RS-232 serial channels from electrical noise on the serial lines and dangerous transient spikes. Four metal male D-sub (DB-9) connectors are found on the front of the ZT 2595 Transient Protection plate.

Interfacing

The ZT 2595 is available in two versions depending on the serial connections used on the back. The ZT 2595-S1 provides four 14-pin serial headers, while the ZT 2595-S2 provides four 10-pin serial headers. Both versions of the ZT 2595 have four D-sub connectors on the front side.

Three different cables are available for interfacing between the ZT 2595 and the serial ports used on serial I/O and processor cards. See the ordering information section for a list of cables available from Ziatech. Cables are not currently available for interfacing to 3-pin or 5-pin serial connectors used on some Ziatech processor cards.

Signals

The ZT 2595 protects the following signals on the serial port: transmit data (TXD), receive data (RXD), data terminal ready (DTR), request to send (RTS), clear to send (CTS), data set ready (DSR), ring indicator (RI) and data carrier detect (DCD).

For maximum noise immunity, only those signals actually needed should be connected to the 9-pin D-sub connectors. A fully shielded cable is also required with an earth ground for the external connection to the front of the ZT 2595. An earth ground location is provided for this purpose.

Noise suppression

The ZT 2595 is designed for continued operation when exposed to a wide variety of environmental stimuli. A surge voltage test using a 3 kV pulse of 50 microseconds is used to simulate exposure to switching of inductive or capacitive loads and lightning strikes of nearby power lines. A spark test using a 5 kHz burst of 2 kV with a rise time of 5ns simulates exposure to mechanical relay contacts and signals with very short rise times. The final test is a combination of both the surge and spark tests.

The environmental stimuli used above are derived from IEC 801.1-5 Electronic Equipment for Industry and Trade and several Swedish and German standards. These standards have been applied to the TXD and RXD signals on each of the four RS-232 channels using circuitry with a combination of gas tubes, ferrite beads and transzorbs. For the remaining RS-232 signals, protection of a lesser extent is provided using only transzorbs.

Specifications

Mechanical

- Mounts in ZT 250 and ZT 300 Industrial Computer Enclosure front bezels.
- Three slot-units in width
- Connectors

ZT 2595-S1

- J1 J4: 9-pin male metal D-sub connector, mates with AMP 747523-1
- P1 P4: 14-pin dual row vertical header, mates with T&B Ansley 622-1430 or equivalent as used on ZT 90109 cable

ZT 2595-S2

- J1 J4: 9-pin male metal D-sub connector, mates with AMP 747523-1
- P1 P4: 10-pin dual row vertical header, mates with T & B Ansley 622-1030 or equivalent as used on ZT 90104 and ZT 90183 cables

Environmental	
Operating Temperature	-55° to +125° Celsius
Storage Temperature	-55° to +125° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

Ordering Information

ZT 2595-S1 RS-232 Transient Protection plate (width: three slots)

For use with RS-232 ports on most Ziatech boards. Available in two versions (S1 and S2) depending on serial requirements. Requires one or more serial interface cables listed below. External cabling to the 9-pin male D-sub connectors on the front of the plate is customer supplied.

Interface Options:

- S1 Uses four 14-pin connectors for interface to STD card serial ports
- S2 Uses four 10-pin connectors for interface to STD card serial ports

Accessories

Cables (see Data Book cable section for details): For ZT 2595-S1

ZT 90109 14-pin ribbon cable, ten inches in length (up to four required with ZT 2595-S1), used with all cards using 14-pin serial ports

For ZT 2595-S2

ZT 90104 10-pin ribbon cable, 13 inches in length (up to four required with ZT 2595-S2), used with all cards using 10-pin serial ports

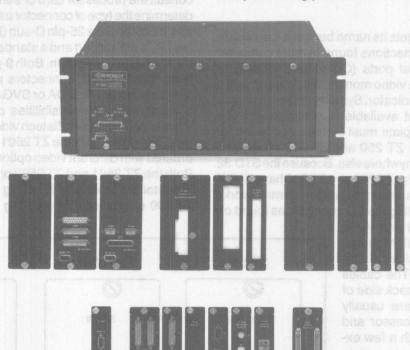
ZT 90183 40-pin to four 10-pin cable, ten inches in length (one required with ZT 2595-S2), used with ZT 8932 Intelligent Serial Controller



I/O breakout plates in a number of widths bring STD I/O to the front panel of ZT 250 and ZT 300 Industrial Computer Enclosures

The ZT 2500 Series of removable I/O access plates are used to complete the front panel of ZT 250 and ZT 300 Industrial Computer Enclosures. The series includes blank plates, as well as plates with I/O connectors and cables for bringing I/O connections found on STD 32® and STD cards to the front of the enclosure. Plates are also available for easy user access to front panel mass storage media such as floppy disks and PCMCIA cards. The number of ZT 2500 Series plates continues to grow as new STD 32 cards are created, and new user requirements emerge.

ZT 2500 Series plates are available in a number of different widths including the unique "system" width, as well as one, two, three, and five slot-unit widths. The "system" width plates must be mounted on the far left-hand side of the ZT 250 or ZT 300 enclosure, while all other plates can be mounted anywhere to the right side of the system plate. All ZT 2500 Series plates are constructed of steel with a durable black powder coating. Grounding lugs are provided on a number of plates, and stainless steel thumbscrews are used for easily removing plates from the enclosure.



- · Sturdy, steel construction
- Corrosion resistant powder coated finish
- Available in "system", one, two, three, and five slot-unit widths
- Easily removable with large stainless steel thumbscrews
- Serial, parallel, video, keyboard, network and other types of I/O supported
- · Mass storage access plates available
- Provides FCC Part 15, Class A device shielding for enclosure when installed
- · Shock and vibration resistant



4 /

Functional Considerations

Mechanical

The ZT 2500 Series Removable I/O Access Plates are required to complete the front panels of the ZT 250 and ZT 300 Industrial Computer Enclosures. Additionally, the plates bring the I/O found on STD 32 and STD Bus cards to the front of the enclosure through cables mounted on the back side of the plate. Some plates use printed circuit boards on the back for converting or signal conditioning I/O signals into a standard configuration, while most plates simply use cables with panel mount connectors. The mass storage access plates simply provide an opening for floppy and PCMCIA drives to extend to the front surface of the plate for easy user access. Blank plates are used to fill in the front panel after the "system" width plate and all other I/O or mass storage access plates have been mounted in the ZT 250 or ZT 300 hinged front bezel. Blank plates are available in a variety of widths for accomplishing this

System Plates

The system plate gets its name because it is usually used for the I/O connections found in most computer systems: Two serial ports (COM1 and COM2), a printer port (LPT1), a video monitor, a keyboard, and a system power LED indicator. System plates are unique in width and are not available in standard slot unit widths. The system plate must be mounted to the far left-hand side of the ZT 250 and ZT 300 bezel, and cannot be mounted anywhere else. Because the STD 32 backplanes used in the ZT 250 and ZT 300 have Slot X on the far left side, the system plate arrangement works well for accommodating the I/O connections found on

the processor board and video card, which are usually mounted on the left-hand side of the STD 32 backplane. The cables extending from the back side of the system plates are usually attached to the processor and video cards only, with a few exceptions. A blank system plate exists for ZT 250 and ZT 300 applications where the "system" I/O connections are not desired on the front panel of the enclosure.

After the system plate is installed in the bezel of a ZT 250 or ZT 300, a fixed number of slot units are available for additional plates as shown below:

 ZT 250: 15-slot units remaining

 ZT 300: 20-slot units remaining Depending on individual system requirements, any ZT 2500 Series plate can be installed to fill this remaining area after the system plate is installed. Blank plates should be selected last.

ZT 2501-Vx

The ZT 2501 System Plate has two 25-pin D-subminiature (DB-25) connectors for the COM1 and COM2 serial port connections in addition to the printer, video and keyboard connectors, and power LED. The ZT 2501 is intended for interfacing to Ziatech processor cards or serial I/O cards that use 14-pin headers for the serial connectors.

ZT 2502-Vx

The ZT 2502 System Plate uses 9-pin D-sub (DB-9) connectors for COM1 and COM2 serial connections. The ZT 2502 is used with processor cards or serial cards using 10-pin headers for the serial port. Please consult the processor card or serial card data sheet to determine the type of connector used. Both the ZT 2501 and ZT 2502 use a 25-pin D-sub (DB-25) connector for the LPT1 printer port and a standard DIN connector for the keyboard connection. Both 9-pin D-sub and 15-pin high density D-sub connectors are available for the video connection to MDA or SVGA/VGA monitors with a variety of cable possibilities on the back side for interfacing to different Ziatech video/keyboard controllers. Therefore, both the ZT 2501 and ZT 2502 can be ordered with different video options (V1, V2, V3, etc.). Both the ZT 2501 and ZT 2502 provide an LED power indicator that connects to a plug inside the ZT 250 or ZT 300 enclosure for indicating when the system is

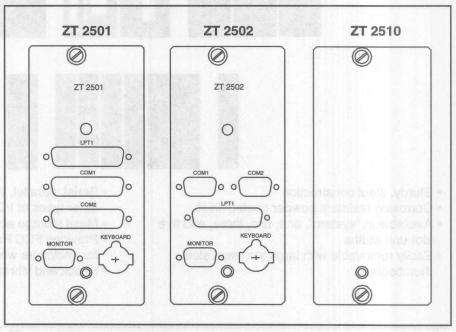


Figure 1. The ZT 2501, ZT 2502, and ZT 2510 System plates

powered. Please see the ordering information at the end of this data sheet, or the latest price list from Ziatech, for the available ordering options.

ZT 2510

The ZT 2510 Blank System Plate is a blank plate for systems that do not extend the standard system I/O connections out to the front of the ZT 250 or ZT 300 enclosure. Like the ZT 2501 and ZT 2502, the ZT 2510 is unique in width and can only be mounted on the far left side of the enclosure bezel.

STD 32[®] STAR SYSTEM™ Video/Keyboard Access Plate

ZT 2503-Vx

The ZT 2503 Video/Keyboard Access Plate is a 2 slot-width plate providing video output and keyboard input access for temporary

ZT 2503

ZT 2503

MONITOR

KEYBOARD

+

Figure 2. The ZT 2503 STD 32 STAR SYSTEM Video/Keyboard Access Plate

master processors used in STD 32 STAR SYSTEMs. A typical STAR SYSTEM may have several temporary master processors. The narrow width of the ZT 2503 is designed to accomodate this arrangement, and may be ordered in several different configurations (V1, V2, V3, etc.) for interfacing to different Ziatech video/keyboard controllers. Several serial and parallel I/O access plates are also available to interface to that type of I/O found on temporary master processors.

ZT 2521 ZT 2521 PCMCIA ACCESS ZT 2522 FLOPPY DISK ST 2523 FLOPPY DISK ST 2523 FLOPPY DISK ST 2523 FLOPPY DISK ST 2523 FLOPPY DISK

Figure 3. The ZT 2521, ZT 2522, and ZT 2523 Mass Storage Access Plates

Mass Storage Access Plates

Mass storage access plates provide front panel user access to removable media mass storage devices. These access plates are essentially blank plates with holes in them to allow specific versions of STD drives to extend to the front panel of ZT 250 and ZT 300 enclosures.

ZT 2521

The ZT 2521 PCMCIA "PC CARD" Access Plate is five slot-units in width and provides access to the dual PCMCIA slots of the ZT 8921-M1. The ZT 2521 also provides a thumbscrew locking mechanism to reduce vibration of the extended PCMCIA card connector used on the ZT 8921-M1, in applications where shock and vibration is present.

ZT 2522

The ZT 2522 Floppy Disk Access Plate is a three slotunit plate providing front panel access to the ZT 8950-D1M floppy disk controller.

ZT 2523

The ZT 2523 Floppy Disk Access Plate is similar to the ZT 2522, except it is 2 slot-units in width and is used with the low profile (narrow) ZT 8954-D1M floppy disk controller.

Digital I/O Access Plates

Two I/O access plates are available that support digital I/O connections to Ziatech boards incorporating digital I/O ports. Both of these plates provide two Optocompatible 50-pin connectors on the front of the plate. **ZT 2531**

The ZT 2531 Industrial I/O Adapter Plate is three slotunits in width. This plate converts the high density 56-pin I/O connector (48-points of digital I/O) into two

> Opto-compatible male 50-pin connectors (24-points each with alternating grounds). This plate uses a printed circuit board on the back side to accomplish the signal transition with a 56-pin cable being used to attach to the STD board. This plate also provides diode protection for each digital I/O line with a clamp diode pair between +Vcc and ground, thus shunting voltage transients to either +Vcc or ground. Power jumpers are provided as well for pin 49 of each front panel connector. The ZT 90089 56-pin cable (1m) is included with the ZT 2531. Ziatech boards using the high density 56-pin digital I/O connector include the ZT 8801, ZT 8802, and ZT 8901 processor boards.



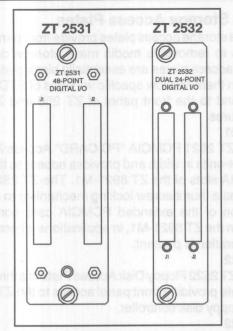


Figure 4. The ZT 2531 and ZT 2532 Digital I/O Access Plates

ZT 2532

The ZT 2532 Dual 24-Point Digital I/O Plate occupies just two slot-units. It is a simple extender plate for extending the Opto-compatible 50-pin digital I/O connections found on many Ziatech I/O and processor boards to the front of the ZT 250 or ZT 300 enclosure. Two male 50-pin connectors are found on the front of the plate with two 50-pin cables extending to the following boards: ZT 8845, ZT 8846, ZT 88CT49, ZT 88CT72, ZT 89CT61, ZT 8902, and ZT 8911.

Serial I/O Access Plates

A large number of I/O access plates are available for supporting serial communications ports of various kinds. These plates include support for standard RS-232 COM ports, Ethernet and ARCNET interfaces, modem telephone lines and PLC serial communications. **ZT 2541**

The ZT 2541 Quad DB-25 Serial Plate is three slotunits in width, bringing the serial port signals of the 14-pin headers found on a number of Ziatech boards out to 25-pin male D-sub connectors. The signal pinout on the DB-25 connectors is the same as the IBM personal computer standard when connected to any Ziatech processor board or serial board using the 14-pin dual-row header. The boards using this 14-pin header include the following: ZT 8809A, ZT 8830, ZT 8832, ZT 8901, ZT 88CT41, ZT 88CT75, and zSBX CT32.

ZT 2542

The ZT 2542 is a Dual DB-25 Serial Plate occupying two slot-units. It is identical to the ZT 2541 except it only provides two serial port connectors on the plate and

can therefore only interface to two 14-pin serial ports on the boards listed above.

ZT 2543

The ZT 2543 Dual RJ-11 Serial Plate is a two-slot plate extending two RJ-11 telephone style socket connectors to the front panel. It interfaces to STD boards using RJ-11 connectors such as the ZT 8843 modem card and the ZT 89CT90-D4 ARCNET interface with twisted-pair transceiver.

ZT 2544

The ZT 2544 Dual DB-9 Serial Plate is a two-slot plate bringing two AT pinout-compatible 9-pin D-sub

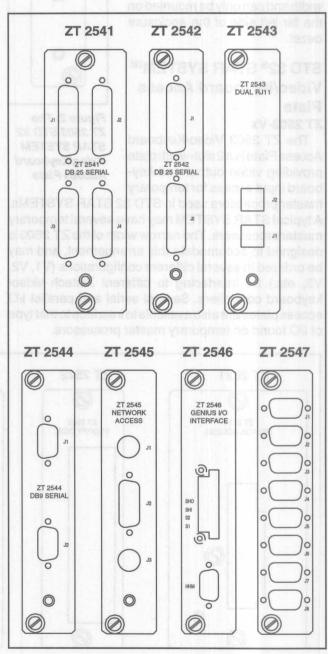


Figure 5. The ZT 2541, ZT 2542, ZT 2543, ZT 2544, ZT 2545, ZT 2546, and ZT 2547 Serial I/O Access Plate

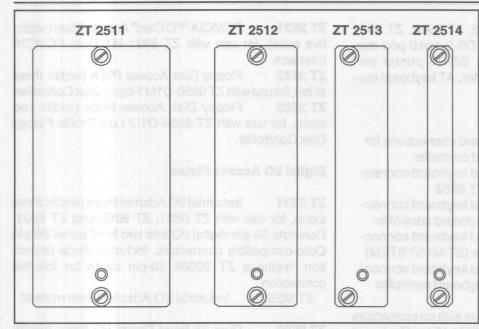


Figure 6. The ZT 2511, ZT 2512, ZT 2513, and ZT 2514 Blank Plates

connectors to the front, while connecting inside the enclosure to two 10-pin dual-row serial headers used on several Ziatech processor cards. Ziatech processor cards using 10-pin serial headers include the ZT 8802, ZT 8902, and ZT 8911.

ZT 2545

The ZT 2545 Network Access Plate is a two slot-unit plate with two cutouts for panel mount coaxial connectors and a cutout for a panel mount DB-15 connector. This plate accommodates users who want to provide their own coaxial cabling to ARCNET (ZT 89CT90) and Ethernet (ZT 8895) cards for star or multidrop connections. The DB-15 cutout is for Ethernet users desiring to use the DB-15 AUI interface for 10BASE5 networks. ZT 2546

The ZT 2546 GE FANUC GENIUS™ I/O Interface Plate is two slot-units wide with two connectors. A 6-position 5mm connector is used for the GE GENIUS I/O network interface, while a standard DB-9 connector is used for connecting GE's Hand Held Monitor (HHM). This plate supports Ziatech's ZT 88CT93 STDIM™ for GE Fanuc Genius I/O.

ZT 2547

The ZT 2547 Octal DB-9 Serial Plate is a two slot-unit plate with eight D-sub connectors on the front. It can be ordered with different cable options to extend the serial port connections of Ziatech processor boards. The ZT 90119 cable converts a 10-pin header as used on many Ziatech processor cards to an AT-compatible 9-pin male D-sub connector. Up to eight ZT 90119 cables can be used with the ZT 2547. The ZT 90183 cable converts the 40-pin header used on the ZT 8932 Intelligent, Multi-Channel Serial Controller into four 9-pin male D-sub connectors. Up to two ZT 90183

cables can be used with the ZT 2547 to support the eight serial ports on the ZT 8932.

Blank Plates

Blank plates should be selected after the System Plate and all other I/O or Mass Storage Access Plates have been attached to the ZT 250 or ZT 300 Industrial Computer Enclosure's front bezel. The blank plates come in four widths as shown below. A ZT 250 has 15 slot-units of front panel area remaining after the unique width system plate is installed, and the ZT 300 has 20 slot-units of panel area remaining after the system plate is installed.

ZT 2511

The ZT 2511 Blank Plate is five slot-units in width and the most cost effective method for filling in large areas of space on the front panel.

ZT 2512

The ZT 2512 Blank Plate is three slot-units in width and another good choice when large areas remain on the front panel after installing other plates.

ZT 2513

The ZT 2513 Blank Plate is a two-slot-unit plate. **ZT 2514**

The ZT 2514 Blank Plate is a one-slot-unit plate.

Ordering Information System Plates

The following plates are used on the far left side of the ZT 250 and ZT 300 enclosures to extend COM ports, printer port, video, keyboard, and the system power LED to the front panel. A blank "system width" plate should be used if a ZT 2501 or ZT 2502 is not used.

ZT 2501-V1 Use with ZT 8809A and ZT 8901 (width: "System"). Includes two DB-25 serial port connectors (COM1, COM2), one DB-25 printer port connector (LPT1, for ZT 8809A only), video connector, AT keyboard connector, and system power LED. A printer emulation cable (ZT 90156) is also available for the ZT 8901.

Video and Keyboard Options:

- V1 MDA and keyboard connections for ZT 8842
- V2 SVGA/VGA and keyboard connections for ZT 8842 and ZT 8982



4 /

ZT 2502-V1 Use with ZT 8802, ZT 8902, ZT 8911 (width: "System"). Includes two DB-9 serial port connectors (COM1, COM2), one DB-25 printer port connector (LPT1), video connector, AT keyboard connector, and system power LED.

Video and Keyboard Options:

- V1 MDA (DB-9) and keyboard connections for ZT 8842 video/keyboard controller
- V2 SVGA/VGA (DB-15) and keyboard connections for ZT 8842 and ZT 8982
- V3 SVGA/VGA (DB-15) and keyboard connections for zVID1 video/keyboard controller
- V4 SVGA/VGA (DB-15) and keyboard connections for multiple zVID1s (STAR SYSTEM)
- V5 SVGA/VGA (DB-15) and keyboard connections for zVID2 video/keyboard controller

ZT 2510 Blank System Plate with no connectors (width: "System"). STAR SYSTEM Video/Keyboard Access Plates.

STD 32 STAR SYSTEM Video/Keyboard Access Plate

ZT 2503-V1 Video/Keyboard Access Plate (width: two slots), provides additional video and keyboard connector on a non-system plate for STD 32 STAR SYSTEM temporary master processors.

Video and Keyboard Options:

- V1 MDA (DB-9) and keyboard connections for ZT 8842 video/keyboard controller
- V2 SVGA/VGA (DB-15) and keyboard connections for ZT 8842 and ZT 8982
- V3 SVGA/VGA (DB-15) and keyboard connections for zVID2 video/keyboard controller
- V4 SVGA/VGA (DB-15) and keyboard connections for multiple zVID2s (STAR SYSTEM)
- V5 SVGA/VGA (DB-15) and keyboard connections for zVID2 video/keyboard controller

Blank Plates

Blank plates are used to fill open space in the front panel area of ZT 250 and ZT 300 enclosures after all other plates have been inserted.

ZT 2511	Blank Plate (width: five slots)
ZT 2512	Blank Plate (width: three slots)
ZT 2513	Blank Plate (width: two slots)
ZT 2514	Blank Plate (width: one slot)

Mass Storage Access Plates

The following plates provide front panel access to mass storage devices using removable media.

ZT 2521 PCMCIA "PC Card" Access Plate (width: five slots), for use with ZT 8921-M1 Dual PCMCIA Interface.

ZT 2522 Floppy Disk Access Plate (width: three slots), for use with ZT 8950-D1M Floppy Disk Controller.

ZT 2523 Floppy Disk Access Plate (width: two slots), for use with ZT 8954-D1M Low Profile Floppy Disk Controller.

Digital I/O Access Plates

ZT 2531 Industrial I/O Adapter Plate (width: three slots), for use with ZT 8801, ZT 8802 and ZT 8901. Converts 56-pin digital I/O into two front panel 50-pin Opto-compatible connectors. Includes diode protection. Includes ZT 90089 56-pin cable for internal connection.

ZT M2531 Industrial I/O Adapter Plate manual

ZT 2532 Dual 24-Point Digital I/O Plate (width: two slots), extends two 50-pin connectors used on the ZT 8845, ZT 8846, ZT 88CT49, ZT 88CT72, ZT 89CT61, ZT 8902, and ZT 8911 to the front of the plate.

Serial I/O Access Plates

ZT 2541 Quad DB-25 Serial Plate (width: three slots), for use with all Ziatech boards using 14-pin serial headers. Extends 14-pin serial ports used on ZT 88CT41, ZT 88CT75, ZT 8901, zSBX32, ZT 8832, ZT 8830, and ZT 8809A to four DB-25 connectors on the front of the plate.

ZT 2542 Dual DB-25 Serial Plate (width: two slots), for use with all Ziatech boards using 14-pin serial headers. Same as ZT 2541 except has just two DB-25 serial connectors.

ZT 2543 Dual RJ-11 Serial Plate (width: two slots), extends two RJ-11 connectors to front panel. For use with ZT 8843 or ZT 89CT90-D4.

ZT 2544 Dual DB-9 Serial Plate (width: two slots), extends 10-pin serial ports used on ZT 8902, ZT 8911, and ZT 8802 to two DB-9 connectors.

ZT 2545 Network Access Plate (width: two slots), provides two round front panel holes so users can mount their own coax connectors and cables for Multidrop and STAR connections to the ZT 89CT90 ARCNET and ZT 8895 Ethernet interfaces. A panel cutout for a DB-15 connector is also provided for ZT 8895 users who wish to use the AUI interface for 10BASE5 networks. Call Ziatech for cable requirements.

ZT 2546 GE FANUC GENIUS I/O Interface Plate (width: two slots), provides front panel access for ZT 88CT93. A 6-pin, 5mm (0.2") connector is used for the GENIUS I/O interface. A DB-9 connector is used for the interface to GE's Hand Held Monitor (HHM).

ZT 2547 Octal DB-9 Serial Plate (width: two slots), for use with Ziatech processor cards using 10-pin serial headers (ZT 8802, ZT 8902, ZT 8911) and the Intelligent, Multi-Channel Serial Controller (ZT 8932).

Accessories

Cables (see Data Book cable section for details):

ZT 90119 10" (25cm) serial cable, 10-pin header to 9-pin DTE male D-sub connector.

ZT 90182 10" (25cm) serial cable, 40-pin header to four 9-pin male D-sub connectors.

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.



FAX (805) 541-5088 • Telephone (805) 541-0488



A truly industrial workstation based on the rugged STD 32® and STD Bus, the ZT 1000's NEMA 4/12 front panel, and PC/AT software compatibility make it ideal for stand-alone and networking control applications

The ZT 1000 Industrial Workstation is designed for computerized machine and process control in the tough factory environment. This highly-integrated product features a truly industrial STD 32 or STD computer with a human interface. Its solid aluminum front panel meets NEMA 4 and NEMA 12 requirements for resistance to harsh environments. The ZT 1000 can mount in a sealed industrial enclosure or a 19" RETMA rack.

A flush, sealed panel provides access to a floppy disk drive and external keyboard connector, while the standard display panel features a 14-inch high-resolution color monitor, optional touch screen, numeric keypad, and function keypad.

The ZT 1000 can run DOS and other operating systems as well as hundreds of PC-based programs. Yet, unlike PC implementations, it does not require rotating media, and can use more reliable solid state RAM, ROM, and flash disks. Processor choices range from an 8 MHz V20 (8088 compatible) to the 66 MHz 486DX2. Ziatech's Industrial BIOS rounds out the industrial characteristics of the ZT 1000. Every ZT 1000 can be ordered with a wide range of choices for peripheral devices and industrial I/O.



- Solid aluminum NEMA 4 and 12 front panel
- 14" 1024 x 768 (Super VGA) monitor
- Processor choices range from an 8 MHz NEC V20 to a 66 MHz Intel 486DX2
- Flush, sealed front door for access to floppy disk drive and keyboard connector
- · Front panel hinged to chassis for easy maintenance
- STD 32 Bus-based system for maximum reliability and performance
- Multiprocessing capability for combined user interface and control functions
- · Industrial network capability
- · Mounts in 19" RETMA rack or in a NEMA cabinet

- Compatible with numerous operating systems and hundreds of PC software packages
- Compatible with a variety of STD 32 and STD Bus I/O cards
- Rear panel connections for COM1, COM2, LPT1, LPT2, and Network
- Choice of DOS in ROM, floppy disk drive, hard disk drive, or solid state drive options
- Touch-screen option (resistive overlay)
- Twelve spare slots for expansion
- Hard disks available from 80 to 530 Mbytes
- FCC Class B certification



Functional Considerations Rugged Front Panel

Manufactured out of 1/2" aluminum, the ZT 1000 front panel is one of the most solid in the industry. Designed to NEMA 4 and 12 standards, it is impervious to dust and moisture. A sealed door that is flush to the front panel provides front access to floppy or credit card-sized solid state disks and a connector for an external keyboard. The hinged front panel swings away from the ZT 1000 chassis for easy maintenance.

Large Screen and Friendly User Interface

A 14" color SVGA monitor provides users with a

interface. The ZT 1000 can utilize the advanced features provided by STD 32, the extension to the STD-80 specification. These include 16- and 32-bit data transfers, more interrupts, and sophisticated multiprocessing. Choose the Performance for the Job. . .

> The ZT 1000 is available with any choice of processors, peripherals, and I/O boards, depending on the user's requirements.

> STD 32 I/O products. This rich supply of I/O enables the

ZT 1000 to function as a controller, as well as a user

Ziatech processor boards that can be ordered with

the ZT 1000 include the economical 8 MHz NEC V20. the 16 MHz NEC V53 offering 80286 performance, the 25 MHz 486SX, the 33 MHz 486DX, the 50 MHz 486DX2, or the 66 MHz 486DX2.

...Add Standard Peripherals...

Standard peripherals including a wide range of graphics/keyboard controllers are selected to match the processor board.

...and Optional Storage Components...

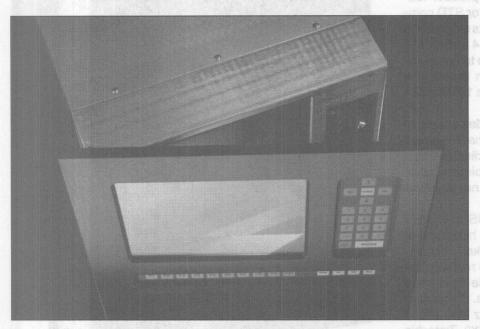
Optional storage components include hard and floppy disk drives, and solid state credit card-sized memory support (PCMCIA 2.0). Floppy disks are accessed

through a front panel door as is a keyboard port.

Like all Ziatech DOS-based systems, the ZT 1000 can operate without rotating media through RAM and ROM disk support built into Ziatech's industrial BIOS.

... Then Add Industrial Interfaces

Up to twelve expansion slots are available to the user. These slots can be used to customize the ZT 1000 to the task at hand, whether it is multiprocessing or application specific. The ZT 1000 accepts any STD 32 and STD Bus I/O, such as analog-to-digital interfaces, extra serial channels, ARCNET or Ethernet interfaces, motion controllers, and much more. Many of these devices are supported by the optional STD Device Driver Package (STD DDP).



Hinged front panel swings away from the ZT 1000 chassis for easy accessibility and maintenance.

large bright display. Membrane pads provide numeric and function key input. A connector for an external keyboard allows for further programming. An optional resistive touch screen makes operator interaction as simple as pointing.

A Tough STD 32 Backplane

The STD 32 Bus gives the ZT 1000 its true industrial nature. This not only provides the ZT 1000 with an intrinsically rugged and reliable computer core, it also makes the removal and installation of cards easy. A rear-mounted STD 32 card rack means that cards can be inserted and removed from the back of the ZT 1000 without sliding out assemblies or removing motherboards. All active computer components are easily replaceable.

The STD 32 Bus also gives the ZT 1000 user access to the enormous supply of industrial STD and

Specifications

Display

- 14-inch diagonal color Super VGA (1024 x 768 non-interlaced) monitor
- Optional touch-screen panel (resistive)

Keyboards/Keypads

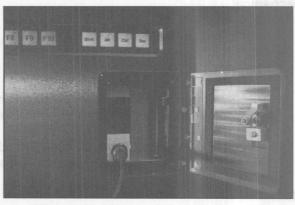
- One numeric sealed membrane keypad which includes four cursor control keys with home; ten numeric keys with decimal, minus, back-space, and enter keys
- One functional sealed membrane keypad with ten function keys and four control keys (alt, shift, escape, and control)
- Standard IBM DIN connector located inside front panel access door for a detachable IBM XT/AT-style keyboard

Communications

- Two 25-pin or 9-pin D-shell connectors provided for serial ports (RS-232, RS-485).
- Two 25-pin D-shell connectors provided for printer support (LPT1, LPT2).

Optional Mass Storage

- 80 to 530 Mbyte hard disk drive option
- 1.44 Mbyte floppy disk drive option
- RAM, ROM, or flash disks
- PCMCIA 2.0 "PC Card" Interface



The front panel access door makes it easy for technical personnel to reprogram the computer.

Connectivity

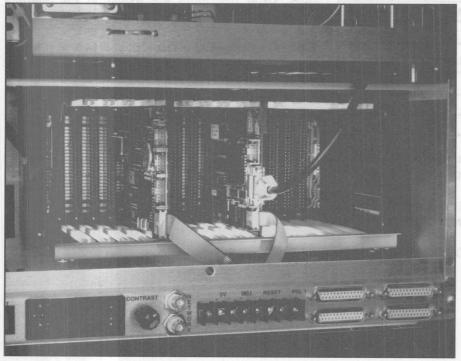
- ARCNET
- Ethernet

Expansion

- Card cage: 15-slot STD 32
- Twelve expansion slots available

Software

- Microsoft® MS-DOS® in ROM is standard
- STD Device Driver Package (STD DDP) option supports industrial I/O from Ziatech and other STD Bus manufacturers



Twelve expansion slots make customizing the ZT 1000 for diverse industrial applications easy.



Mechanical

(43.2cm)D

- Dimensions:
 19.0" (48.3cm)W x 21.0" (53.3cm)H x 17.0"
- Weight: approximately 60 lbs. (27.2Kg)
- Removable plate for cables and strain relief
- · Accessible area on bottom for conduit connections
- Standard dual-fan cooling system with replaceable external filters
- Provisions for mounting in panel cutout or 19" RETMA rack, with allowances for chassis slides

Electrical

- Power: 110/220 VAC at 60/50 Hz for 200 watts, nominal, 275 watts maximum
- External power terminals: +5V at 3A
- External terminal for alarm/bell
- · External terminal for reset/stop

AC Power Input	Min.	Max.
AC Voltage (low range)	90VAC	132VAC
AC Voltage (high range)	180VAC	264VAC
AC Frequency	47Hz	440Hz
Power Consumption	95W	275W

Output Voltage	Min.	Max.
DC Output Voltage +5V	4.75V	5.25V
DC Output Voltage +12V	11.40V	12.60V
DC Output Voltage -12V	-12.60V	-11.40V

Output Current	Min.	Max.
DC Output Current +5V	2A	20A
DC Output Current +12V	0A	6A
DC Output Current -12V	0A	3A

- IEC power connector (rear panel)
- External rear panel terminal for +5 volt source and system reset input
- · Rear panel power switch and reset switch
- Contrast and brightness controls for monitor
- Meets all requirements for FCC Class B industrial devices

Environmental	Oksploy volgario
Operating Temperature	0° to 50° Celsius
Storage Temperature	0° to 70° Celsius
Non-Condensing Relative Humidity	5% to 95% at 40° Celsius

Ordering Information

The minimum configuration for the ZT 1000 is ordered as:

ZT 1000-T0

A ZT 1000 with touchscreen:

Touch Screen

TO No touchscreen

T1 Touchscreen overlay

Note: Any Ziatech STD Bus processor board, from the 8 MHz ZT 8809A Single Board V20 Computer to the 66 MHz 486DX2-based ZT 8911 Scalable Processor Board, can be ordered with the ZT 1000. A number of STD Bus video, mass storage, communication and industrial I/O boards are available as well. A multiprocessing version of the ZT 1000 is another option with Ziatech's STD 32 STAR SYSTEM™. The ZT 1000 comes as an integrated and tested unit from the factory.

nin D-shell competents

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. Two-year warranty on fans. See the full warranty statement in the *Technical Data Book* appendix.



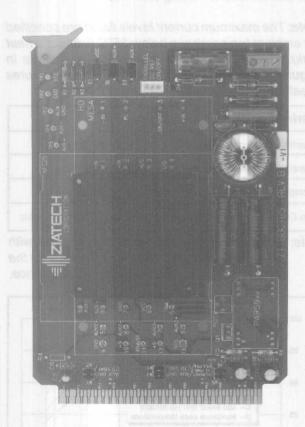
STD Bus DC/DC power supply card provides removable in-rack power

The ZT 88CT85 is a general purpose STD card which provides an easily accessed and removable power source for the STD Bus backplane. A very high-density, high efficiency DC-to-DC converter card, the ZT 88CT85 is suitable for a variety of space-critical applications. These include telecommunications, transportation, distributed power networks, and battery powered systems. The ZT 88CT85's small size conserves

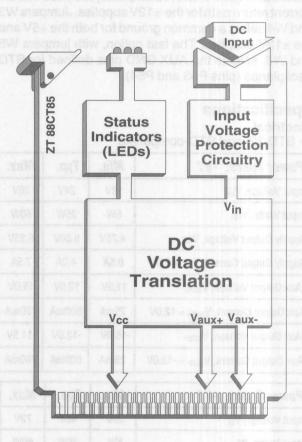
usable backplane space and requires just one slot. This makes compact control systems possible.

The ZT 88CT85 is available in three models offering 12V, 24V, and 48VDC nominal inputs, spanning the range from 9VDC to 72VDC. The ZT 88CT85 maintains a nearly constant 80% efficiency over the entire input voltage range.

Contact Ziatech for special requirements.



- STD 328- and STD Bus-compatible
- Fused and transient input protection
- Processor independent
- · Requires only one card slot
- Extended temperature operation
- 80% power translation efficiency



- LED status indicators
- Wide input voltage range
- Jumper-selectable path for isolated or common ground paths
- Burned-in at 55°C and tested to guarantee reliability

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40° to +85° C. (Users should make adjustments for temperature rise in enclosures.)



Functional Considerations

The ZT 88CT85 has a triple screw terminal input that allows wires up to 14 AWG in diameter to supply the input voltage to the card and a safety earth ground. The input to the ZT 88CT85 is fused and protected from overvoltage conditions.

The output of the ZT 88CT85 is short circuit protected with automatic recovery from short circuit conditions. The board is factory shipped with triple output capability: 5V, +12V, and -12V. This satisfies most computer-based system requirements. (For other input and output configurations, contact Ziatech.)

Ground Path Selection

The ZT 88CT85 provides an isolated 5V, and ±12V supply to the STD 32 and STD Bus. The ground path for the 5V may be isolated from that of the ±12V by selectively jumpering the board. Jumpers W1 and W2 allow VBAT (pin P5 on the backplane) to be used as the current return path for the ±12V supplies. Jumpers W3 and W4 select a common ground for both the +5V and the ±12V supplies. The last option, with jumpers W5 and W6, selects the AUX GND pins defined for STD backplanes (pins P53 and P54).

Specifications

Electrical

• STD 32- and STD-compatible

Power SpecsV1	Min.	Тур.	Max. 36V	
Input Voltage, Vin	18V	24V		
Input Watts, Win	5W	25W	60W	
Supply Output Voltage, Vcc	4.75V	5.00V	5.25V	
Supply Output Current, VCC = 5.0V	0.5A	4.0A	7.5A	
†Aux Output Voltage, V _{aux+}	11.5V	12.0V	15.0V	
Aux Output Current, Vaux+ = 12.0V	25mA	500mA	750mA	
†Aux Output Voltage, V _{aux} -	-15.0V	-12.0V	-11.5V	
Aux Output Current, Vaux- = -12.0V	25mA	500mA	750mA	

Power SpecsV2	Min.	Тур.	<i>Max.</i> 72V
Input Voltage, V _{in}	36V	48V	
Input Watts, Win	5W	25W	60W
Supply Output Voltage, Vcc	4.75V	5.00V	5.25V
Supply Output Current, VCC = 5.0V	0.5A	4.0A	7.5A
†Aux Output Voltage, Vaux+	11.5V	12.0V	15.0V
Aux Output Current, Vaux+ = 12.0V	25mA	500mA	750mA
†Aux Output Voltage, Vaux-	-15.0V	-12.0V	-11.5V
Aux Output Current, Vaux- = -12.0V	25mA	500mA	750mA

Power SpecsV3	Min.	Тур.	Max.	
Input Voltage, Vin	9V	12V	18V	
Input Watts, Win	5W	25W	31W	
Supply Output Voltage, Vcc	4.75V	5.00V	5.25V	
Supply Output Current, VCC = 5.0V	1A	ЗА	5A	
†Aux Output Voltage, V _{aux+} = 12.0V	11.3V	12.0V	13.5V	
Aux Output Current, Vaux+ = 12.0V	0A	0.5A	1A	
†Aux Output Voltage, Vaux- = -12.0V	-13.5V	-12.0V	-11.3V	
Aux Output Current, Vaux- = -12.0V	0A	0.5A	1A	

† The Aux Voltage levels depend upon both the Supply Current and the Aux Current. See **Figures 3 through 5** for the relationship between the Aux Voltage regulation and the output loading (current).

Note: The maximum current levels listed are specified for ambient temperatures below 35°C (without a heat sink). Please refer to the power derating curves in **Figures 1** and **Figure 2** for operation at temperatures greater than 35°C for the -V1 and -V2 options.

Environmental	
Operating Temperature (-V1, -V2)	-25° to +85° Celsius
Operating Temperature (-V3)	-25° to +70° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

Note: Temperature specifications are for units with or without heat sinks. See curves below for the heat sink's effect on converter performance.

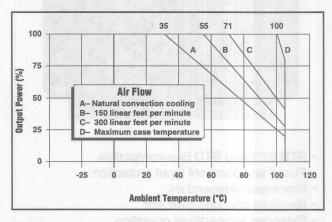


Figure 1. Power derating curve without heat sink, -V1 and -V2 options

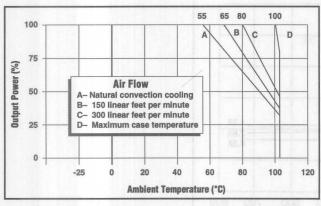


Figure 2. Power derating curve with top-mounted heat sink, -V1 and V2 options

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 mechanical specifications
- Measures 4.5" (11.3cm) by 6.5" (16.5cm)
- Component Height without heat sink = 0.50" (12.7mm)
- Component Height with heat sink = 0.80" (20.3mm)
- Weight = 5.6 oz. (158.8g)
- Connectors

P1: 114-pin STD 32 Bus

J1: Three-position screw terminals for

DC input

Reliability

MTBF: 15 years

• MTTR: five minutes (based on board replacement)

Ordering Information

ZT 88CT85-Vx(H) DC to DC Power Supply Board

Must choose one option from Input Voltage Range, heat sink cooling is optional:

(For example: ZT 88CT85-V1H)

Input Voltage Range Option:

V1 18 to 36VDC (24VDC nominal) V2 36 to 72VDC (48VDC nominal) V3 9 to 18VDC (12VDC nominal)

Heatsink Cooling Option:

H Heat sink installed on unit *
(Heat sink improves DC-to-DC converter efficiency at high temperatures; available only for -V1 and -V2 options).

* See **Figures 1 and 2** for derating and heat sink information. Requires two STD card slots with the heat sink installed.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.

All products are shipped FOB San Luis Obispo, CA USA. OEM discounts are available for most products.



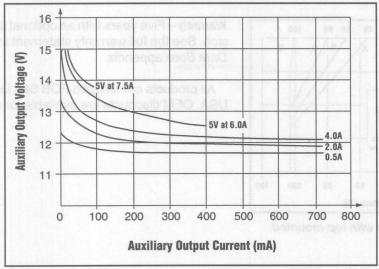


Figure 3. Auxiliary voltage output to auxiliary current output, -V1 and -V2 options

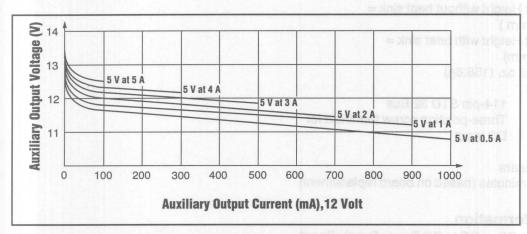


Figure 4. Auxiliary voltage output to auxiliary current output, -V3 option

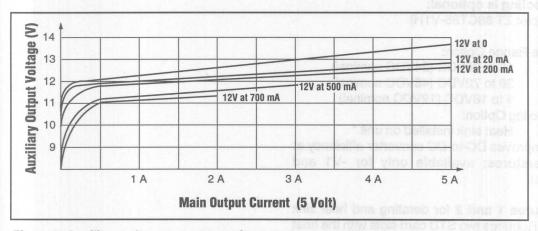


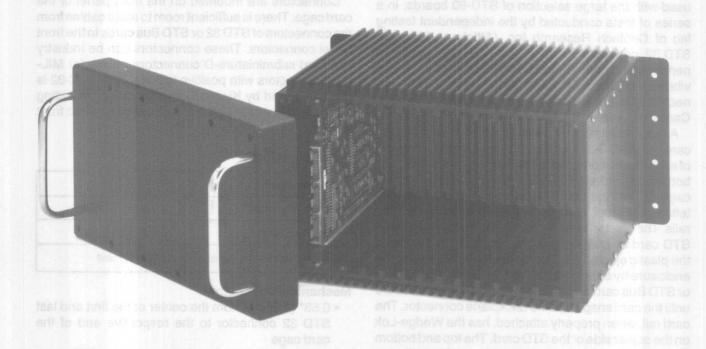
Figure 5. Auxiliary voltage output to main current output, -V3 option

NEMA-rated STD 32® card cages designed for severe environments including high shock and vibration

The RCC-32 allows STD 32® and STD Bus computers to be used in severe industrial, mobile vehicle and defense applications, where conventional card cages and computer systems would be destroyed. Having proved itself in rugged industrial environments, the STD 32 Bus is ideal for high shock and vibration and exposed environments such as those found on trains, buses, aircraft and outdoors. The Kinetic Computer Corp. RCC-32 Rugged Card Cage enclosures allow

users to package standard STD 32 and STD Bus boards for severe environments.

The RCC-32 is available in 4-, 6-, 9-, 12-, 15- and 24-slot widths. The integrated low-noise backplane accommodates 8-, 16- and 32-bit data transfers. STD 32 or STD Bus boards are individually mounted in the STD 32 card cage using a card module. This module consists of top and bottom card rails that clamp the board to the top and bottom of the enclosure.



- STD 32- and STD Bus-compatible, 0.625" (15.9mm) spacing
- 4-, 6-, 9-, 12-, 15-, and 24-slot configurations
- NEMA 4/12-rated
- · Conduction cooled
- MIL-STD-810, -975, -1540, 461
- SAE specification J1455

- 30G shock and 19G RMS sine and random vibration
- Optional integrated power supplies available
- Successfully used in space shuttle, heavy-duty trucks, jet aircraft, unmanned aerial vehicles, rocket launch sites and outdoor applications



KINETIC COMPUTER CORP.

TEL>617.547.2424 FAX>617.547.7266



14-57

Functional Considerations

The RCC-32 Rugged Card Cages from Kinetic Computer Corp. are available in 4-, 6-, 9-, 12-, 15- and 24-slots on 0.625-inch (15.9mm) centers. The RCC-32's construction uses high-tolerance machined aluminum hardware, providing NEMA 4 and 12 characteristics and the tight tolerances necessary for high shock and vibration operation. The RCC-32 is a two-piece design with a front cover securely attached to the card cage via 3/32" (2.4mm) hex screws. A gasket on the inside of the front cover provides the NEMA seal for the enclosure. The front cover is used for all I/O connections and has two large handles mounted on it. The RCC-32's aluminum finish is black anodized.

Backplane

The RCC-32 uses a low noise 5-layer STD 32 backplane providing 8-, 16- and 32-bit data transfers with Slot X capability for multiprocessing applications. In addition to compatibility with the growing selection of STD 32 processor and I/O cards, the RCC-32 can be used with the large selection of STD-80 boards. In a series of tests conducted by the independent testing lab of Contech Research Inc. (Attleboro, MA), the STD 32 connector used in the RCC-32 backplane performed comparably to DIN connectors in shock and vibration environments, and was superior to DIN connectors in some aspects.

Card Modules

A card module tightly fastens the STD 32 or STD Bus card in the RCC-32 enclosure. A card module consists of a top and bottom card rail that attaches to the top and bottom edge of the STD card as it is slid into the card cage. A Wedge-Lok™ system, in conjunction with teflon card slots, comprises the top and bottom card rails. The ejector handle must first be removed from the STD card by pushing the retaining pin out, removing the plastic ejector. STD cards are then mounted in the enclosure by attaching the card module to the STD 32 or STD Bus card and sliding the unit into the enclosure until the card snaps into the backplane connector. The card rail, when properly attached, has the Wedge-Lok on the solder side of the STD card. The top and bottom rail guides are not identical and are specific to the top and bottom of the STD card. A screw is tightened on each card rail with a 3/32" hex key to force the wedges apart, providing a shock and vibration-resistant friction mount inside the card cage. The Wedge-Loks also provide some thermal conductivity from the card to the card cage for increased heat dissipation.

Cooling

The RCC-32 is designed for conduction cooling without the use of fans. Optimum conduction cooling takes place when the enclosure is mounted vertically so the handles of the front cover point upward with respect to gravity. The integrated heatsink fins on two

sides of the enclosure conduct heat away from the enclosure.

Mounting

A rear mounting flange behind the backplane is standard, with four mounting holes on each side of the RCC-32. This enables the RCC-32 to be mounted vertically to any flat surface using eight #10 screws. Other mounting configurations are available as a custom order from Kinetic Computer Corp. Handles on the front cover allow the RCC-32 to be carried and moved conveniently.

I/O Connections

All I/O signals (serial and parallel data, analog data, etc.) as well as power signals are brought into the RCC-32 enclosure through the removable front cover. The front cover is secured to the card cage with hex screws. A 3/32" hex key is included with every RCC-32 card cage for securing the front cover. This hex key is also used for attaching the card module to the STD card.

Connectors are mounted on the front panel of the card cage. There is sufficient room to route cables from the connectors of STD 32 or STD Bus cards to the front panel connectors. These connectors can be industry standard subminiature-D connectors or circular MIL-type connectors with positive locking. The RCC-32 is fully supported by Kinetic Computer Corp., including design and manufacturing of application specific front covers.

Specifications

Environmental	
Operating Temperature	-40° to +85° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	NEMA 4/12-rated

Mechanical Dimensions

- 0.53" (1.35cm) from the center of the first and last STD 32 connector to the respective end of the card cage
- 1.75" (4.44cm) between the top of the STD computer boards and the inside of the front cover for running cables
- · Construction: Black anodized aluminum
- Weight: 6-slot: 3lbs.; 9-slot: 5lbs.; 12-slot: 5lbs.; 15-slot: 6lbs.; 24-slot: 7lbs.
- Operating Shock: 30G
- Operating Vibration

Maximum: 20 to 2000 Hz @ 0.075 g²/Hz Composite: approximately 19G-RMS

EMI: Per MIL-STD-461C

• Heat Dissipation: 100W @ 25° C. ambient

temperature results in a temperature rise of less than 13° C. inside enclosed card cage with no heatsinking or

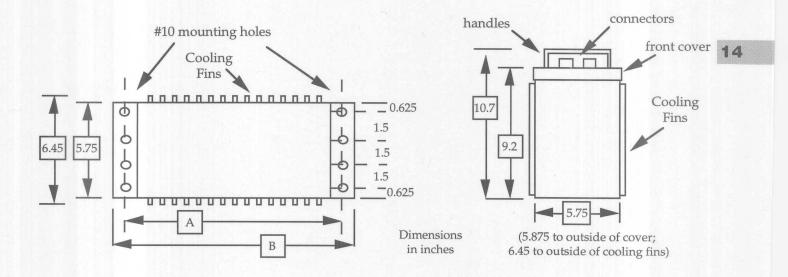
external fans

	4-Slot	6-Slot	9-Slot	12-Slot	15-Slot	24-Slot
A	4.175"	5.425"	7.300"	9.175"	11.050"	16.675"
В	5.175"	6.425"	8.300"	10.175"	12.050"	17.675"

Note: See diagram below for more mechanical dimensions

All products are shipped FOB Cambridge, MA, USA. OEM discounts are available. Contact Kinetic Computer Corp. for additional information at 270 Third Street, Cambridge, MA, 02142. Or, call (617) 547-2424. Units may also be shipped and integrated by Ziatech Corporation.

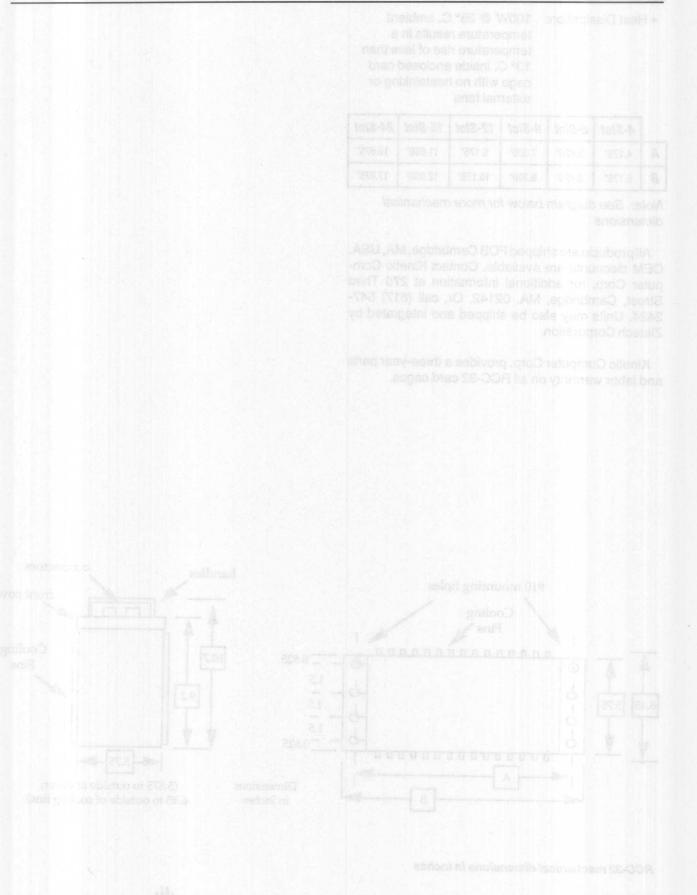
Kinetic Computer Corp. provides a three-year parts and labor warranty on all RCC-32 card cages.



RCC-32 mechanical dimensions in inches



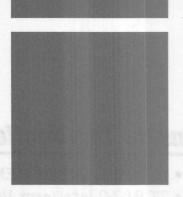




STD 32[®] Multiprocessing



15



Inside This Section

- STD 32 STAR SYSTEM™
- ZT 8830 Intelligent I/O Control Processor
- ZT 8832 Intelligent I/O Control Processor
- ZT 89CT39 Slot X Arbiter Card
- DOS Multiprocessing Extension (DOS MPX)
- Application Note #9: Expanding STD Bus Performance Through Multiprocessing
- An Application Guide to Multiprocessing



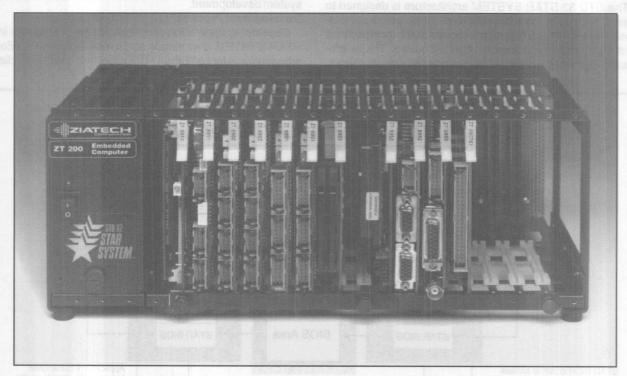
STD 32 STAR SYSTEM

Multiprocessing Computer System

The STD 32 STAR SYSTEM™ features multiple single board computers that share peripherals over a single backplane

The STD 32 STAR SYSTEM takes a simple, yet extremely powerful approach to the design of a real-time control computer. The STD 32 STAR SYSTEM concept includes multiple DOS CPUs in a single card cage. Each CPU has its own local memory and DOS operating system, but shares backplane memory, DOS disks, and video with other CPUs in the system. This is accomplished with Ziatech's STAR BIOS which manages the DOS resources in a way that is transparent to the user. The STAR SYSTEM features Ziatech's

modular line of processor boards from the 16-bit NEC V53 (286) to the powerful 32-bit Intel 486. Boards can be mixed in a system to provide combinations of high-powered user interface functions and fast, real-time control functions. All processors can run from on-board or shared solid state disks for operation in rugged environments. For applications combining multiprocessing and multitasking capabilities, STAR-QNX is available (see separate data sheet).



- Multiple processors running MS-DOS®
- Supports processors up to the 486 CPU
- Simplest method of partitioning a control application for real-time response
- Uses standard DOS programs and development tools on all processors
- STD 32 hardware arbitration provides reliability and performance
- · All I/O cards accessible from all CPUs
- Disk partitions are shared for read access

- · Write access to disk partitions is assignable
- Video and keyboard can be toggled among CPUs for easy debugging
- CPUs operate from local memory for maximum speed
- Common memory accessible to all CPUs for communication
- NetBIOS for interprocessor communications
- Microsoft® Windows™ 3.1 support
- Supports all STD I/O cards



Functional Considerations

Types of Multiprocessing

There are many different definitions and applications of the term multiprocessing. A common form of multiprocessing employs multiple processors sharing the same memory space. This method optimizes performance by having all the processors work on the same problem to arrive at a solution more quickly.

The STD 32 STAR SYSTEM uses Multiple Instruction Multiple Data multiprocessing, which employs a distributed memory architecture. That is, each processor has its own memory for instructions and data, and communicates with other processors via a messaging system. This distributed memory design is a scalable system that provides a proportional performance increase as processors are added.

In the STAR SYSTEM, the messaging system is built around an area of common memory on the backplane. Therefore, the STAR SYSTEM is similar to a very fast and transparent Local Area Network, except that all the processors are on the same STD 32 Bus.

Partitioning Control Applications

The STD 32 STAR SYSTEM architecture is designed to meet the needs of complex real-time control system applications. Real-time control systems require that critical portions of the process occur exactly when required. These processes can not be delayed by pauses for operator input,

network response, or other, less critical functions. In the past, designers resorted to complex programming and time consuming development of interrupt service routines. In some cases, a real-time multitasking executive or operating system was necessary, and the programming became even more complex and expensive.

Now, the STAR SYSTEM allows the designer to allocate one processor (or more) to meet the demands of each real-time process, while another processor looks after the less critical functions. Since each processor has its own memory, core devices, and its own copy of DOS, there is no interference from other processors. Processors communicate via clearly defined (but not restricted) common memory, while access to shared DOS peripherals is managed by the STAR BIOS and is transparent to the application program (see Figure 1). Since DOS disk devices are typically used for program and data loading, their effect on the real-time operation is easily controlled.

These features enable the STAR SYSTEM to provide a fast, predictable system with easily defined parts and straightforward software design. This is ideal for real-time control system development.

Development Process

Developing application programs for the processors in a STAR SYSTEM is as simple as developing on a PC. Each processor is in fact a "Virtual PC" except that it shares its disks

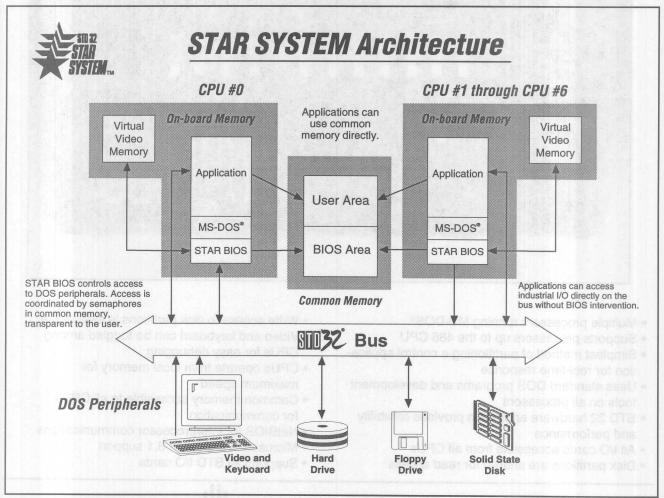
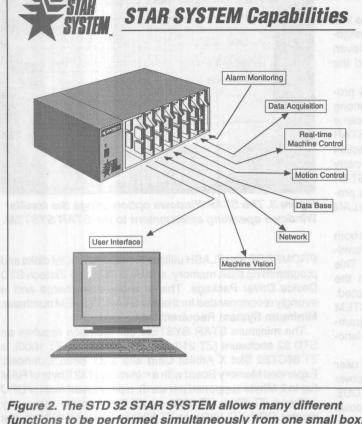


Figure 1. The STD 32 STAR SYSTEM allows multiple DOS processors to share peripherals over the same STD 32 backplane.



functions to be performed simultaneously from one small box.

with other "Virtual PCs." The video display and keyboard console can be "switched" from processor to processor by a CTRL-ALT-SPACE key combination. For cards with local bus video controllers, full graphics mode switching is

If there is a single video card in the backplane, this switching feature supports text mode applications only. This is ideal for development and debugging using popular textbased tools such as Turbo Debugger and QuickBASIC because the programs run simultaneously on different processors sharing the same video card. Virtual video memory on the processor cards emulates an actual video card. when the user switches control of the physical video card to a particular processor, the display is updated from that processor's "virtual" video card. The processor that loses control of the physical video card sends video output to its own virtual memory instead. The entire process is transparent to the application program and the user.

Bus arbitration in an STD 32 system is a hardware function controlled by an arbiter card located in "Slot X" (the left-most slot in a system). Signal pairs run from each of the first 15

STD 32 Multiprocessing Bus Arbitration

slots to Slot X. The MREQ* signal is used by a processor to request access to the backplane and is granted by the arbiter card using MACK*. The arbiter card supports seven slots and uses either fixed priority (left-most slot goes first), or rotating priority (each slot gets equal access) to determine which CPU gets access if more than one simultaneous request is received.

This design approach reduces the complexity of the CPU design (and therefore the cost) versus other schemes that put the arbitration logic on every CPU in the system. It also increases reliability since arbitration is controlled by one simple, very reliable circuit.

A memory card provides common memory accessible to all CPUs. This card also has extra capacity for use as shared solid state disks (RAM, ROM, or flash).

Systems using Ziatech's ZT 8911 Scalable Processor Board as the permanent master use an alternate configuration. The ZT 8911 has the bus arbitration and common memory built-in.

The STAR BIOS

The STAR SYSTEM's STAR BIOS is an extension of Ziatech's proven industrial BIOS and incorporates all of its unique features. These include the ability to define the boot source (PROM, floppy drive, fixed drive, or network), the ability to select a fast boot (no memory test), built-in support for PROM, RAM, and flash memory drives, the ability to boot without a keyboard attached, and support for the Virtual System Console facility.

The STAR BIOS also manages all backplane accesses to DOS disks and to the video console. All this is accomplished at the BIOS level (a 100% ATcompatible BIOS interface) while the multiprocessing features are transparently supported. Additional functions enable applications to communicate with other processors and determine the state of DOS peripheral devices.

CPU Options

STAR SYSTEM processors fall into two categories: permanent and temporary masters. The permanent master is the one that provides the backplane clock and is responsible for initializing all the DOS peripherals. There can be only one permanent master in a system, but up to six temporaries can exist with it.

The STAR SYSTEM supports the ZT 8911 Scalable Processor Board, the ZT 8902 Single Board 486 Computer, and the ZT 8901 Single Board V53 Computer as permanent masters. The ZT 8902 and ZT 8901 processors can be jumper configured to operate as either permanent or temporary masters. The ZT 8911 must be used as a permanent master. For complete information on these processor cards, please refer to their respective data sheets.

All processors in the STAR SYSTEM include Microsoft MS-DOS in flash memory. Non-DOS CPUs and other operating systems and kernels are not excluded from a STAR SYSTEM but are not supported directly by the STAR BIOS. Interprocessor Communication

The STAR SYSTEM provides many methods of sharing and exchanging data between processors in a system. Here is a brief summary:

1. The Shared Drive Subsystem-Fixed, floppy, and solid state disk are all shareable. However, only one processor is allowed write access to a given drive partition. Ownership is assigned at boot time. This allows one processor to write files to its own drive partition for other processors to read. Files should be closed before other processors read the data. This mechanism is the easiest to implement, and probably the slowest.



- Common Memory

 A minimum of 16 Kbytes (at CC00:0)
 of common memory is available for users and can be
 referenced by any program on any CPU in a STAR
 SYSTEM.
- STAR BIOS Functions—Extra STAR BIOS functions that
 provide messaging functions and semaphore management are available. Additional STAR BIOS functions even
 allow screen switching under program control and the
 ability to reboot another CPU in the system.
- 4. STAR NetBIOS Functions—The STAR NetBIOS provides a standardized method for communicating among processors in the STAR SYSTEM. Based on the same standard used by local operating networks (LANs), STAR NetBIOS allows programmers to use familiar function calls to pass messages between processors. Third-party software packages provide a bridge between the STAR NetBIOS and a LAN-based NetBIOS, allowing any processor in a STAR SYSTEM to communicate over the LAN to processors outside the STAR SYSTEM.

NetBIOS is included with every STAR SYSTEM as both an installable device driver (a .SYS file) and as a Terminate and Stay Resident (TSR) file (an .EXE file). This means it can be installed on each CPU when the CONFIG.SYS or AUTOEXEC.BAT file is executed. NetBIOS is not required for normal STAR SYSTEM operation and using NetBIOS does not prevent programmers from using common memory or STAR BIOS function calls directly.

 STAR DDE-For systems using a Windows-based user interface, the STAR DDE software with the STARWindows option lets control processors place data directly into DDE (Dynamic Data Exchange) variables on the Windows processor.

STARWindows

Microsoft Windows is the most popular platform for user interface software, but is problematic for real-time applications. The STAR SYSTEM overcomes this limitation by allowing real-time applications to be delegated to other processors that are not subject to the Windows scheduler. The STARWindows option adds Microsoft Windows to STD 32 STAR SYSTEMs. STARWindows combines the Windows software with elements that allow Windows-based applications to take full advantage of the STAR SYSTEM. STARWindows includes the STAR Console, STARDDE, and Windows 3.1 installed (see Figure 3).

The STARWindows DDE server supports the Dynamic Data Exchange mechanism of Windows that allows applications to exchange changing data. In a STAR SYSTEM, this data is shared by all the processors in the system.

The STAR Console allows an operator to open a window into any processor in the system. This means that a program running on a processor (i. e., Borland's Turbo Debugger, Microsoft QuickBASIC, etc.) can be viewed and changed through a STAR SYSTEM window. In fact, up to four processors can be viewed simultaneously by opening a STAR Console window for each processor.

The STARWindows option is available for any STAR SYSTEM equipped with a ZT 8911 or ZT 8902. The ZT 8901 does not support Windows, but it can still operate as a DOS processor in a STAR SYSTEM that has Windows operating on another CPU.

Development Software

An optional development package includes the Virtual System Console utility for remote system development, the

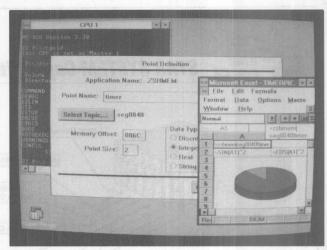


Figure 3. The STARWindows option brings the familiar Windows operating environment to the STAR SYSTEM.

PROMPREP and FLASH utilities for making PROM disks and programming flash memory, and STD DDP, the Ziatech STD Device Driver Package. This is a one-time charge and is strongly recommended for the first STAR SYSTEM purchase. **Minimum System Requirements**

The minimum STAR SYSTEM configuration requires an STD 32 enclosure (ZT 210, ZT 250, ZT 300, or ZT 1000), a ZT 89CT39 Slot X Arbiter Card and a ZT 8825 Extended/ Expanded Memory Board with a minimum of 32 Kbyte of RAM (up to 2 Mbyte supported per card), a permanent master CPU (either a ZT 8911, ZT 8902, or ZT 8901) and a temporary master CPU (ZT 8902 or ZT 8901). If the ZT 8911 is the permanent master, the arbiter card and common memory (ZT 89CT39 and ZT 8825) are not required.

Other peripherals can be added as required (see **Figure 4**). Options include ZT 8952 and ZT 8953 IDE hard drives, the ZT 8950 Integrated Disk Drive/DMA Controller (1.44 Mbyte), ZT 8921 PCMCIA 2.0 Interface Card, the ZT 8842 VGA/Flat Panel Display and Keyboard Interface, and the ZT 8982 Super VGA/FPD and Keyboard Interface. Additional ZT 8825 memory boards can be added for expanding ROM, RAM, and flash EPROM solid state drives.

Extended Temperature Option

The ZT 8901 and the core system components are all available in CT versions with a -40° to +85° C operating range for extra harsh environments. The ZT 8902 and ZT 8911 are available in LT versions for low temperature (-40° to +70° C) environments. Specify the ZT 88CT25, ZT 89CT01, ZT 89CT39, ZT 89LT02 or ZT 89LT11. Other CPUs are not available in CT or LT versions.

Specifications

General

- Maximum number of processors: 7
- Bus arbitration time: 125 ns
- Maximum bus inter-CPU transfer rate
 (highest CPU in fixed priority): 2 Mbytes/second
 Note: ZT 8911 can transfer 32 Mbytes/sec. to STD 32 peripherals.
- Common memory 32 Kbyte minimum (more if additional memory cards are installed)
- Worst case transfer rate (Any CPU [of n] in rotating priority mode): 2/n Mbytes/second



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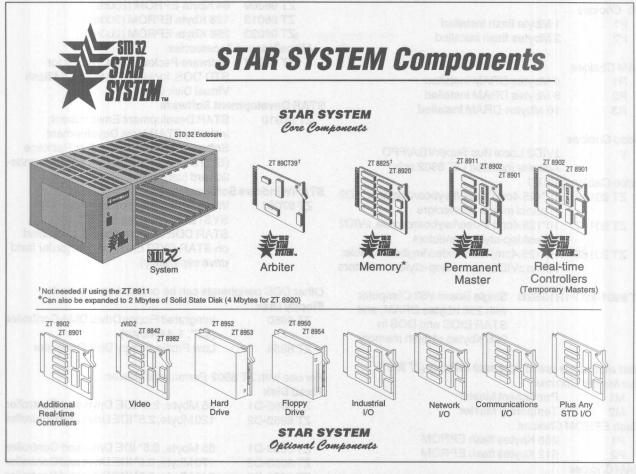


Figure 4. With the STD 32 STAR SYSTEM, a variety of peripherals can be added to the standard configuration.

Note: Transfer rate data assumes that all CPUs are continually requesting the bus. Bus bandwidth available to a lower priority CPU depends on the activity of the higher priority CPUs.

Ordering Information Permanent Master Only

ZT 8911-C1E0R1S2

Scalable Processor Board with 33 MHz 486DX CPU, no cache, 4 Mbytes DRAM, and STAR BIOS and DOS 5.0 in flash memory

Must choose one option from each category (ZT 8911): CPU Choices

C1	33 MHz 486DX installed
C2	66 MHz 486DX2 installed

No cacho

Flash Memory Choices

P1	1 Mbyte flash memory installed
P2	2 Mbytes flash memory installed

Cache Choices

	140 Cacile
E1	64 Kbytes cache memory installed
E2	128 Kbyte cache memory installed

RAM Choices

R1	4 Mbytes DRAM installed
R2	8 Mbytes DRAM installed
R3	16 Mbytes DRAM installed
R4	32 Mbytes DRAM installed

Permanent or Temporary Masters

ZT 8902-C1M1R1S2	Single Board 486 Computer
	with 25 MHz 486SX CPU,
	4 Mbytes DRAM, and STAR
	BIOS and DOS 5.0 in
	flash memory

Must choose one option from each category (ZT 8902): CPU Choices

"	0 01101000	
	C1	25 MHz 486SX installed
	C2	33 MHz 486DX installed
	C3	50 MHz 486DX2 installed
	C4	66 MHz 486DX2 installed
	C5	33 MHz 486SX installed

Bus Master Choices

M1	Permanent master
M2	Temporary master



Permanent or To	emporary	Masters (continued)	Memory Kit A	Accessories
Flash Choices	omporar,		ZT 96009	
P1	1 Mhyte	flash installed	ZT 96013	
P2		s flash installed	ZT 96033	
F2	Z Mibytes	S liasii liistalleu		us Accessories
DAMChainea			ZT 97047	
RAM Choices		- DDAM in stelled	2101011	STD DOS. Includes RAM/PROM/flash
R1		s DRAM installed		Virtual Disk Driver
R2		s DRAM installed	CTAP Develor	
R3	16 Mbyt	es DRAM installed		oment Software
			ZT 94010	STAR Development Environment;
Video Choices	3			includes STAR Host Development
V	zVID2 L	ocal Bus SuperVGA/FPD		Software, STD Device Driver Package
	Adapter	installed (ZT 8902 only)		(STD DDP), MS-DOS 5.0, BIOS diagnos-
Video Cables	(zVID2)			tic card (cables excluded)
ZT 90166		1cm) Video/keyboard cable, zVID2	STARWindow	s Software
2100100		mount connectors	ZT 97091	Windows support software for STAR
ZT 90167		4cm) Video/keyboard cable, zVID2		SYSTEMs. Includes STAR Console,
21 90107		op-style connectors		STAR DDE and Windows 3.1 installed
7T 00400				on STAR SYSTEM hard disk (order hard
ZT 90168		4cm) multi-video/keyboard cable;		drive separately)
	seven z	VID2s to desktop-style connectors		drive separately)
ZT 8901-M1P	1B13S2B	Single Board V53 Computer	Other DOS per	ripherals can be ordered as required:
2100011111	IIIIOOLD	with 256 Kbytes DRAM, and	Floppy Disk	direct that enter high in anything of polytoper but only wat?"
		STAR BIOS and DOS in	ZT 8950	Integrated Floppy Drive/DMA Controlle
		256 Kbytes of flash memory		(3.5", 1.44 Mbyte)
		256 Rbytes of flash filemory	ZT 8954	Low Profile Floppy Disk Controller
		(ZT 0004):	21 0004	Low Fromo Froppy Blok Controllor
		om each category (ZT 8901):	For use with 7	T 8902 Permanent Master:
Bus Master Ci			Fixed Disk	1 0302 Fermanent Master.
M1	ALC: U.S. The state of the little	ent Master		OF MILES OF FILIPE DESIGNATION
M2	Tempor	ary Master	ZT 8952-D1	85 Mbyte, 2.5" IDE Drive and Controlle
Flash EPRON	1 Choices		ZT 8952-D2	120 Mbyte, 2.5" IDE Drive and Controlle
P1	256 Kby	rtes flash EPROM		
P2		rtes flash EPROM	ZT 8953-D1	85 Mbyte, 3.5" IDE Drive and Controlle
RAM Choices			ZT 8953-D2	170 Mbyte, 3.5" IDE Drive and Controlle
R1		tes DRAM (120ns)	ZT 8953-D3	
R2		rtes DRAM (55ns)	ZT 8953-D4	530 Mbyte, 3.5" IDE Drive and Controlle
			Solid State Di	
R3		static RAM (120ns)		PCMCIA 2.0 Interface Card for STD
R4		static RAM (55ns)		Bus Computers
		R4 cannot be battery backed		ous computers
Miscellaneous		SEC servolat SE	Display	ICA/Flat Danal Dianlay and
M	80287 N	lumeric Coprocessor, 20 MHz		VGA/Flat Panel Display and
				Keyboard Interface
Arbitration and	Memory	(Not necessary with the ZT 8911)		SuperVGA/Flat Panel and Keyboard Interface
ZT 89CT39	Slot X A	rbiter Card		e Data Book cable section for more details)
ZT 8825	Expand	ed Byte-Wide Memory system	Cables for Z	T 8911 and ZT 8902
ZT 8920		lemory System	ZT 9007	24VAC wall transformer
		wo banks of separately configured	ZT 90072	2 10' digital I/O (50-pin connectors both ends
		y a configuration for each bank.		3' printer (20-pin header to 25-pin D-shell)
			ZT 90135	
		imum configuration: ZT 8825	ZT 90136	
AM1BM0B.			Cables for Z	
		CPU Choices 1 - 121 - 121		
		or memory banks A and B (Contact		4 40" serial (14-pin header to 25-pin D-shell
Ziatech for othe		ations):	ZT 90027	
Memory Option			ZT 90069	
MO	No Mem	nory as AM 88	ZT 90071	
M1		rtes static RAM (100ns)	ZT 90100	Frontplane interrupt cable (16-pin to 10-pin
M2		rtes static RAM (100ns)		
M3		static RAM (120ns)	Serial ports,	ARCNET, Ethernet, and LonWorks interfaces
M4		rtes flash memory (200ns)		llers, and other devices are available from
M5		rtes flash memory (200ns)		dard product line for expanding the STAF
		tes hash memory (2001s)	SYSTEM.	The state of the s
Battery Option		avelithium batter autorial atte		tered trademark, and STD 32 STAR SYSTEM™ is a
В	1 amp-h	our lithium battery, extended temp.		ch Corporation. Other product names may be trademarks



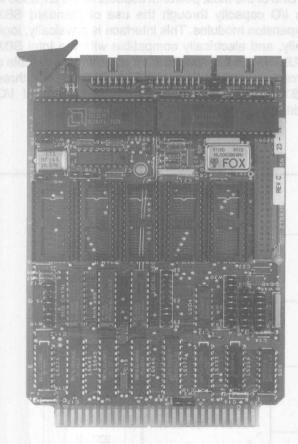
of their respective companies.

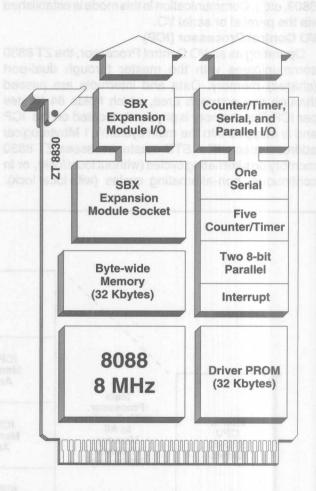
A single board 8088 computer that operates as an Intelligent I/O Control Processor

The ZT 8830 is designed for data acquisition, communication, and robotics applications where real-time performance and high-speed programmable I/O are requirements. This 8088-based STD Bus computer can function as an intelligent I/O Control Processor (ICP) or as a single board computer, depending on the user's application.

As an ICP, the ZT 8830 "teams up" with the STD processor to form a multiprocessing STD Bus system.

The ZT 8830 can be used as a single board computer in situations that require low-cost, compact computer power. Operation in the single board (non-STD Bus) mode requires only the addition of electrical power.





- 8 MHz 8088 processor
- Eight-level, vectored interrupt controller
- On-board and external interrupt capability
- One 28-pin EPROM socket (32K capacity)
- Four 28-pin RAM sockets (32K capacity)
- Two 8-bit parallel I/O ports
- Eight control registers

- Serial port with option for RS-232 or RS-485
- Optional DOS Multiprocessing Extension (DOS MPX) software
- Five 8-bit counter/timers
- SBX Expansion Module socket
- Burned-in at 55° C and tested to guarantee reliability



Functional Considerations

Central Processor

The ZT 8830 has an 8.192 MHz 8088 central processor. The CPU accesses local on-board memory and I/O, but cannot access off-board memory, or I/O, or interact with an 8087 Math Coprocessor. Interrupts can be sent to the STD Bus backplane.

Single Board Computer Mode

The ZT 8830 can operate as a stand-alone single board computer with on-board memory and I/O.

Free Mode

The ZT 8830 can operate as a loosely coupled parallel processor in an STD Bus system. The STD Bus master can be any STD processor (8085, 8088, Z80, 6809, etc.). Communication in this mode is established via the parallel or serial I/O.

I/O Control Processor (ICP)

Operating as an I/O Control Processor, the ZT 8830 communicates with the master through dual-port (shared) memory. Data and interrupts are passed through this common area, which holds 64 Kbytes per ICP. The memory is physically located on the ICP and is mapped into the main system's 1 Mbyte logical address space. The STD master accesses ZT 8830 memory on alternating cycles (without local lock), or in continuous, non-alternating cycles (with local lock).

Memory System

The ZT 8830 supports 32 Kbyte of EPROM and four 8 Kbyte static RAMs for a total of 32 Kbytes of RAM. **Serial I/O**

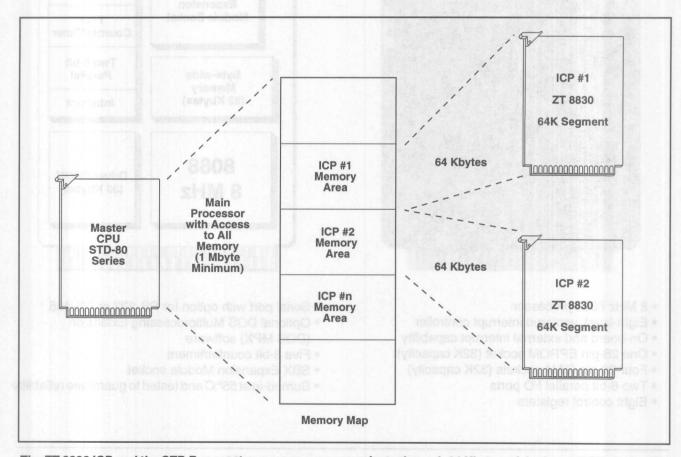
The ZT 8830 has one asynchronous serial I/O port with an on-board programmable baud rate generator. Serial line drivers can be added with optional Ziatech off-board interface adapters for RS-232 or RS-485 compatibility.

Parallel I/O

Two 8-bit, parallel I/O ports are provided. Port 1 is bidirectional and bit-programmable. Port 2 is bidirectional and nibble (4 bits) programmable. Both ports are combined for bidirectional, asynchronous, and parallel communication with handshake.

SBX Expansion Interface

One of the most powerful aspects of the ZT 8830 is its I/O capacity through the use of standard SBX expansion modules. This interface is physically, logically, and electrically compatible with the Intel SBX MULTIMODULE specification and makes available a broad array of I/O functions. The ZT 8830 uses three SBX address modes for up to 64 bytes of I/O address capability.



The ZT 8830 ICP and the STD Bus master processor communicate through 64 Kbytes of dual-port RAM on the ICP.

Counter/Timers

The ZT 8830 features five 8-bit programmable counter/timers and a programmable pre-scaler to give the ZT 8830 the capability to accurately measure time and count off-board events. Four counter/timers can be programmably cascaded into two 16-bit timers; one of the 8-bit counter/timers can be reset to its initial value by an external signal.

Interrupt Controller

The interrupt controller vectors eight priority levels. Vectored interrupts can be generated from external TTL signals, serial or parallel I/O activity, counter/timer activity, SBX module interrupts, or STD master/ICP interaction.

Software Development Considerations

Ziatech's DOS Multiprocessing Extension (DOS MPXTM) is a development and an operating environment that provides high-level support for designers developing STD DOS (MS-DOS on STD Bus) applications with the ZT 8830.

DOS MPX is comprised of a boot ROM for the ICP, an installable device driver for the system's master processor, and a utility for downloading programs to ICPs. The Virtual Processor Console (VPC) program provides a flexible user interface to the ICPs.

Software development for the ZT 8830 ICP is simplified by the use of DOS MPX, which allows programmers to develop applications with a high-level language such as "C." Any or all of the components of DOS MPX can also be used in the run-time environment. (See the DOS MPX data sheet for more details.) STD ROM

The ZT 8830 I/O Control Processor is also supported by STD ROM. The STD ROM development environment is designed for users who want to develop ROM-based applications using high-level languages like "C," but don't want the cost and overhead of an operating system in their final application.

The STD ROM package includes Paradigm DEBUG/RTTM, Ziatech PDREMOTE/ROM EPROM and Paradigm LOCATE, and startup libraries. This allows the developer to write programs in Microsoft or Turbo C®, debug these programs at the source level on the actual hardware, and make a final target EPROM of the application (see the STD ROM data sheet).

Specifications

Electrical

Compatible with STD-80 Series Bus, up to 8 MHz.

Power Output	Min.	Тур.	Max.
Supply Voltage, V _{CC}	4.75V	5.00V	5.25V
Supply Current, V _{CC} = 5.0V		0.85A	1.7A
Aux Voltage, V _{aux+}	11.4V	12.0V	12.6V
Aux Current, V _{aux+} = 12.0V		0.15A	0.25A
Aux Voltage, V _{aux} -	-12.6V	-12.0V	-11.4V
Aux Current, Vaux- = -12.0V	-	0.15A	0.25A

Note: Vaux+ and Vaux- are needed only if the RS 232 interface adapter is installed.

Data Rates

Serial I/O:

 1.024 Mbaud maximum with external baud clock, 29.3 Kbaud maximum with on-board baud rate generator

Parallel I/O:

- 228 Kbytes/second maximum STD master block transfer
- 380 Kbytes/second maximum STD master block transfer
- 380 Kbytes/second maximum at 5 MHz, 600 Kbytes/second maximum at 8 MHz, in lock configuration

Mechanical

- Size- and pin-compatible with the STD Bus and SBX MULTIMODULE specifications
- Measures 4.5" x 6.5" (11.4cm x 16.5cm)
- Occupies two 0.625" (1.6cm) spacing card slots with SBX module installed
- Connectors

P1:	56-pin card edge-connector on 0.125"
	(3.2mm) spacing for the STD Bus
J1:	16-pin parallel channel 2
J2:	16-pin parallel channel 1
J3:	16-pin serial channel
J4:	36-pin SBX expansion module

Environmental		
Operating Temperature	0° to 65° Celsius	
Storage Temperature	-40° to +85° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

Reliability

- MTBF: 59 years
- MTTR: five minutes (based on board replacement)

ZIATECH

Ordering Information

The minimum configuration of the ZT 8830 does not include RAM, PROM, or software and is ordered as: ZT 8830-P0R0S0.

ZT 8830

I/O Control Processor

ZT M8830

I/O Control Processor manual

Must choose one option from each category:

PROM Options

PO No EPROM

P1 32 Kbyte EPROM, 170ns

RAM Options

RO No RAM

R1 32 Kbytes RAM

Software Options

SO No software installed on board

S1 DOS MPX boot software

(Requires Options P1R1 or greater)

Accessories

Cables (see Data Book cable section for details):

ZT 90011 RS-232 adapter board with 40" (1m)

cable and 25-pin female D-shell

ZT 90012 RS-422 adapter board with 40" (1m)

cable and 25-pin female D-shell

ZT 90021 10' (3m), 50-pin to 50-pin card edge

ZT 90072 10' (3m), 50-pin both ends

ZT 90137 2' (0.6m), 50-pin both ends

Boards (see separate data sheets for details):

ZT 2224 24-Line Termination Assembly ZT 2225 Industrial I/O Cable Adapter

ZT 2226 24-Channel I/O Mounting Rack

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

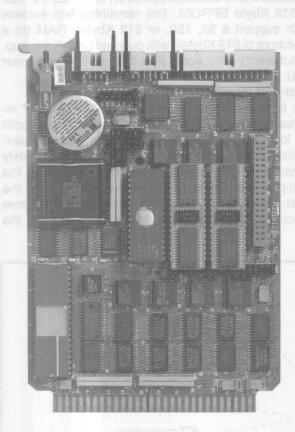
Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.

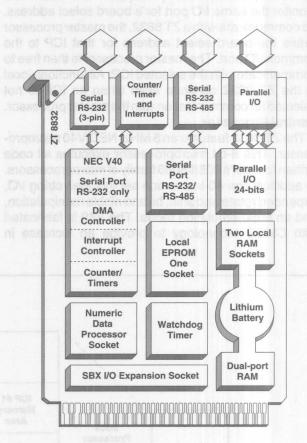
A single board V40 computer with a large I/O complement for intellegent I/O functions

The ZT 8832 I/O Control Processor (ICP) is an 8 MHz, V40-based single board computer designed to operate by itself or as an intelligent control processor in an STD Bus system. It increases system throughput by managing time-critical operations and includes a large complement of on-board I/O and expansion capability. Use of the ZT 8832 simplifies complex systems because it allows them to be partitioned into a series of tasks assigned to one or more ICPs.

The ZT 8832 and the STD master processor communicate through 32 Kbytes of dual-port RAM and I/O-mapped control and status registers located on the ZT 8832. The ZT 8832 does not directly access other STD I/O or memory cards, and therefore does not restrict STD backplane throughput.

The ZT 8832 is supported by Ziatech's DOS Multiprocessing Extention (DOS MPX), which integrates multiprocessing into the DOS environment.





- 8 MHz, V40 microprocessor
- 512K ROM/512K RAM capacity
- 32 Kbyte dual-port RAM (populated)
- Optional battery backup on all RAM
- Two serial ports (V40, 82050) RS-232/485
- Three 8-bit parallel ports, Opto 22 compatibility
- SBX expansion interface with DMA support
- Three 16-bit counter/timers (V40)

- Interrupt controller (V40)
- Push-button reset
- Two-stage watchdog timer
- 8087 Numeric Data Processor socket
- 20-/24-bit STD memory decoding
- Optional DOS Multiprocessing Extension (DOS MPX)
- Optional PROM-based debugger



Functional Considerations I/O Control Processor (ICP)

The ZT 8832 can operate as a stand-alone single board computer or as an I/O control processor (ICP), communicating with a master processor through 32 Kbytes of dual-port memory. The memory is physically located on the ICP and is mapped into the main system's address space.

Board Select Option

One ZT 8832 ICP occupies 32 Kbytes of STD addressing space. For applications using multiple ICPs, each ICP can be mapped into a unique 32 Kbyte space or, by using the board select option, up to seven can be mapped into a common 32 Kbyte space. This option is enabled by mapping each ZT 8832 to the same memory address range and to a unique board select address. In operation, all commonly mapped ZT 8832 ICPs monitor the same I/O port for a board select address. To communicate with a ZT 8832, the master processor writes the board select address for that ICP to the common I/O port. The master processor is then free to communicate with the selected ICP. All functions local to the ZT 8832 continue even when an ICP is not selected for communication with the master processor. **Central Processor**

The ZT 8832 features an 8 MHz, NEC V40 microprocessor. This 8-bit microprocessor executes all code written for Intel's 8088/8086 family of microprocessors. In addition, the 40-instruction set includes string I/O, expanded rotate and shift, bit and nibble manipulation, and an 8080 emulation mode. The V40 is fabricated with CMOS technology to provide an increase in

operating temperature range and noise immunity, with a reduction in power consumption.

Extended Math Performance

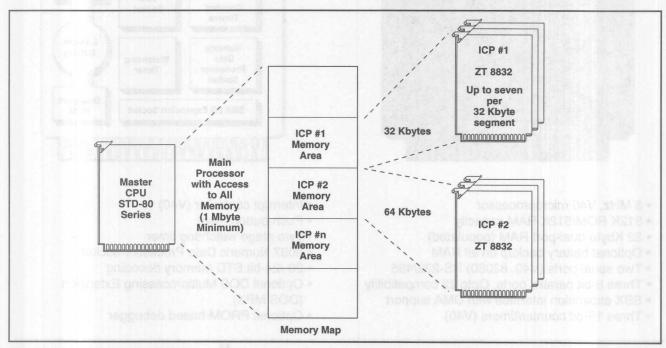
The Intel 8087 Numeric Data Processor (NDP) can be added to the ZT 8832 ICP for applications that require additional math capability. Plugging the NDP into the socket on the ZT 8832 provides 68 added instructions for extended arithmetic, trigonometric, exponential, and logarithmic functions. These added instructions are supported by seven additional data types, including integers (16-, 32-, and 64-bit), floating-point (32-, 64-, and 80-bit), and BCD (18-digit). Using the NDP increases performance up to 100 times that of equivalent routines implemented in software.

Local Memory

The ZT 8832 ICP is populated with three 32-pin memory sockets dedicated for use by the V40 microprocessor. One socket supports an 8, 16, 32, 64, 128, or 512 Kbyte EPROM. The remaining two sockets each support a 32, 128, or 512 Kbytes RAM (to a maximum of 512 Kbyte), with optional battery backup. This memory is not accessible by the STD Bus master CPU.

Dual-port Memory

In its standard configuration, the ZT 8832 ICP includes 32 Kbytes of RAM that are accessible from both the local ICP processor and the master processor. Arbitration for simultaneous access is done completely in hardware. To increase system performance, the dual-port memory is physically separated from the local memory. This permits the ICP to continue executing local operations at full speed while the



The ZT 8832 ICP and the STD Bus master processor communicate through 32 Kbytes of dual-port RAM on the ICP.

15

master processor is accessing the shared memory. The master processor can also continue operations while the ICP processor accesses dual-port memory. Only when both processors attempt a dual-port memory access is the operation of one suspended until the other is completed. Repetitive accesses from both processors are interleaved on a machine cycle basis. The dual-port memory also supports software-programmable interrupts, a locking mechanism, and battery backup. The locking mechanism allows either the master processor or the local ICP processor to keep the other from accessing the dual-port memory until the lock is removed.

Serial I/O

The ZT 8832 includes two asynchronous serial communication channels, each with a programmable baud rate generator. The NEC V40 provides one serial channel (a subset of the 8251A) configured as RS-232 DTE. This serial channel supports the transmit data (TXD) and receive data (RXD) signals only, and is available through a 3-pin frontplane connector. An optional one-meter cable (ZT 90069) joins the 3-pin connector to a male 25-pin, D-shell connector.

The second serial channel (Intel 82050 or equivalent) is functionally equivalent to the serial controller used in the IBM PC. This channel supports all handshaking and modem control signals and can be jumper-programmed for RS-232 or RS-422A/485. Other features include loopback diagnostics, maskable interrupt generation, and jumper-selectable DCE or DTE configuration. The 82050 serial channel is accessed through a 14-pin frontplane connector. Optional one-meter cables (ZT 90014 and ZT 90027) connect the 14-pin connector to a male or female 25-pin, D-shell connector, respectively.

Parallel I/O

There are three, 8-bit parallel ports on the ZT 8832, for a total of 24 I/O lines. Each I/O line can be programmed as input, or output with readback. The I/O signals and fused power are accessible through a 26-pin, frontplane connector. An optional one-meter cable (ZT 90068) connects the 26-pin connector directly to an 8-, 16-, or 24-position I/O module mounting rack, such as those manufactured by Ziatech and Opto 22.

Interrupt Controller

The ZT 8832 includes one programmable interrupt controller (8259A architecture) with eight inputs. Features of the interrupt controller include level- and edge-triggered sensing, fixed and rotating priorities, and the ability to mask individual inputs. Two of the interrupt request inputs are available through a frontplane connector to be used as needed by the application. The remaining inputs are dedicated to interrupt sources to support interrupt-driven data transfers from the master processor through

dual-port memory. These interrupt sources include serial controllers (for interrupt-driven data transfers), SBX modules (for interrupt-driven I/O), and the STD Bus.

Counter/Timers

The ZT 8832 has three independent 16-bit counter/timers (8254 architecture) that can be used as timers or event counters. There are six programmable counter/timer modes: interrupt on end-of-count, frequency divider, square wave generator, software-triggered, hardware-triggered, and retriggerable one-shot. One of the counter/timers is available for application use through a frontplane connector. The other two counter/timers are dedicated for uses such as baud rate generation for the NEC V40 serial channel, and interrupt generation for timed and periodic interrupts.

Watchdog Timer

The ZT 8832 includes a selectable, two-stage watch-dog timer. If the application fails to strobe the watchdog timer, the ZT 8832 sends a non-maskable interrupt to the V40. The non-maskable interrupt service routine must take corrective action that includes strobing the watchdog timer within a certain time period or the ZT 8832 is reset. The watchdog timer is enabled through jumper selection.

DMA Controller

Direct Memory Access (DMA) provides high-speed data transfer between ZT 8832 memory and SBX expansion module I/O. The DMA controller performs the memory and I/O operation in a single machine cycle for a data transfer rate of up to 2 Mbytes per second. The following transfers are supported: SBX I/O to and from the local memory sockets, and SBX I/O to and from the dual-port RAM.

SBX Expansion Interface

An on-board SBX expansion socket allows users to customize the I/O capabilities of the ZT 8832 to the needs of the application. The SBX interface is electrically, mechanically, and functionally equivalent to the Intel SBX MULTIMODULE standard, including DMA support for high-speed data transfers. This makes it compatible with hundreds of off-the-shelf I/O modules.

Battery Backup

An optional battery can be installed to support the RAM during system downtime. The battery will support the 32 Kbyte dual-port RAM and can be configured to support all the RAM.

Software DOS MPX

Ziatech's DOS Multiprocessing Extension (DOS MPX) is a development and an operating environment that provides high-level support for designers developing STD DOS (MS-DOS on STD Bus) applications with the ZT 8832.



DOS MPX includes a boot ROM for the ICP, an installable device driver for the system's master processor, and a utility for downloading programs to ICPs. The Virtual Processor Console (VPC) program provides a flexible user interface for the ICPs. (See the DOS MPX data sheet for more details.)

The ZT 8832 I/O Control Processor is also supported by Ziatech's STD ROM Development package. STD ROM is designed for users who want to develop a ROM-based application using high-level languages like C, but don't want the cost and overhead of an operating system in their final application (see STD ROM data sheet).

Specifications

Electrical

STD ROM

- Size- and backplane-compatible with the STD 32 and STD-80 specifications
- RAM data retention for optional battery backup:
 5 yrs. typical, 2 yrs. minimum for dual-port RAM

Power Output	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00A	5.25A
Supply Voltage, Vcc = 5.0V		1.0A	1.8A
Aux Voltage, Vaux+	11.4V	12.0V	12.6V
Aux Current, Vaux+ = 12.0V	MC ent.	4mA	8mA
Aux Voltage, V _{aux} -	-12.6V	-12.0V	-11.4V
Aux Current, Vaux- = -12.0V	tranefers	4mA	8mA

Mechanical

- Size- and backplane-compatible with the STD 32 and STD-80 mechanical specifications
- SBX MULTIMODULE-compatible
- Measures 4.5" (11.4cm) by 6.5" (16.5cm)
- Height measured from component surface:
 Without battery = 0.38" (9.7mm)
 With battery = 0.43" (10.9mm)
- Weight = 4 oz. (113.4g)
- Connectors

P1: 56-pin card edge-connector on 0.125" (3.2mm) spacing for the STD Bus

J1: 26-pin parallel channel

J2: 14-pin serial channel

J3: 10-pin interrupt and counter/timer

J4: 36-pin SBX expansion module

J5: 3-pin serial channel

Environmental	
Operating Temperature	0° to 65° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

Reliability

• MTBF: 20 years

• MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8832 I/O Control Processor

ZT M8832 I/O Control Processor manual

Must choose one option from each category: PROM Options:

P0 No PROM installed P1 128 Kbytes PROM P2 512 Kbytes PROM

RAM Options:

RO No RAM

R1 128 Kbytes static RAM, 120ns

(extended temperature)

R2 512 Kbytes static RAM, 120ns

(extended temperature)

Software Options:

S0 No software

S1 DOS MPX Boot Software

(Requires Options P1R1 or greater)

Choose Miscellaneous options as needed:

Miscellaneous Options:

B 1 amp-hour lithium battery (extended temperature)

M 10 MHz 8087 Numeric Coprocessor

and 8087-2 math coprocessor (extended temperature)

Accessories

Cables (see Data Book cable section for details):

ZT 90014
ZT 90021
40" (1m), 14-pin to 25-pin female
10' (3m), 50-pin on both ends
2T 90027
40" (1m), 14-pin to 25-pin male
2T 90068
40" (1m), 26-pin to 50-pin header
and 50-pin edge
ZT 90069
ZT 90090
40" (1m), 3-pin to 25-pin female
40" (1m), 26-pin on both ends

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.



STO32°

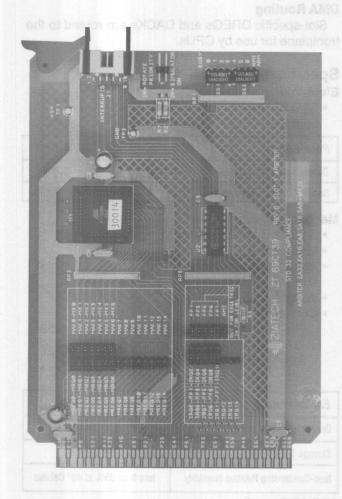
Slot X Arbiter Card for the STD 32® Bus

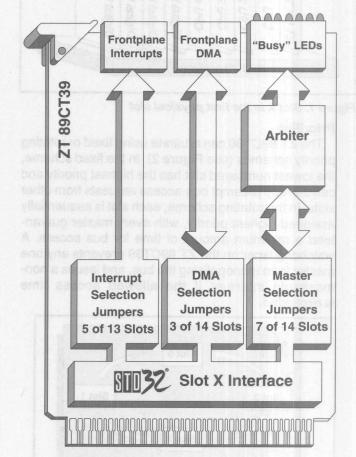
Arbiter card provides STD 32 Bus-master arbitration for multiple processors in STD 32 systems

The ZT 89CT39 provides STD 32 Bus-master arbitration to facilitate up to seven processors in an STD 32 system. The low part count of the ZT 89CT39 ensures extremely reliable operation.

Both fixed and rotating priority arbitration schemes are available to provide flexibility for individual system

requirements. In the fixed priority scheme, access requests from CPUs in lower numbered slots have precedence over those from CPUs in higher numbered slots. Conversely, the rotating priority scheme provides equal access to the bus for each CPU, regardless of slot number.





- STD 32 Slot X-compatible
- Supports up to seven STD 32 Bus-masters
- Rotating or fixed priority arbitration
- · LEDs to identify active bus-master
- · Watchdog timer prevents bus monopolization
- Slot-specific interrupts routed to frontplane connector

- · Low part count ensures high reliability
- All CMOS logic
- Extended temperature operation (-40° to +85° C)
- · 8 MHz bus arbitration rate
- Slot-specific DMA requests and acknowledges routed to frontplane connector

Note: CT denotes CMOS, TTL backplane-compatible and extended temperature operation of - 40° to + 85° C. (Users should make adjustments for temperature rise in enclosures.)



Functional Considerations STD 32 Bus Arbitration

Utilizing the EISA technique for bus arbitration, STD 32 uses a pair of slot-specific lines which request and grant access to the bus. These lines run from the first 15 general-purpose slots in an STD 32 backplane, to Slot X, the first physical slot (see **Figure 1**). Any busmaster that needs the bus asserts the master request line from its own slot. The ZT 89CT39 then arbitrates among other requests and asserts master acknowledge on the slot-specific line when the bus is available. Arbitration is initiated every 125ns.

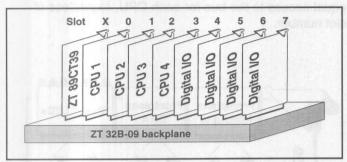


Figure 1. Slot X is the first physical slot

Priorities

The ZT 89CT39 can arbitrate using fixed or rotating priority schemes (see **Figure 2**). In the fixed scheme, the lowest numbered slot has the highest priority and can thereby preempt bus-access requests from other slots. In the rotating scheme, each slot is sequentially assigned highest priority, with every master guaranteed a minimum amount of time for bus access. A watchdog timer on the ZT 89CT39 prevents any one master from monopolizing the bus, and issues a non-maskable interrupt if the allowed access time is exceeded.

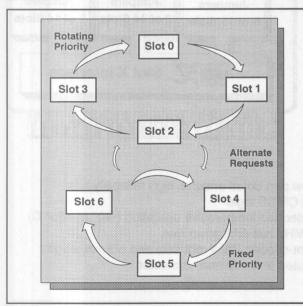


Figure 2. Rotating priority scheme

LED Indication

An LED indicator bar on the front of the ZT 89CT39 identifies the slot that last accessed the bus. This is useful for monitoring bus activity, as well as for trouble-shooting and diagnostics.

Low Part Count

The ZT 89CT39 uses few components and has an extremely high MTBF (Mean Time Between Failure). Since arbitration is handled from an individual board, rather than several complex CPU arbiters, the reliability of the entire system is enhanced.

Interrupt Routing

Slot-specific interrupts are collected at the ZT 89CT39 and routed to the frontplane to be returned to individual processors.

DMA Routing

Slot-specific DREQs and DACKs are routed to the frontplane for use by CPUs.

Specifications

Electrical

 STD 32 Bus-compatible for 8 MHz operation (Slot X only)

Power Req.	Min.	Тур.	Max.	
Supply Voltage, Vcc	4.75V	5.00V	5.25V	
Supply Current, Vcc=5.0V	_	110mA	150mA	

Mechanical

- STD 32 Bus-compatible
- Measures 4.5" (11.4cm) by 6.5" (16.5cm)
- Height measured from component surface: 0.34" (0.9cm)
- Weight = 3.5 oz. (99.2g)
- Connectors
 - P1: 114-pin card edge connector on 0.0625" (0.2cm) spacing for the STD Bus
 - J1: 10-pin latching interrupts
 - J2: 10-pin latching slot-specific DMA

Environmental		
Operating Temperature	-40° to +85° Celsius	
Storage Temperature	-40° to +85° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

STD 32 Compliance

 Arbiter D (7): SA16, SA8-MX, IXL, IXP
 Note: SA8 is equivalent to STD-80 Series Rev. 2.3 (5 and 8 MHz)

Reliability

- MTBF: 55 years
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 89CT39 Slot X Arbiter Card



System Designer's Guide

EXPANDING STD BUS PERFORMANCE THROUGH MULTIPROCESSING

January, 1994

The star Campol Campol

First edition printed July, 1989

ZIATECH

I. Introduction to Multiprocessing

In the increasingly complex world of control, computers are called upon to perform many more difficult functions. Not only are they now required to control tasks faster and more reliably, the development time of these applications is being drastically shortened. "Time to market" is now paramount, along with the associated costs of software development.

This application note discusses how innovative multiprocessing solutions from Ziatech can be used to solve many of these problems. These multiprocessing approaches provide a modular approach to system design that integrates hardware and software to ensure responsiveness, yet simplifies software development.

II. Multiprocessing

Multiprocessing refers to the use of more than one processing unit to perform a set of operations. In the world of control systems, this usually means more than one microprocessor. However, given this definition there are many different ways microprocessors can be connected together and coordinated to perform their function. For example, in some applications many processors are mounted on the same board, all sharing the same memory and peripherals. In these cases each processor does some of the work of a very large program that usually involves massive data manipulation. This is typically called array processing and is often used for very complex mathematical or graphical projects.

In other types of multiprocessing, the different processors may be specialized and dedicated to a specific function (e.g. communications) as part of the larger system.

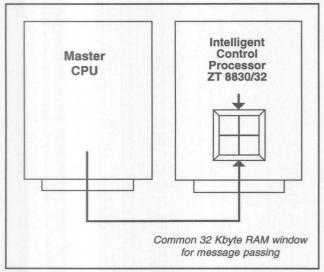


Figure 1: Ziatech's multiprocessing communications mechanism using the intelligent control method.

The approach that is best suited for control system applications is a multiprocessing architecture called Multiple-instruction, multiple data (MIMD) 1 with distributed memory. In this design, multiple processors perform instructions independently of their own data. This data is generally in each processor's memory so there is no contention between processors for the majority of their processing time. Each processor communicates with the others through a well defined area of common memory and includes a hardware arbiter to prevent contention. The processors spend the majority of their time executing and accessing local memory and only a small amount of time in common memory. This approach minimizes delays caused by other processors and has little effect on the timing of control functions.

Ziatech's Multiprocessing Approaches

Within the MIMD architecture, Ziatech supports two types of multiprocessor boards, both of which are STD Bus based, and one of which requires the extended features provided by STD 32.

STD 32 STAR SYSTEM

The STD 32 approach provides the core of Ziatech's STD 32 STAR SYSTEM. Processors in this system all have their own local RAM and ROM as well as extensive I/O. They boot MS-DOS from their own ROM and execute independently of the other processors. They can, however, share the DOS disks and video card and, if they wish, access I/O and memory on the STD 32 backplane. When this happens, the arbitration is managed by a bus arbiter in Slot X of the STD 32 backplane. In this case an external memory board is viewed as "common" memory by all the processors on the bus.

Intelligent Control Processors

The other Ziatech multiprocessing approach uses multiple Intelligent Control Processors (ICPs) with dualport memory on board as well as "local" memory. These ICPs cannot, however, access the backplane and must rely on their own "on-board" I/O to interface to the controlled process. The dual-port memory window allows communication between the STD Bus "Master" Processor and the ICP(s) (see Figure 1). In an STD system, there can be only one bus master, but in an STD 32 system any of the masters can access the bus side of this dual-port memory. In fact, from the bus side it would appear as common memory.

In the ICP approach, each CPU is usually configured as a dedicated controller for specific functions. This is described in more detail in the brief appendix at the end of this application note.

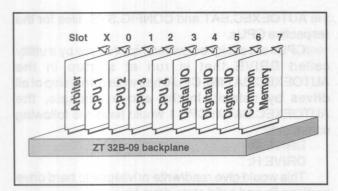


Figure 2. STD 32 Multiple Bus-Master System

III. The STD 32 STAR SYSTEM STAR SYSTEM Hardware

The STAR SYSTEM is built around the STD 32 Bus which supports the Multiple Bus-Master form of multiprocessing through extensions to the STD Bus. STD 32 uses new connectors that accept the older STD cards, but define many more backplane signals. While some of these lines are used for extra data lines and auto-sense features, others are reserved for bus arbitration that allows multiple CPUs to share the same backplane. STD 32 overcomes many of the limitations of older STD-based systems, including limited throughput, complex and expensive arbitration schemes, and multiprocessing schemes that redefined standard STD signals at the expense of DMA and interrupts.

In STD 32 systems, there are two signals, called Master Request (MRQX*) and Master Acknowledge (MAKX*). They lead from each connector on the backplane to the left-most connector (called Slot X) in the backplane (see Figure 2). Each CPU in the system typically has most of its own memory on board and accesses the backplane only during reads or writes to an I/O card or common memory. When this is necessary, the CPU card asserts Master Request (MRQX*), thereby signalling the central arbiter card in Slot X. The arbiter card decides whether or not to grant the CPU access based on the current state of the bus. When the bus is available, the arbiter card asserts Master Acknowledge (MAKX*) and allows the CPU card backplane access. This process typically takes less than 125 nanoseconds.

If, however, another CPU is already accessing the backplane, a potential conflict can occur. This conflict is resolved by the arbiter card. First, the current bus cycle must be completed, and then the arbiter card decides which CPU has priority, based on two user-selectable priority schemes: Fixed or Rotating.

In the Fixed Priority Scheme, the card closest to Slot X (Slot 0) has the highest priority. The slots to the right have progressively lower priority down to slot 15. Hence, it is possible to configure a system where one CPU always gets the bus when it wants it. The maxi-

mum wait would be to the end of the current bus cycle. The Rotating Priority Scheme assures that each CPU receives equal access to the bus. Thus, if all CPUs request bus access at the same time, each obtains it for a single bus transfer every cycle (see Figure 3).

The user can select either a fixed or rotating priority scheme for a system via a jumper on the arbiter card. Interprocessor communication is usually handled through an external memory card. Because the bus is open to any CPU, a memory board installed in the backplane is addressable by any CPU card. This memory board becomes "common" memory and can be any size. It is utilized to share data and software semaphores.

A common interrupt is provided so that each CPU can alert any or all of the others that it has a message or requires attention.

STAR SYSTEM processors fall into two categories: permanent and temporary masters. The permanent master provides the backplane clock and is responsible for initializing all the DOS peripherals. There can only be one permanent master in a system, but up to six temporary masters can exist with it.

The STAR SYSTEM supports the ZT 8911 Scalable Processor Board, the ZT 8902 Single Board 486 Computer, and the ZT 8901 Single Board V53 Computer as permanent masters. The ZT 8902 and ZT 8901 processors can be jumper-configured to operate as either permanent or temporary masters. The ZT 8911 must be used as a permanent master. For complete information on these processor cards, please refer to their respective data sheets.

In STAR SYSTEM configurations that do not include the ZT 8911, bus arbitration is managed by the ZT 89CT39 Slot X Arbiter Card, while the ZT 8825 Extended/Expanded Memory System provides common memory. A minimum of 32 Kbytes of battery-backed static RAM is required for the STAR SYSTEM common memory area. In STAR SYSTEM configurations that include the ZT 8911, the bus arbitration and 32 Kbytes of common memory are provided by the processor board.

The STAR BIOS and Software Support

Software issues arise when multiple CPU cards share the same I/O card in a system. If this I/O card has various states (such as channel select for a multiplexed A to D, or head positioning for a disk controller) the potential exists for conflicting instructions from different processors. Most of these issues are resolved by careful system configuration, but can also be handled via software semaphores in common memory.

A similar issue arises when DOS is used on different CPUs. A desktop DOS BIOS from any of the major BIOS suppliers will try to "own" all the peripheral



devices it finds on power-up, which is unacceptable in multiple processor applications. The STAR SYSTEM addresses this problem with a special STAR BIOS. This BIOS software is specially written to exist in a multiprocessing environment but at the same time provides a 100% AT-compatible BIOS interface to application software. In a STAR SYSTEM, one processor is designated as the "permanent" master by a jumper selection on board. This processor is responsible for driving the backplane clock and initializing the DOS peripherals (e.g. the hard and floppy disk drives and the video card). The other processors, the "temporaries," do not attempt to access the peripherals during this period.

The STAR BIOS does much more than this. All devices on the backplane are accessible from all processors, making it possible to share DOS peripherals but requiring some software management. The STAR BIOS provides this management, eliminating the need for specially-written application software. In a STAR SYSTEM, all disk drives (and logical partitions) are readable by each CPU, while only one CPU can have write ownership of any drive partition. This prevents corruption of data files. *Figure 4* illustrates a system with three CPUs, a floppy drive, a 50 Megabyte hard drive and a 1.0 Megabyte solid state disk. This table shows a possible arrangement of drives among CPUs.

In Ziatech's DOS system, each CPU has its own local solid state drives. Depending on the CPU, these drives may be EPROM and battery-backed RAM or flash memory. Each CPU has a read-only drive containing the operating system and drivers and a Read/Write drive for applications data and startup files. The local operating system is usually booted from the read-only drive, although it can be booted from the hard drive or floppy if required. Either solid state drive can contain

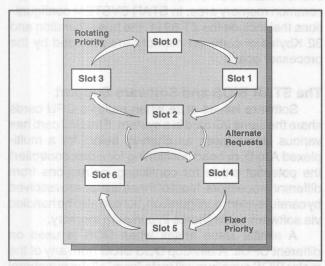


Figure 3. Rotating and Fixed Priority Scheme

the AUTOEXEC.BAT and CONFIG.SYS. files for the respective CPUs.

CPUs are assigned ownership of drives by a utility called DRIVE that is run at startup in the AUTOEXEC.BAT file. CPU 0 has write ownership of all drives by default. In the above example, the AUTOEXEC.BAT in CPU 1 would have the following commands:

DRIVE D:

DRIVE H:

This would give read/write privileges to hard drive partition D: and solid state drive H:.

Management of the video card is another issue that arises in this type of system. Most control applications only require one user interface, with other processors dedicated to real-time control. One of the main reasons for multiprocessing is to separate the user interface from the real-time control tasks, so that, in a final system, the video card is usually managed by only one processor. But what about development? Control programs are usually complex and need a lot of work to debug successfully. A developer wants access to all the productivity tools that make this difficult and time consuming task easier. The STAR BIOS provides the answer to this problem with a "hot key" video switch. Pressing the CTRL-ALT-SPACE combination on the keyboard "switches" the video and keyboard to the next processor number. The video screens on the other processors are kept in local memory and the local programs are not aware that they are no longer writing to the "real" video. This is like having a monitor for each processor, but only viewing one at a time. This system supports text modes only, but this is enough to run programs such as Borland's Turbo Debugger or Microsoft's QuickBASIC on multiple processors and switch the video between them.

The STAR BIOS also provides interprocessor communication services to application software discussed in the next section.

Interprocess Communication and Common Memory

Within a STAR SYSTEM there are five main methods of passing data between processors. They are not exclusive and can all be used together. They are:

Passing Data Through Common Files

The simplest method of exchanging data between processors is through common files on the shared disks. While there is quite a bit of overhead involved, this can still be fast, particularly if the file is on a common RAM disk. This method is appropriate if one CPU is collecting large amounts of data for later processing or display by another CPU. It requires some polling or another method that tells the other CPU when

Physical Drives	Logical Drives	CPU 0	CPU 1	CPU 2
Floppy 0 (1.44 MB)	A: (1.44 MB)	Read/Write	Read Only	Read Only
Fixed Disk 0 (50 MB)	C: (20 MB) D: (10 MB) E: (20 MB)	Read/Write Read Only Read Only	Read Only Read/Write Read Only	Read Only Read Only Read/Write
ZT 8825 Memory with 1 MB	F: (512 KB) G: (256 KB) H: (256 KB)	Read Only Read/Write	Read/Write Read Only Read Only	Read Only Read/Write Read Only

Figure 4. Possible arrangement of CPU drives

the data can be collected to avoid letting both CPUs have the same file open at the same time. The typical sequence would be something like this:

- 1. CPU 1 opens file and begins data logging.
- 2. CPU 1 has collected enough data so closes file.
- 3. CPU 1 signals CPU 0 that data is available.
- 4. CPU 0 Collects data and processes it.

This approach is easily implemented from a high-level language.

Passing Data Through Common Memory

The STAR SYSTEM has a minimum of 32 Kbytes of common memory mapped in the upper memory area at segment C800. The first 16 Kbytes are reserved by the STAR BIOS for its own use while the next 16 Kbytes (CC00:0 to CFFF:F) are available for the user. This memory can be directly accessed from most high-level languages. For example, it can be accessed with far pointer declarations in "C" or with PEEK and POKE in BASIC. This means that is can be used for quickly passing small amounts of information.

Two processors may try to read the same memory location at the same time. This is likely if that location is a semaphore (a flag used by software to show that a resource is in use). The STD 32 bus arbiter prevents both CPUs from colliding, but it is possible for data to be corrupted if precautions are not taken. Typically, the processors attempt to read the word/semaphore, make a decision, change the word, and write it back out. If CPU 1 writes the word after CPU 0 reads it but before CPU 0 writes the update, then that write will be lost.

Fortunately, the STD 32 STAR SYSTEM provides two solutions to this problem. The STAR SYSTEM implements the LOCK signal from the CPU, which allows software to lock a memory location during a memory exchange. System designers can create their own program libraries to protect critical memory during read/write cycles, or they can use the STAR BIOS multiprocessing extensions.

For more details of how this mechanism works, see the STAR SYSTEM manual or contact Ziatech for programming examples.

STAR BIOS Function Calls

The STAR BIOS defines additional function calls to support the multiprocessing environment. BIOS calls are easily implemented in "C" and libraries are available with some of the more common implementations. These routines use the common backplane interrupt for a fast response and allow for passing pointers to data structures, or file names between processors. There are many other STAR BIOS functions that are described in detail in the STAR SYSTEM manual. They can be briefly summarized into a few categories:

- Message Passing POST and PEND Functions
- Screen Management screen switching, enabling, and disabling
- Message delivery and reception
 - Rebooting other CPUs
 - Drive management

STAR NetBIOS functions

The STAR NetBIOS is an optional software extension to STAR SYSTEMs that implements all the standard functions found in NetBIOS. NetBIOS is a standard that was defined to implement communication between different processors on a network. This standard is ideal for the STAR SYSTEM, which can be thought of as a tightly coupled network of processors. NetBIOS provides a large set of functions that let a programmer set up communication "sessions" between processors using a clearly defined method. While not as fast as STAR BIOS calls, NetBIOS is more portable. In fact, it lets applications written for NetBIOS on a network run directly on a STAR SYSTEM. This includes many of the control software packages that support distributed processing and allows separate applications to run in the same card cage.

STAR DDE

Systems using a Windows user interface can utilize the optional STAR DDE program to exchange data between DOS-based applications on the real-time control processors and Windows programs.

STAR DDE takes data out of common memory and places it in the Windows environment as Dynamic Data Exchange (DDE) variables.

Software Development

Software development for a STAR SYSTEM is similar to software development for any DOS-based system, with an important exception. In a STAR SYSTEM, the components of the system should be defined carefully and analyzed "up front" to determine which components can be designed as separate modules and run on separate CPUs. The best approach first examines the interconnection between the parts of the software system. System parts that contain the fewest



interconnections are then grouped together. Ideally, these groups should be handled by separate processors so no one processor depends too closely on the other processor for continued operation. This also makes it easier to develop the software for each function independently of the others.

This approach is similar to a multitasking system design, except that with the STAR SYSTEM, the designer need not worry about system overhead which occurs when a CPU's bandwidth is used up.

Once the application has been broken down into individual modules, the software can be written on a PC or directly on the STAR SYSTEM itself, using the software development tools of choice. Development on the target STAR SYSTEM is efficient because the program can be edited, compiled, and debugged directly on the hardware it will be used with, and with the final I/O. In fact, with a STAR SYSTEM, it is possible to compile and link one program while debugging another, without performance degradation.

Once individual programs have been developed and debugged, it is necessary to test the integrated system. Here, the ability to switch the video screen between CPUs comes in very handy. It can be used to switch between debuggers on each CPU to watch the interaction of programs in a running system. If an application on a CPU stops, the screen can be switched to see how far it got. This can be a very time consuming task in many systems, but is very fast on a STAR SYSTEM.

Once the whole system is debugged, each CPU is set up (either in EPROM, flash, battery-backed RAM or on hard disk) with its own AUTOEXEC.BAT to load the individual programs. The system is then ready to go.

Support Under Windows

Microsoft® Windows® is the most popular platform for user interface software, but is problematic for realtime applications. The STAR SYSTEM overcomes this limitation by allowing real-time applications to be delegated to other processors that are not subject to the Windows scheduler. The STARWindows option adds Microsoft Windows to the STD 32 STAR SYSTEM. STARWindows combines Windows software with elements that allow Windows-based applications to take full advantage of the STAR SYSTEM. STARWindows includes the STAR Console, STARDDE, and Windows 3.1 installed. The STARWindows DDE server supports the Dynamic Data Exchange mechanism of Windows that enables applications to exchange changing data. In a STAR SYSTEM, this data can be shared by all the processors in the system.

The STAR Console allows an operator to open a window into any processor in the system. This means

that a program running on a processor (e.g. Borland's Turbo Debugger, Microsoft QuickBASIC, etc.) can be viewed and changed through a STAR SYSTEM window. In fact, up to four processors can be viewed simultaneously by opening a STAR Console window for each processor.

The STARWindows option is available for any STAR SYSTEM equipped with a ZT 8911 or ZT 8902. processor board. The ZT 8901 single board computer does not support Windows, but it can still operate as a DOS processor in a STAR SYSTEM that has Windows operating on another CPU.

Real-Time Issues

A common misconception is that DOS-based systems cannot be real-time control systems. DOS itself must deal with non real-time devices such as disk drives that may have unpredictable response times (depending on head location, etc.), but this need not limit the DOS-based control application. Unless the control program actually calls a DOS service (such as a disk access), DOS will never gain control of the processor, and the programmer can always have a guaranteed response. In addition, the processor's interrupt system can be used to provide rapid response to any event.

In this case, the only issue to worry about is whether DOS has interrupts disabled for any appreciable length of time. Ziatech has carefully designed its BIOS to minimize these interrupt latencies and has measured those latencies caused by DOS. The maximum latency period was found to be less than 200 microseconds for an 8 MHz V20 processor, and considerably less for faster processors.

The only background activity that takes place in a DOS system is the timer tick that occurs every 55 ms. Although there are no appreciable interrupt latencies associated with the timer tick, it can be disabled by the user in systems that do not require time of day or floppy disk support. In fact, some programmers may wish to disable the timer tick for time-critical code, and reenable it for floppy disk access.

IV. System Implementations

Designing A System's Functional Partitions

In any multiprocessing application, partitioning an application requires careful consideration. Deciding which functions are to be performed by each processor can be made easier by mapping out the application in terms of functional blocks. This involves the separation of specific functional blocks into software modules which can later be transferred to a separate processor if necessary.

Choosing Tasks for the Master

Typically, the Permanent Master processor performs the user interface functions (if any) and system coordination. This usually includes functions such as user interface (keyboard input and video output), disk storage and management, network management, message passing and sending new commands to other processors. After delegating this set of tasks to the master processor, it is up to the application designer to determine what additional load can be carried by the master. This may not occur until well into the project when designs and programs have stabilized.

Real-Time CPU Assignments

A good system design assigns the majority of the critical tasks to the temporary masters in the STAR SYSTEM. These temporary masters can have a good set of on-board peripherals, limiting their need to access the system bus. The CPUs can be configured for individual functional blocks such as an interface to an Opto 22 rack, a high-speed dedicated serial interface, or an analog/digital converter with a numerical data processor for data formatting or broader tasks (e.g. management of a conveyor system.).

The use of multiprocessing and structured soft-ware design practices mean that additional processing power can be added at virtually any stage of the development cycle. With this knowledge, the developer can partition his application with few worries about whether or not the processor will have enough power for the job. If the software is structured by functional tasks, it should be an easy job to delegate the tasks to another processor should the demands on the system grow.

Choosing a Software Development Environment

The STAR SYSTEM does not use a proprietary development environment. STAR SYSTEM processors are general purpose DOS platforms that can run virtually any compiler output and even standard software packages. STAR SYSTEM processors also support specific packages such as ladder logic interpreters and other control languages written for industrial needs.

V. Conclusion

Multiprocessing can greatly improve system performance by reducing the processing load on a single processor system, and distributing it over several dedicated processors.

The STAR SYSTEM provides a breakthrough in the ease and power of multiprocessing, greatly simplifying the task of designing a complex control system.

Appendix

The Intelligent I/O Control Processor (ICP) Approach

In addition to Ziatech's STD 32 STAR SYSTEM, another complementary multiprocessing approach involves intelligent I/O Contol Processors usually dedicated to handling specific I/O functions via I/O devices on the ICP itself.

ICP Hardware

There are two general purpose Ziatech ICPs, the ZT 8830 and the ZT 8832. The ZT 8830 has an 8 MHz 8088 microprocessor and supports 32 Kbytes RAM and 32 Kbytes ROM. For I/O, it has 16 TTL I/O lines, a serial port and an SBX expansion module socket. The ZT 8832 has an 8 MHz V40 and up to 512 Kbytes RAM and 512 Kbytes ROM as well as 32 Kbytes of dual-port RAM. For I/O it has 24 lines of Opto 22-compatible I/O, two serial ports and an SBX expansion module socket.

Two other specialized intelligent control processors are the ZT 89CT30, a Digital Signal Processor based on the Motorola 56001 DSP board, and the ZT 8932, a powerful intelligent, multi-channel serial controller.

The ZT 89CT30 DSP is ideal for processing analog information up to audio frequencies in real-time. It requires some knowledge of DSP techniques to program.

The ZT 8932, on the other hand, is available with an on-board program executive. The card supports up to eight serial channels.

ICP System Software and Development

Both the ZT 8830 and 8832 ICPs are supported with Ziatech's DOS Multiprocessing Extension (DOS MPX) and STD ROM software support packages. DOS MPX runs compiled DOS programs on the ICP and even supports a limited number of DOS calls. A "virtual processor console" utility lets users on the host interact directly with the target process during development. STD ROM is used for developing applications that will run directly out of ROM.

¹Multiprocessor Surf's Up, Bob Ryan. Byte June 1991

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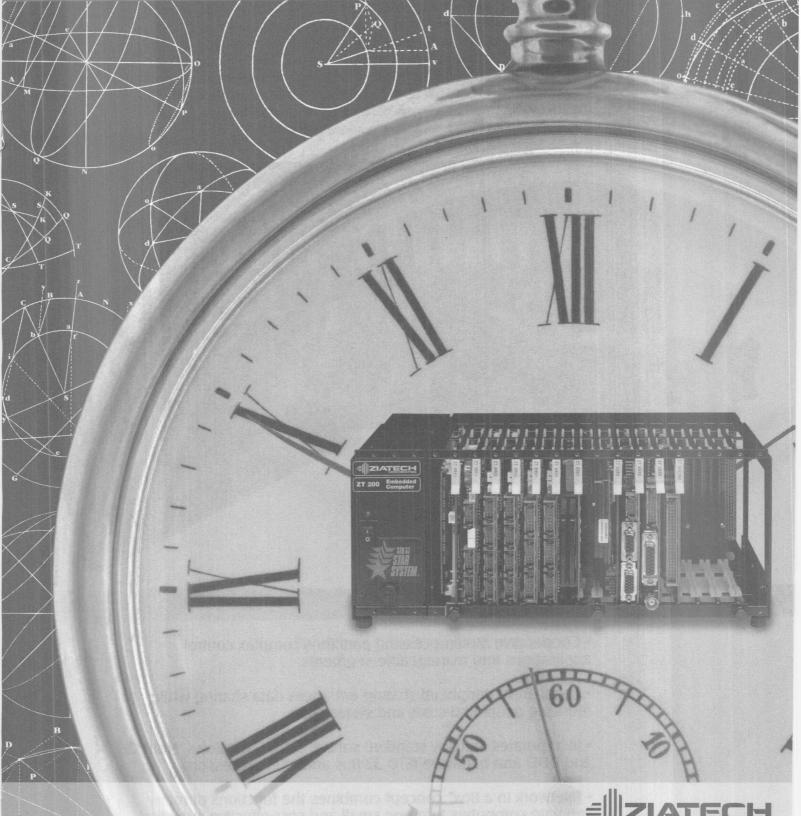
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ICP System Software and Development

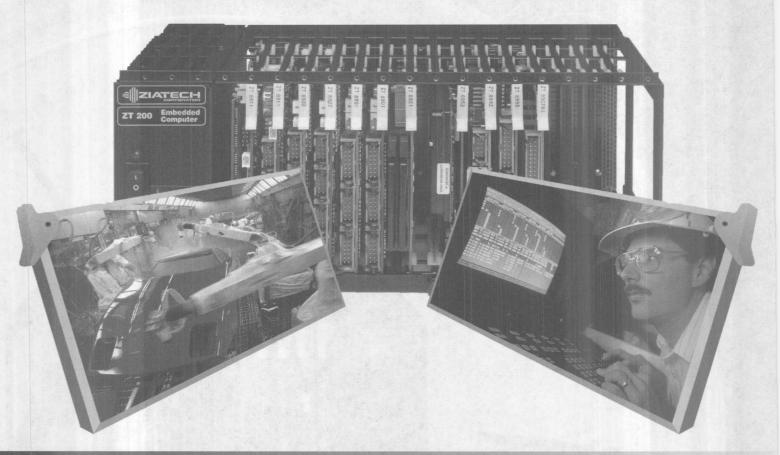
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APPLICATION GUIDE TO MULTIPROCESSING



Itatech, a major force in the design and manufacture of embedded systems, is rapidly gaining recognition as *the* multiprocessing control system company. As the inventor of STD 32®, a 32-bit extension to the STD Bus, Ziatech has used EISA technology to provide sophisticated multiprocessing capability. Many systems implement multiple computers to interconnect non-compatible but related environments, such as the graphical user interface and the real-time world. Recognizing this, Ziatech created a "network in a box" solution — the STD 32 STAR SYSTEM™. This multiprocessing engine allows for the orderly integration of dissimilar tasks while still providing for the sharing of peripherals and data. The Ziatech STD 32 STAR SYSTEM concept has been successfully adopted by many companies for their products and/or in-house systems.



STAR SYSTEM Technology

- Cooperative Multiprocessing partitions complex control applications into manageable segments
- Transparent peripheral sharing enhances data sharing while reducing peripheral costs and system size
- Incorporates industry standard software (DOS/Windows, NetBIOS and DDE) and hardware (STD 32 Bus and Intel processors)
- "Network in a Box" concept combines the functions of many separate computers into one small and cost-effective industrial computer

Real-World Applications of Real-Time Multiprocessing

What kinds of applications need multiprocessing?

While single processor systems provide adequate solutions to many of today's control challenges, a multiprocessing system can increase performance, hasten response time, and simplify software development.

Applications for multiprocessing encompass all kinds of industries and equipment types, but share some basic characteristics and requirements.

These control systems typically need to perform several different functions simultaneously, and these functions must be able to be separated with only minimal linkage. Often, these functions must be performed

immediately, or in other words, in real-time.

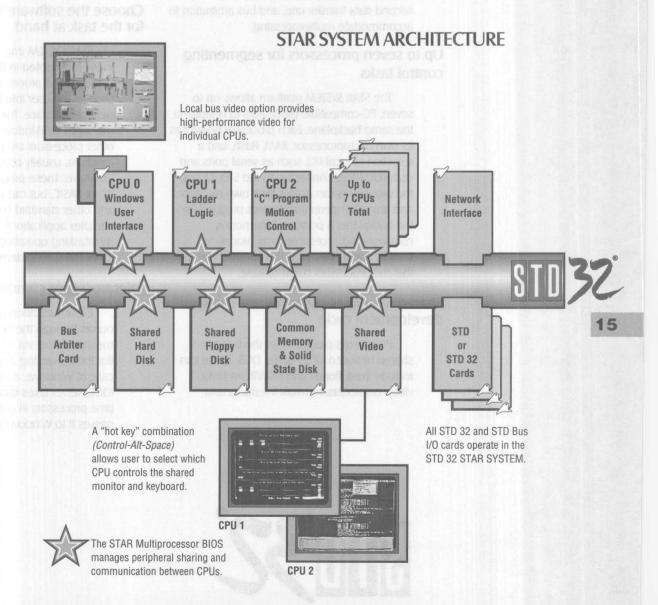
A system that combines a Windows®-based graphical user interface with motion control and on-going temperature measurements is a good candidate for a multiprocessing solution.

Multiprocessing also makes sense for existing applications where programs are already distributed over several computers, such as in a local area network. A multiprocessing system can dramatically increase system throughput and reduce cost by collapsing several PCs or industrial computers into a single multiprocessing computer.

n today's highly ompetitive global narketplace, control vstems are ncreasingly expected o perform more unctions faster, and system designers are expected to create hese systems more quickly for less cost. This guide uses application examples o show how the cooperative nultiprocessing echnique used in Ziatech's STD 32 STAR SYSTEM increases system performance and response, while

simplifying control

system development.



Real-World Applications of Real-Time Multiprocessing

Cooperative Multiprocessing: the STD 32 STAR SYSTEM Solution

The STD 32 STAR SYSTEM uses a cooperative multiprocessing technique to meet the real-time demands of control system applications. It combines an industrial computer architecture with the PC software environment so that system integrators can quickly implement a modular computer designed to withstand the rigors of harsh environments.

Architecture keys multiprocessing performance

The STAR SYSTEM is based on the STD 32 Bus, an open architecture, industrial bus with a 32-bit data path, a 32 Mbytes-persecond data transfer rate, and bus arbitration to accommodate multiprocessing.

Up to seven processors for segmenting control tasks

The STAR SYSTEM platform allows up to seven, PC-compatible processors to operate in the same backplane. Each processor board has its own microprocessor, RAW, Flash, and a selection of local I/O, such as serial ports and optional video. Connected to the STD 32 Bus, the processors can access their own memory and any other peripheral boards plugged into the backplane. A portion of memory is common and accessible to all processor boards, and it is through this common memory that the processors communicate.

Shared resources cut hardware costs, development cycle

Peripherals plugged into the bus are shared between CPUs under DOS. These can include fixed, floppy and RAW/ROM disks, video controllers, network interfaces and industrial I/O cards. The ability of STAR SYSTEM processors to share resources can eliminate the expensive peripheral and packaging redundancies found on networks and other multiprocessing solutions.

DOS-compatible tools and programs

Ziatech's unique STAR BIOS enables the STAR SYSTEM to support concurrently operating DOS-based processors, and manages access to the shared resources to prevent contention. This allows each processor to run standard DOS or Windows programs and development tools, making this a very accessible, easy-to-use multiprocessing platform.

Choose the software tools for the task at hand

STAR SYSTEM implementations, such as those highlighted in this brochure, typically dedicate one processor to non-real-time tasks, such as the user interface, data logging and network interface. These are increasingly managed by Windows-based programs. The other processors are assigned real-time functions, usually controlled by DOS-based programs. These programs are often written in "C" or BASIC, but can also include ladder logic and other standard software packages. More complex applications can use the power of a multitasking operating system such as QNX (QNX Software Systems Ltd., Kanata, Ontario).

Interprocessor communication

Communication between the processors occurs through the simple common memory mechanism, or via a NetBIOS implementation (for those wanting a standard protocol). In the case of Windows, a Dynamic Data Exchange (DDE) server takes data supplied by the real-time processors in common memory and passes it to Windows application programs.



Combining a Graphical User Interface and Real-Time Control

A chemical processing equipment manufacturer needed a computer with a graphical user interface (GUI) built directly into its equipment so that operators could easily monitor and adjust the state of a process. The company chose a Windows-based program for the user interface, and then discovered that a single PC could not simultaneously run the user interface program and provide adequate real-time control.

The manufacturer considered connecting a Programmable Logic Controller (PLC) to an embedded computer via a serial link to operate the digital and analog functions. This approach proved to be too slow, too difficult to program, and too big for the available space.

By dividing the different tasks among several processors in a single system, the STD 32 STAR SYSTEM proved to be the best solution.

The STAR SYSTEM solution implemented here features a 486-based processor with local bus video to handle the Windows-based user interface with exceptional performance. All the PLC functions are handled by a second processor running a ladder logic program. This processor is connected to a distributed I/O subsystem via a serial link. A third processor controls the analog functions from a simple-to-develop QuickBASIC program. The programs communicate via common memory and shared files. The Windows-based programs access the common memory via DDE (Dynamic Data Exchange).

Each processor loads its program from a shared hard disk. Program updates can be sent to each processor via the shared floppy drive (see the Technical Highlight sidebar). The entire system measures less than 15" by 6" by 8", and cost far less than the company expected.

With Windows and the GUI on a separate processor, the process control is never delayed or interrupted. In fact, the Windows-based processor can be reset while the control portion of the process continues to operate uninterrupted. This improves the system's reliability and "maintainability."

Should the manufacturer wish to upgrade its equipment in the future, it can easily enhance the STAR SYSTEM by adding processors to support new features or new functions.

Technical Highlight:

Shared Resources Peripherals

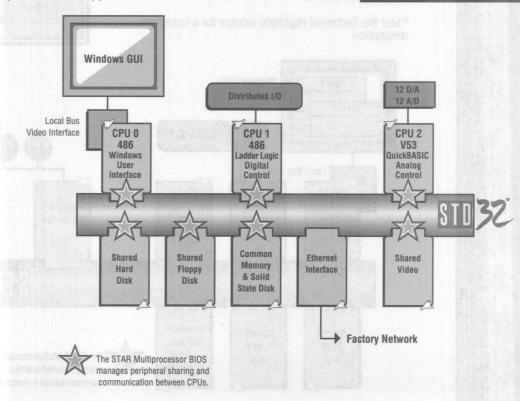
Any I/O card in the STAR
SYSTEM's STD 32 backplane can be
shared by all the processors in the
system. The sharing of DOS peripherals such as video, keyboard, hard
disks, floppy disks and solid state
disks is managed by a multiprocessing BIOS called STAR BIOS. All STAR
SYSTEM processors can boot from
shared disks or local Flash EPROM
disks. The processors can read from
every hard disk partition in the system, but only one processor can
write to any one partition at a time.

Common Memory

STAR SYSTEM processors use 32 Kbytes of common memory to share data and communicate with each other. The processors manage semaphores or use BIOS-level routines to coordinate common memory usage. This allows Windows programs to use the STAR DDE server to transparently move data into DDE variables via the common memory. The DDE variables can then be accessed by any program.

NetBIOS adds an industry standard software communications mechanism to the system. This lets STAR SYSTEM processors pass information among themselves, just like a network

15-31



Fast Track Development Using Multiprocessing

A systems integration company that builds complex, customized systems for the steel industry, needed to update its basic system design to remain competitive. Configuring new systems had to be quick and efficient, even though each system presented its own unique configuration challenges.

To shorten the software development cycle and meet real-time requirements, the new design had to combine a Windows-based graphical user interface (GUI) with one or more specialized control functions, yet keep those GUI and control functions on separate modules. It also needed to connect to the steel plant's existing network.

The STD 32 STAR SYSTEM's modular architecture was ideal for the application, and met both the user interface and real-time requirements. With the STAR SYSTEM, the integrator was able to use an off-the-shelf software package for the user interface, a ladder logic program to control the digital I/O, and a "C" language program for the motion control functions.

While the control programs for each function were written separately, these programs were able to work in parallel, using the STAR SYSTEM's common memory to exchange data. The Windows program automatically updated variables, using the STAR DDE* server to access the data in common memory. When all of the programs were integrated, system designers were able to view the operation of each processor through the STARWindows Console*. This allowed them to fine-tune the ladder logic control program, and monitor the entire system when it was up and running.

Using the existing STAR SYSTEM as the hardware base, the systems integrator can now easily configure new systems by modifying software modules. Similarly, systems can be configured with new functions by simply adding processors and control programs. This modular approach minimizes interference with the rest of the process and does not affect overall system performance.

* See the Technical Highlight sidebar for a complete description.

Technical Highlight:

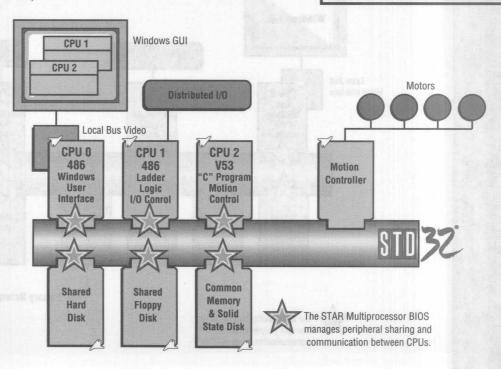
STARWINDOWS

Graphical user interfaces (GUIs), such as Wonderware's InTouch, and Microsoft's Visual BASIC have become extremely popular with industrial system designers. System builders appreciate these mostly Windowsbased programs because they simplify system configuration and are easy to use. In the past, Windows-based GUIs have presented a problem for control applications, because it is impossible to guarantee reliable real-time response on a processor that is running a Windows GUI. The STD 32 STAR SYSTEM solves this problem by assigning the GUI functions and the real-time functions of an application to different processors. Ziatech's STARWindows option makes this possible with tools that help the designer integrate the user environment with realtime processors.

The STARWindows option is comprised of three parts — STAR DDE, STAR Console, and Microsoft Windows.

The STAR DDE server supports the Dynamic Data Exchange (DDE) mechanism of Windows, the popular feature that allows data sharing between applications. STAR DDE lets non-Windows processors share data with Windows applications by passing the data through common memory. Only one processor bears the Windows program overhead, and it does this independently of the other processors in the system. This guarantees uninterrupted real-time response from all the non-Windows processors.

STAR Console lets the system designer view each processor in the STAR SYSTEM through its own window. Up to four of these windows can be open simultaneously, and can display any text-based application (i. e., Turbo Debugger, Turbo C or QuickBASIC). This allows different programs to be developed simultaneously for different processors.



Integrating Different Applications into a Single System

A material processing company wanted to reduce the overall size and cost of its system, without losing its investment in software. The existing system was both complex and wasteful, with four different PC-based machines, each with its own unique software configuration. The four machines communicated with each other through NetBIOS-compliant calls over a network. The company wanted to combine these functions into a single system.

A four-processor STD 32 STAR SYSTEM, complete with local bus video, provided a solution that met all of the company's requirements. Each processor in the STAR SYSTEM was recognized by the system software as a separate PC. The multiprocessing STAR BIOS made it possible for each CPU to act independently but to also share system peripherals such as the monitor, keyboard, and hard and floppy drives. This allowed the existing software to run unmodified.

Compressing four original PCs into a single system eliminated the space and cabling problems of the old system. Since the STAR SYSTEM incorporates the same NetBIOS standard as the original network, the different programs running on the different processors were still able to communicate and exchange data.

The various I/O functions of the original system were easily incorporated into the new system. Each application program retained direct access to all the same I/O. Some applications connected through distributed I/O, using the processor's on-board serial port. Other applications shared I/O interfaces plugged into the STAR SYSTEM's STD 32 backplane. Since on-board I/O is local to each processor in the STAR SYSTEM, this local I/O does not conflict with I/O shared over the backplane. In the case of this application, minor software changes eliminated any address conflicts with the I/O shared on the backplane.

Instead of four PCs with four separate displays, the new system features one GUI which lets the operator view any of the applications, switching from one to another using a "hot key" sequence.

The company hopes to eventually port the operator interface to a single program on a single processor, and use less powerful processors to run the control programs. In the mean time, the quickly implemented STAR SYSTEM design provides a cost-effective solution to a major operational and packaging problem.

Technical Highlight:

Video Choices in a Multiprocessing System

The user interface in a STAR SYSTEM can be driven in several ways, depending on the system requirements.

In one configuration, each processor shares a single video board, display, and keyboard. The user can "switch" control of these resources from processor to processor using a "hot key" sequence or a software function call. When a processor receives control of the video card, the display is automatically updated with the current state of the application running on that processor. The STAR SYSTEM's STAR BIOS makes this possible through its use of "virtual" video memory, which emulates an actual video card.

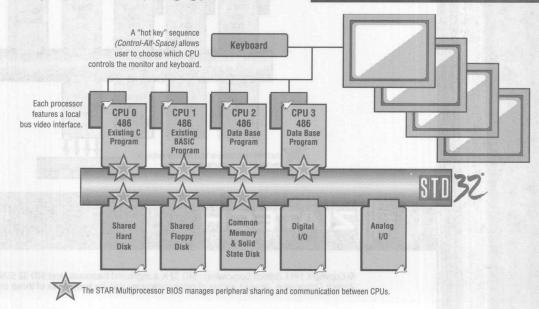
When the user switches control of the physical video card to a particular processor, the display is updated from the virtual video memory. The processor that loses control of the physical video board sends video output to its own virtual video memory instead. The entire process is transparent to the application program and the user.

This feature supports text mode applications only, so it is ideal for development and debugging using popular text-based tools such as Borland C++ and Turbo Debugger. (Graphics mode applications require a dedicated video card.)

The multiple graphics configuration puts a local bus video adapter on each of the computers in a system. The video adapters are linked together via a cable that connects them to a single Super VGA monitor and keyboard. Each adapter can operate in a different video mode. Like the first configuration, the user can switch between processors with a keyboard command, regardless of video mode.

Each processor/adapter combination can also drive independent monitors and keyboards for applications that require full-time viewing.

A single STAR SYSTEM can include a combination of the three configurations described above, depending on the application requirements.



Multitasking and Multiprocessing in a Supervisory Control System

A complex supervisory system required three user interfaces and fast updates of real-time data. The system also needed to communicate through a high-speed communications link, and through a standard computer network. In addition, the entire system had to fit in a small control room.

The designers decided to use a multitasking operating system because of the complexity of the design, and the number of simultaneous functions it had to perform. The traditional approach would have dedicated a network of PCs to handle each operator interface, while another PC operated the front-end communication. But the company needed a more compact, higher performance solution.

A four-processor STD 32 STAR SYSTEM solved the problem. The QNX Real-Time Operating System was installed on each of the processors. QNX was chosen because its built-in real-time and multitasking capabilities provided enough performance for the application. Its built-in networking features made communication between processors transparent to the programmer. (See the Technical Highlight sidebar.)

In the STAR/QNX configuration, three 486 processors, each with its own local bus video module, control the system's three operator interfaces. The screen handlers and data base functions run as tasks on each processor. While one processor operates the disk and acts as the file server, another processor provides access to the main Ethernet network. The operating system bridges the STAR SYSTEM backplane and the Ethernet network.

The fourth processor acts as the front-end for the high-speed communications subsystem and provides critical alarm monitoring for the plant. Because this processor must operate uninterrupted, it loads its own copy of the operating system and its application tasks from local Flash memory. This allows it to operate independently of the other processors.

Assigning the various functions to multiple computers makes the system more reliable, and greatly improves its performance. The STAR SYSTEM/QNX combination condenses the performance and functionality of an entire network into a cost-effective, single system that fits in a 19-inch rack below the operator console.

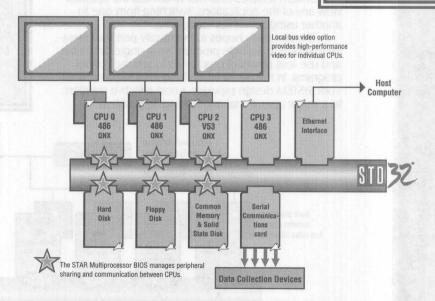
Technical Highlight:

QNX Real-Time Operating System

The marriage of the QNX Real-Time Operating System and the STAR SYSTEM has created an ideal environment for running complex, high-performance applications.

QNX adds a network-like software layer to the STAR SYSTEM. Complex tasks are divided among processors, and communicate with each other using standard ONX calls. The operating system assigns certain tasks to specific processors. For example, one processor-the "disk server"-typically provides disk services to the others through the STAR SYSTEM's "backplane network." (In harsh environments, STAR SYS-TEM "disks" can be rugged, solid state memory.) The physical location of each task is transparent, so it is easy to move tasks between processors. The combination improves overall system performance and simplifies configuration.

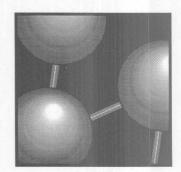
QNX lets processors request a copy of the operating system and applications from the disk server and store them in Flash memory. Applications can then access a complete version of the operating system and applications at all times. This guarantees that critical operations can run even if the processors in the system are unable to communicate with each other.





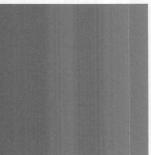
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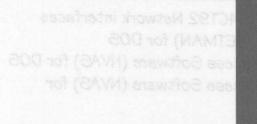
LONWORKS Control Network Products



16







LonWonks Control Network Products

Inside This Section

- ZT 88CT92 and ZT 14CT92 Network Interfaces
- Network Manager (NETMAN) for DOS
- Network Variable Access Software (NVAS) for DOS
- Network Variable Access Software (NVAS) for Windows

ZT 88CT92 and ZT 14CT92 Network Interfaces

for LonWorks™ Control Networks

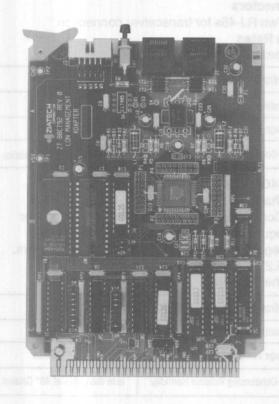
The ZT 88CT92 (STD 32®) and ZT 14CT92 (PC/AT) interfaces connect industrial PCs and desktop computers to networks of devices based on Echelon's Neuron® Chip.

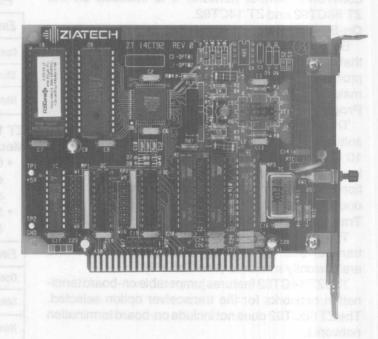
Ziatech's ZT 88CT92 and ZT 14CT92 provide LONWORKSTM control network connectivity for STD 32® industrial computers and PC/AT computers. LONWORKS control networking is new technology created by Echelon Corporation for use in distributed, intelligent control systems.

The Network Interfaces allow STD 32 and PC/AT Bus systems to configure, install, and monitor NEU-RON-based devices in the network.

Ziatech's Network Interfaces can be used as a network manager and a network monitor, or to transform an STD 32 or PC/AT computer into a simple node on a LONWORKS control network. The software used to support the network interface determines which one of these functions the interface will serve in the network.

The ZT 88CT92 and ZT 14CT92 operate within an extended temperature range of -40° to +85° Celsius.





- · STD 32 and half-slot PC/AT formats
- · Device driver software included
- LONWORKS management capability
- · Compatible with Echelon's API board software
- · Works with network management software
- 16-bit I/O address decode capability
- · Programmable clock frequencies
- · Service request push-button

- EPROM Socket
- Three twisted-pair transceiver options:
 - RS-485, 4.8 Kbps to 1.25 Mbps
- Isolated, 78 Kbps
 - Isolated, 1.25 Mbps
- Interrupt support
- Jumperable on-board termination network (PC/AT version)

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40° to +85° C. (Users should make adjustments for temperature rise in enclosures.)



Functional Considerations

Network Interfaces

Ziatech Network Interfaces make use of Echelon's 3150™ VLSI NEURON CHIP. Both interfaces provide software programmable input clock frequencies, three transceiver options, and a service request indicator/switch.

NEURON Communications

Each interface incorporates a NEURON CHIP which provides information exchange across the network media. All layers of the OSI networking model have been implemented with the LONTALK, firmware-based protocol. The 3150 NEURON CHIP utilizes external memory (EPROM) to store the LONTALK protocol and the Microprocessor Interface Program (MIP).

The Microprocessor Interface Program facilitates communication between the LonTalk network and the STD 32 or PC/AT host computer.

Microprocessor Interface Program (MIP)

This Echelon-developed program (mentioned in the API section above) translates Neuron management commands and responses as they enter and exit the LonWorks control network. It is included on the ZT 88CT92 and ZT 14CT92.

On-Board ROM

Both boards include 24 Kbytes of additional ROM that improves the throughput on the board. The Microprocessor Interface Program (MIP) is optimized to make best use of the memory.

Programmable Input Frequencies

The ZT 88CT92 and ZT 14CT92 interfaces allow software selection of all valid input clock frequencies: 10 MHz, 5 MHz, 2.5 MHz, 1.25 MHz, and 625 KHz. Lower input clock frequencies reduce power consumption for battery powered operation, but result in slower operation.

Transceiver Options

The interfaces communicate with the network via transceivers. Three serial, twisted-pair transceivers are currently available (see Table 1).

The ZT 14CT92 features jumperable on-board termination networks for the transceiver option selected. The ZT 88CT92 does not include on-board termination networks.

Service Pin

The NEURON service pin on the ZT 88CT92 and ZT 14CT92 is controlled by a push-button switch or with software. The NEURON may also drive the service pin with an LED visual status indicator.

Device Driver

The ZT 88CT92 and the ZT 14CT92 come with the Ziatech Network Interface device driver for DOS. This interrupt driven device driver is compatible with programs developed with Echelon's API. The driver disk also includes a Windows DDL for those who wish to program to the MIP from Windows.

Specifications

ZT 88CT92 (for STD 32 Bus)

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 mechanical specifications
- Measures 4.5" (11.3cm) by 6.5" (16.5cm)

Connectors

• Two RJ-45s for transceiver connection

Data Rates

Please refer to Table 1.

Environmental (ZT 88CT92)	
Operating Temperature	-40° to +85° Celsius
Storage Temperature	-65° to +150° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

ZT 14CT92 (for PC/AT Bus) Mechanical

- Compatible with IBM Personal Computers or equivalent. Contact Ziatech for information regarding compatibility with laptop computers.
- 5.2" (13.2cm) long by 4.2" (10.6cm) high (half-slot size)

Environmental (ZT 14CT92)		
Operating Temperature	0° to 65° Celsius	
Storage Temperature	-65° to +150° Celsius	
Non-Condensing Relative Humidity	less than 95% at 40° Celsius	

Option	Implementation	Speed	# Nodes	Length	Isolation
Default	RS-485	4.8 Kbps-1.25 Mbps	32	1,219-18 m • 4,000-60 ft.	Compatitive with Eq
01	Transformer Coupled	78 Kbps	64	1,372 m • 4,500 ft.	1.5 KV for 60s
02	Transformer Coupled	1.25 Mbps	64	457 m • 1,500 ft.	1.5 KV for 60s

Table 1. Serial, twisted-pair transceiver options

ZT 88CT92 and ZT 14CT92 Network Interfaces

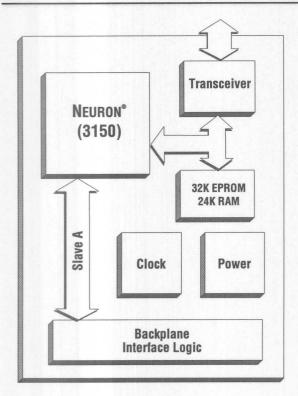


Figure 1. Functional block diagram

Connectors

Two RJ-45s for transceiver connection

Data Rates

Please refer to Table 1.

Reliability

- MTBF: 35 years
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 88CT92 Network Interface for the STD 32

Bus and driver diskette

(with RS-485 transceiver) ZT 14CT92

and driver diskette

Network Interface for PC/AT Bus

(with RS-485 transceiver)

Network Interface Transceiver Options

Select a transceiver option below if transformer coupling is required.

T0 RS-485 twisted-pair transceiver T1 Transformer-coupled 78 Kbps twisted-pair transceiver

T2 Transformer-coupled 1.25 Mbps

twisted-pair transceiver

Software Licensing

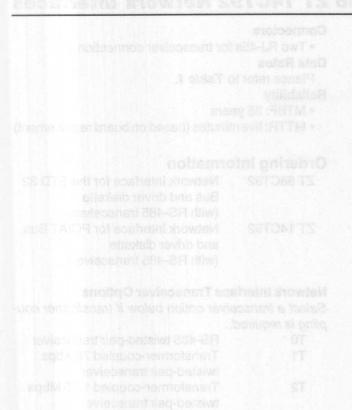
Ziatech and Echelon software can be licensed for use in production systems. Contact the respective companies for details.

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty - Five years with an optional five-year extension. See the full warranty statement in the Technical Data Book appendix.

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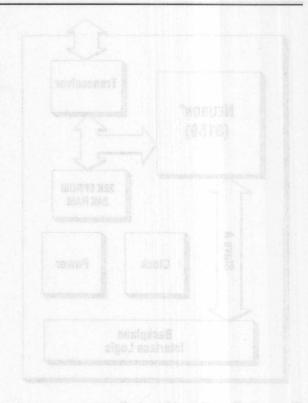






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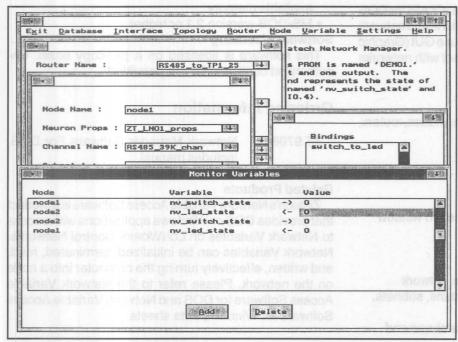
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ZIATECH



Network Manager Software for DOS



A screen view of the Network Manager Software for DOS

Ziatech's Network Manager Software for DOS provides network management, installation, and monitoring functions for LonWorks™ Control Networks.

Ziatech's Network Manager Software For DOS (NETMAN) is an interactive product allowing LonWorks network users to quickly and easily manage, install, and monitor networks using PC or STD computers.

NETMAN allows users to perform network functions (such as modifying network topology) in the lab, the field, or in any other location where a PC, STD computer, or laptop can be used.

The Ziatech Network Manager is designed for LonWorks users who need to have network management functions on site, away from their LonBuilder development system.

This is essential for installing and configuring larger networks (above 50 nodes). It provides a common set of functions that are required for configuration and ongoing maintenance of a LonWorks network. While the Ziatech Network Manager has the basic capabilities for monitoring network variables, it is not intended to be used as a complete network monitor. Such a network monitor is usually developed by the user for a specific application. NETMAN saves the developer time by eliminating the need to incorporate network management functions into a customized user interface.

for LonWorks™ Control Networks

- Easy-to-use
 Windows™-like GUI
 (Graphic User
 Interface)
- Simplifies building and maintenance of networks
- Smart pop-up windows simplify the building of network database entities
- Context-sensitive help
- Compatible with Avalon Technology's installation tool



NETMAN Architecture

NETMAN is compatible with the Echelon® API layer and can work with the Ziatech device drivers for the ZT 88CT92 and ZT 14CT92 Interfaces or any other interface with supported drivers.

NETMAN uses Echelon's LonManager™ API for DOS to provide network communication functions and network database access functions. An easy-to-use GUI (Graphic User Interface) allows the user to interact with networks and network databases.

Basic Functions

- Creates a network database, including nodes, routers, domains, subnets, channels, etc.
- Installs nodes and routers
- · Binds network variables
- Monitors network variables
- Updates network variables
- Provides context-sensitive help for each window

Advanced Functions

- Validates a network database
- Builds a network database from the network
- Creates network entities (e.g., domains, subnets, channels)
- Browses/edits/deletes a network database and its entities
- Replaces a node/router
- Resets a node/router
- · Takes a node off-line
- · Puts a node on-line
- Updates a node's memory
- Updates a node's location string
- Monitors critical nodes
- · Downloads an application
- Specifies channel transceiver characteristics

Functional Considerations

Product Description

The NETMAN package contains a DOS-executable application and a DOS-installable device driver. These modules are provided on a 3.5" diskette and are supported by a comprehensive manual.

System Requirements

- Network Management Interface Card—either a Ziatech ZT 14CT92 (PC-based systems) or a ZT 88CT92 (STD 32-based systems) suggested
- PC or STD computer system with 490 Kbytes of available memory
- MS-DOS-version 2.1 or higher

Software Licensing

This software is licensed on a per-copy basis. Unauthorized duplication is not permitted.

Ordering Information

ZT 97089

Network Manager Software For DOS, includes manual

Related Products

Ziatech's Network Variable Access Software is a product that provides DOS or Windows applications with access to Network Variables on Lonworks Control Networks. Network Variables can be initialized, terminated, read, and written, effectively turning the computer into a node on the network. Please refer to the Network Variable Access Software for DOS and Network Variable Access Software for Windows data sheets.

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

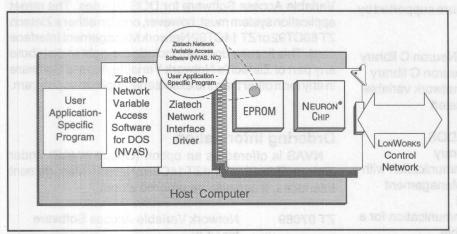
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Network Variable Access Software for DOS



Network Variable Access Software streamlines computer integration into LonWorks network

Software for PC/AT® and STD 32® Interfaces

Ziatech's Network Variable Access Software allows a DOS application to access network variables on LonWorks™ Control Networks.

Ziatech's Network Variable Access Software for DOS (NVAS) allows system designers to quickly and easily integrate a PC or STD 32 computer into Echelon's LonWorks Control Networks.

Integration is accomplished by providing boot applications with access to the Neuron® C program's network variables. This effectively turns a PC or STD 32 computer into a high-powered network node which can be used for monitoring and/or control. A graphical user interface and/or mass storage devices can be used on this "node."

Functions are provided that initialize, terminate, read, write, and determine the update status for network variables.

Software Architecture

NVAS is implemented in three modules—a NEURON Clibrary, a DOS installable device driver, and a DOS application library on Windows DLL. The figure above illustrates the

communication paths between modules.

The NEURON C library is implemented as an "include file" for a userwritten NEURON C program. It executes on a Ziatech ZT 14CT92 or ZT 88CT92 Network Management Interface card. The user must provide application-specific code to declare the network variables, initialize the library, notify the library of updates to any input network variables, and to copy data between the network variables and a buffer.

The DOS installable device driver is added to the system by adding a line to the CONFIG.SYS file. The driver manages all message passing between the DOS application and the NEURON CHIP on the interface card. Message queues are also provided and managed by the device driver.

The DOS application library provides the user-written and Windows DLL application with functions for initializing communication, terminating communication, reading network variables, writing network variables, and determining the update status for network variables.

For LonWorks™ Control Networks

- Provides access to both input and output network variables
- Supports basic NEURON
 C variable types,
 Standard Network
 Variable Types (SNVTs),
 user-defined structures,
 and user-defined unions
- Provides status for network variables to determine whether a variable has been updated
- Supports up to 62 network variables in any combination
- No recurring license fees
- Provides libraries for small, medium, compact, and large memory models for both Microsoft C[®] and Borland C++™ compilers
- Windows DLL included



Functional Considerations

Product Description

NVAS is a software package containing a Neuron C library, a DOS-installable device driver, and a DOS application library and a Windows DLL. These modules are provided on a 3.5-inch diskette and are supported by a comprehensive manual.

Neuron C Library Functions

NvasInit Initializes the Neuron C library
NvasNvUpdated Notifies the Neuron C library

that an input network variable has been updated

DOS Application Library Functions

NvasInitSw Initializes the DOS application library

NvasInitHw Initializes communication with

the Network Management

Interface card

NvasInitNv Initializes communication for a

network variable

NvasGetNv Copies the current value of a

network variable to the corresponding DOS application variable

NvasSetNv Copies the current value of a

DOS application variable to the corresponding network

variable

NvasNvStatus Reports the status of a

network variable

NvasExit Terminates communication

with the Network Management

Interface card

Language Support

- Microsoft C (version 5.1 or later)
- Borland C++ (version 2.0 or later)

System Requirements

- Network Management Interface card, either Ziatech ZT 88CT92 (STD 32-based systems) or ZT 14CT92 (PC-based systems)
- C compiler, either Microsoft C (version 5.1 or later) or Borland C++ (version 2.0 or later)
- Echelon LonBuilder™ Development System
- MS-DOS® (version 2.1 or later)

Software Licensing

The purchase of Ziatech's Network Variable Access Software includes a license to duplicate, for the specific target application, the DOS-installable device driver, and executable application programs utilizing the Network Variable Access Software for DOS libraries. The target application system must, however, contain either a Ziatech ZT 88CT92 or ZT 14CT92 Network Management Interface card. This license does not include the right to distribute any part of Ziatech's Network Variable Access Software in any form other than the executable application program.

Ordering Information

NVAS is offered as an option (Option NVAS) under Ziatech ZT 88CT 92 and ZT 14CT 92 Network Management Interfaces. It can also be ordered alone.

ZT 97089 Network Variable Access Software for DOS

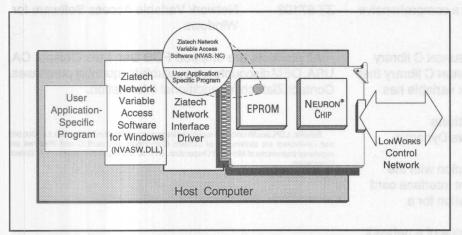
All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

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Network Variable Access Software for Windows



Network Variable Access Software streamlines computer integration into LONWORKS network

Software for PC/AT® and STD 32® Interfaces

Ziatech's Network Variable Access Software for Windows (NVASW) allows system designers to quickly and easily integrate a Windows-based PCorSTD32computerinto Echelon's LONWORKS™ control networks.

Integration is accomplished by providing boot applications with access to the NEURON™ C program's network variables. This effectively turns a PC or STD 32 computer into a high-powered network node which can be used for monitoring and/or control. A graphical user interface and/or mass storage devices can be used on this "node."

Functions are provided for initialization, termination, reading, and writing network variables. Messages are posted to the Windows application when network variables are updated.

Software Architecture

NVASW is implemented in three modules - a NEURON C library, a Windows installable device driver, and a Windows Dynamic Link Library (DLL). The figure above illustrates the communication paths between modules.

The NEURON C library is implemented as an "include file" for a userwritten NEURON C program. It executes on a Ziatech ZT 14CT92 or ZT 88CT92 Network Management Interface card. The user must provide application-specific code to declare the network variables, initialize the library, notify the library of updates to any input network variables, and to copy data between the network variables and a buffer.

The Windows installable device driver is added to the system by adding a line to the CONFIG.SYS file. The driver manages all message passing between the Windows application and the NEURON CHIP on the interface card. Message queues are also provided and managed by the device driver.

The Windows DLL provides the user-written and Windows application with functions for initializing communication, terminating communication, reading network variables, and writing network variables. The DLL also sends messages to the application when network variables are updated.

For LONWORKSTM Control Networks

- Provides access to both input and output network variables
- Supports basic Neuron C variable types, Standard Network Variable Types (SNVTs), user-defined structures. and user-defined unions
- Provides messages to Windows applications when network variables are updated
- Supports up to 62 network variables in any combination
- No recurring license fees
- Provides Microsoft Windows Dynamic Link Library (DLL)



Functional Considerations

Product Description

NVASW is a software package containing a NEURON C library, a Windows installable device driver, and a Windows Dynamic Link Library. These modules are provided on a 3.5-inch diskette and are supported by a comprehensive manual.

Neuron C Library Functions

NvasInit Initializes the Neuron C library
NvasNvUpdated Notifies the Neuron C library that

an input network variable has been updated

Windows Application Library Functions

NvaswInitSw Initializes the Windows Dynamic

Link library

NvaswInitHw Initializes communication with the

Network Management Interface card

NvaswInitNv Initializes communication for a

network variable

NvaswGetNv Copies the current value of a network

variable to the corresponding Windows application variable

NvasSetNv Copies the current value of a

Windows application variable to the corresponding network variable

NvasExit Terminates communication with the

Network Management Interface card

Language Support

Microsoft C[®] (version 5.1 or later)

Borland C++™ (version 2.0 or later)

System Requirements

Network Management Interface card, either
 Ziatech ZT 88CT92 (STD 32-based systems) or
 ZT 14CT92 (PC-based systems)

 C compiler, either Microsoft C (version 5.1 or later) or Borland C++ (version 2.0 or later)

Echelon LonBuilder™ Development System

MS-DOS (version 2.1 or later)

Microsoft Windows (version 3.1 or later, 386 enhanced mode only)

Software Licensing

The purchase of Ziatech's Network Variable Access Software includes a license to duplicate, for the specific target application, the Windows installable device driver, and executable application programs utilizing the Network Variable Access Software for Windows libraries. The target application system must, however, contain either a Ziatech ZT 88CT92 or ZT 14CT92 Network Management Interface card. This license does not include the right to distribute any part of Ziatech's Network Variable Access Software in any form other than the executable application program.

Ordering Information

NVASW is offered as an option (Option NVASW) under Ziatech ZT 88CT92 and ZT 14CT92 Network Management Interfaces. It can also be ordered alone.

ZT 97103 Network Variable Access Software for Windows

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

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CT and LT Products

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Inside This Section

- CT and LT Product Listing/Directory
- CT and LT Products: An introduction to low power, extended temperature products

CT and LT Products (Low Power/Extended Temperature)

About Ziatech CT and LT Products

Ziatech extended temperature products are available in both CT (CMOS, TTL-compatible) and LT (Low Temperature) versions. Many of Ziatech's products are available in low power/extended temperature "CT" versions. A few advanced products are available in low temperature "LT" versions. Both CT and LT product data sheets are featured throughout the databook. This section features a brief listing of Ziatech's CT and LT product line, which shows the typical power consumption figures and page numbers of specific CT and LT product data sheets in this publication. The section also includes a discussion of Ziatech's CT and LT technology.

Extended Temperature Products (-40° to +85° Celsius)

Ziatech's CT products for STD Bus, PC/AT Bus, and SBX standards are designed for harsh environments where a computer must operate under extreme temperature conditions. In addition to burn-in at elevated temperatures, Ziatech assures CT product performance through rigorous design verification testing which stresses the CT product throughout an extended temperature range. Periodically, random product samples are tested under harsh conditions to ensure continued product performance in severe environments.

Low Power Products

Industrial applications often combine a wide temperature requirement with a need for reduced power consumption. The CT product line meets the demand of these applications with low power CMOS components.

Low Temperature Products (-40° to +65° Celsius)

Some advanced products are not available in full industrial temperature ranges. Ziatech's rigorous design, test and inspection enables selected LT products to operate in an extended low temperature range. Please contact Ziatech for details on availability of LT products.

Complete System Available

CT Products are available for most system functions. LT products are available for selected advanced products. CT and LT products are available separately or in integrated systems, and are compatible with TTL boards.

Increased Reliability from 0° to 70° Celsius

CT computer products increase system MTBF (Mean Time Between Failure) from 15 to 25 percent when used in standard temperature ranges of 0° to 70° Celsius.

Directory of Products

Part Number	umber Description	Bus	Typical Power Consumption		Data Book Page
	awo 9 leptoy T	Dus	+5V	+12V	Number
ZT 88CT01	Single Board V40 Computer	STD/STD 32	430mA	-	3-3
ZT 88CT02	Single Board V40 Computer	STD/STD 32	550mA	-	3-7
ZT 88CT09A	Single Board 80C88 Computer	STD/STD 32	200mA	15mA	3-11
ZT 88CT25	Expanded Memory System	STD/STD 32	100mA		5-3
ZT 88CT41	Quad Serial Interface	STD/STD 32	92mA	30mA	7-3
ZT 88CT46	Real-Time Event Sense Interface	STD/STD 32	600mA		9-7
ZT 88CT49A	Optically Isolated Digital Input Interface	STD/STD 32	30mA	h Zietuch te	9-11
ZT 88CT62	Optically Isolated Input and Counter/ Timer Interface	STD/STD 32	11mA	-	9-15
ZT 88CT72	144-Point Digital I/O Interface	STD/STD 32	32mA	-	9-17
ZT 88CT73	Optically Isolated Industrial I/O Interface	STD/STD 32	235mA	-	9-21
ZT 88CT75	Centronics and Serial Interface	STD/STD 32	60mA		7-9
ZT 88CT85	DC to DC Power Supply	STD/STD 32	Contact Ziatech	Contact Ziatech	14-53
ZT 88CT92	Network Interface	STD/STD 32	1.1		16-3
ZT 88CT93	STDIM™ for GE Fanuc Genius™ I/O	STD/STD 32	450mA	-	8-3
ZT 89CT01	Single Board V53 Computer	STD/STD 32	350mA	1mA	3-15
ZT 89LT02	Single Board 486 Computers	STD/STD 32	Contact Ziatech	Contact Ziatech	3-19
ZT 89LT11	Scalable Processor Board	STD 32	230mA	-	3-25
ZT 89CT20	32-Bit Memory System	STD 32	200mA	_	5-7
ZT 89LT21	PCMCIA 2.0 Interface	STD/STD 32	180mA	-	5-9
ZT 89CT30	Integer DSP Control Processor	STD/STD 32	600mA	-	4-11
ZT 89CT39	Slot X Arbiter Interface	.STD 32	110mA	-	15-17
ZT 89CT61	96-Point Digital I/O Interface	STD/STD 32	35mA	-	9-25
ZT 89CT90	ARCNET Interface	STD/STD 32	Contact Ziatech	Contact Ziatech	8-9



CT and LT Products (Low Power/Extended Temperature)

Directory of Products (continued)

	Part Number	Description	Bus	Typical Power Consumption		Data Book
	Part Number		Dus	+5V	+12V	Page Number
PC/AT	ZT 14CT72/73	192-/48-Point Digital I/O Interface	PC/AT	Contact Ziatech	Contact Ziatech	19-3
PC	ZT 14CT92	Network Interface	PC/AT	Contact Ziatech	Contact Ziatech	16-3
X	zSBX CT31	48-Point Digital I/O Interface	SBX	32mA		18-7
SBX	zSBX CT32	Centronics and Serial Interface	SBX	55mA	150mA	18-9

CT and LT Products

Extended Operating Temperatures

An introduction to Ziatech's CT and LT Technology: Extended temperature range and normal operation with standard STD products

CT and LT Technology

Ziatech extended temperature products are available in CT and LT versions. CT (CMOS, TTL-compatible) products feature an extended operating temperature range of -40° to +85° Celsius and reduced power consumption, while LT (low temperature) products feature an extended operating temperature range of -40° to +65° Celsius.

CMOS and TTL Logic Levels Differ

Complementary Metal Oxide Semiconductor (CMOS) is one of several semiconductor chip manufacturing technologies. There are faster technologies than CMOS, but CMOS chips have unique features. For industrial use, the most important advantages of CMOS components are low power consumption and an extended operating temperature range.

CMOS circuits operate on different logic levels than normal TTL logic. Logic levels are specified as low and high voltages for output (driving) circuits and input (receiving) circuits. For example, VIL stands for the lowest voltage an input circuit will recognize as a logic 0, whereas VOL specifies the lowest voltage an output circuit is permitted to drive for a logic 0. The following table shows the specification for both TTL and CMOS circuits.

	TTL	CMOS
VIL	V8.0	0.9V
Vol	0.3V	0.4V
VIH	2.0V	3.1V
Vон	2.4V	3.8V

The table illustrates that CMOS specifications are wider than TTL, which means that any CMOS card can be read by a TTL card, but NOT the other way around.

STD Backplane Signals

The STD Bus defines backplane signal levels to be at TTL logic levels. The majority of STD Bus cards operate at TTL logic levels, but some STD cards operate at the wider CMOS voltage levels. Most TTL STD cards will operate with CMOS cards because the voltage ranges are close, but problems may occur if the

cards are close to the specified tolerances, causing unpredictable results. While mixing TTL and CMOS cards in an STD system may work, it is not recommended for reliable operation.

How can CMOS benefits be retained while maintaining compatibility with existing TTL boards? CT and LT Technology, which Ziatech uses in selected STD, PC/AT and SBX products, provides the answer.

CT and LT Technology

Ziatech's CT and LT technology uses CMOS circuits with TTL logic levels. This technology delivers the benefits of CMOS while retaining full compatibility with TTL circuits. In fact, using CT and LT technology means CMOS components can be used in place of TTL on a board wherever possible, while retaining TTL where equivalent CMOS parts do not exist. Ziatech boards use CMOS/CT components wherever possible to minimize power consumption. However, only CMOS/CT-only boards will bear a CT label, designating an extended temperature, low-power board. Certain high-performance Ziatech products are available in LT versions when components that provide the full extended temperature range are not available.

LT and CT Printed Circuit Boards

Ziatech uses special Printed Circuit Board (PCB) materials in CT and LT products. All PCBs expand and contract when the temperature changes, which can destroy connections on the PCB, both within the board itself, as well as from the board to the chips. In extended temperature conditions, exaggerated PCB expansion and contraction can result in unreliable operation and a shortened product lifetime. When appropriate, Ziatech's LT and CT technology uses special PCB materials that were originally developed for the aerospace industry. These materials minimize board expansion and contraction, resulting in more reliable products with higher MTBF (Mean Time Between Failure) ratings.

CT Technology Benefits

Ziatech uses the CT designation for boards intended for low power and extended temperature operation of

ZIATECH

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-40° to +85° Celsius. These boards incorporate complete CT technology, using only components that operate across the entire -40° to +85° C temperature range. In a few cases, a particular component not available in a CT version is replaced with a wide temperature version using other technologies.

Certain CT products can not cost-effectively meet both the low power and wide temperature goals. Many very low power components are not available in wide temperature versions, or, if they are, they are extremely expensive. When a compromise must be made, Ziatech places highest priority on providing a wide operating temperature range for CT-designated boards.

LT (Low Temperature) Technology Benefits

Ziatech uses the LT designation for boards with an extended operating temperature range of -40° to +65° Celsius. Wherever possible, LT boards incorporate extended temperature technology, using components that operate across the entire -40° to +85° C temperature range. When a particular component for this operating temperature range is not available, a qualified low temperature (-40° to +65° Celsius) part is used.

Care is Needed for Wide Temperature Designs

Designing for wide temperature is not as simple as choosing components with the necessary rating, because signal timings vary over the temperature range. Thus, a wide temperature design must meet the timing requirements over the entire temperature range. Simply replacing TTL parts with their CT or LT equivalents may result in a product that contains wide temperature components, yet only operates correctly over the standard commercial temperature range of 0° to 60° C.

Ziatech takes extreme care to calculate and test timings for all the components used in its CT and LT products. This ensures all CT and LT products will meet timing requirements over the entire operating temperature range, and illustrates Ziatech's attention to detail during the CT and LT design and manufacturing cycle. All of Ziatech's hardware is tested in an environmental chamber before shipping.

Summary

While Ziatech's CT and LT products use CMOS components extensively, they still operate with standard STD and STD 32 TTL boards. Ziatech uses "CT" to designate extended temperature/low power designs, and "LT" to designate low temperature designs. Ziatech exercises extreme care to ensure its CT and LT designs operate properly over the entire extended temperature range.

For information about Ziatech's CT and LT products for STD 32, PC/AT, and SBX products, see the CT/LT product directory or the individual product data sheets. Contact Ziatech directly for further information on the growing family of CT and LT products.



SBX Expansion Modules

		40
		18
		Service VERV

and REX 388 SEX modules are available through Zistech and observe's SEX products is included in this section. For the competent, Robotical can also be contacted directly at (458) 633-2001.



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SBX Expansion Modules Product Feature Guide

Manufacturer	Product	Input	Output	Type and Quantity of Channels	Maximum Sink Current	-40° to +85° C
Ziatech	zSBX 20 GPIB Controller Interface	•	•	(1) IEEE 488 (GPIB)		
Ziatech	zSBX 30 Parallel I/O Interface	٠	+	48 points parallel	1.7mA	
Ziatech	zSBX CT31 48-Point Digital I/O Interface	•	*	48 points parallel	12mA	٠
Ziatech	zSBX CT32 Centronics and Serial Interface	٠	•	(2) RS-232/485 (8) parallel	12mA	٠
Robotrol*	RBX 311 Analog Input Card	•		(8) Differential or (16) Single-ended Analog Inputs	-	
Robotrol*	RBX 388 Analog I/O Card	٠	*	(8) Differential or (16) Single-ended Analog Inputs and (8) Analog Outputs	-	

^{*} Robotrol Corporation's RBX 311 and RBX 388 SBX modules are available through Ziatech and Robotrol. A brief description of Robotrol's SBX products is included in this section. For the complete technical data sheets, contact Ziatech. Robotrol can also be contacted directly at (408) 683-2000.

zSBX 20

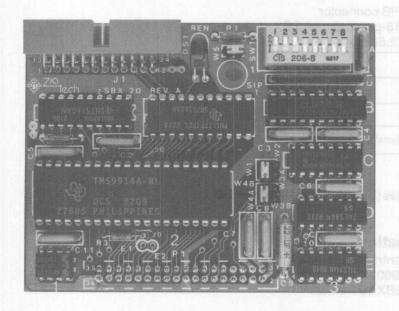
GPIB Controller Interface

GPIB controller interface reduces system interfacing cost, I/O complexity, and programming time

The zSBX 20 expansion module controller brings all the benefits of the IEEE 488 General Purpose Interface Bus (GPIB) to any system that makes use of the standard SBX I/O Bus. The use of GPIB I/O can cut system costs dramatically, thanks to its multidrop feature. The zSBX 20 connects to up to 14 of the

4,000+ GPIB compatible instruments, peripherals, and computers.

Software support for the zSBX 20 is provided by Ziatech's C.488 software driver option. Other software driver options may be applicable, depending on the hardware and software environment. Contact Ziatech for details.



- Conforms to IEEE 488-1978 Standard
- zSBX-, SBX-, BLX-, expansion module-compatible
- · Complete controller, talker, and listener capability
- Several GPIB drivers available
- Burned in at 55° C and tested to guarantee reliability



Specifications

Compatibility

- IEEE 488.1- and IEEE 488.2-compatible
- Size-and backplane-compatible with the MULTIMODULE® (IEEE 959) specification

Electrical

· Data Rate:

Programmed I/O: 30 Kbytes/second DMA I/O: 300 Kbytes/second Command rate (ATN asserted): 20 Kbytes/second

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V		480mA	700mA

Mechanical

- Size- and backplane-compatible with the MULTIMODULE (IEEE 959) specification
- Connectors

J1: Male GPIB connector

P1: 36-pin (18-pin dual-row) SBX connector on 0.1" (2.5mm) centers.

Environmental	
Operating Temperature	0° to 65° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 95% at 40° Celsius

Reliability

• MTBF: 93 years

MTTR: five minutes (based on board replacement)

Ordering Information

zSBX 20 GPIB Controller Interface (SBX Module) with ZT 90010 cable included ZT MzSBX 20 zSBX 20 manual

Accessories

Cables (see Data Book cable section for details):

ZT 90002 40" (1m), round, 26-pin to female

IEEE 488

ZT 90003 40" (1m), flat, 26-pin to female

IEEE 488

ZT 90005 82" (2m), round, 26-pin to stackable

IEEE 488

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.

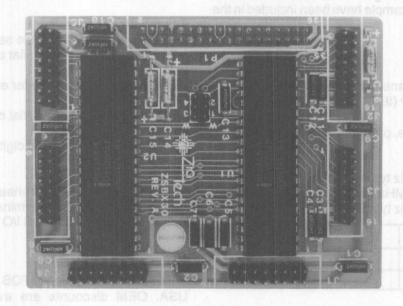


zSBX 30 Parallel I/O Interface

SBX module adds 48 bidirectional, parallel I/O lines to industrial computers equipped with an expansion module connector

The zSBX 30 expansion module facilitates on-board I/O expansion to 48 programmable I/O lines via the SBX I/O Bus. The zSBX 30 can cut system costs by eliminating additional I/O boards and saving card

slots. The zSBX 30 increases programmable parallel I/O capability to 48 I/O lines with or without handshaking capability.



- zSBX-, SBX-, iSBX-, BLX-expansion module-compatible
- · Optional interrupt requests and handshaking
- Each connector provides eight data lines, ±12V,
 +5V, and ground for user interfacing
- No power-up glitching on I/O lines
- Burned in at 55° C and tested to guarantee reliability



Hardware

The zSBX 30 utilizes two 8255A-5 general purpose programmable I/O chips. Each consists of 24 I/O lines which can be individually programmed in two groups of twelve or three groups of eight, and can be used in three major modes of operation.

The three modes of operation available are:

- Mode 0 basic input/output
- Mode 1 strobed input/output
- Mode 2 bidirectional bus input/output

In the first mode (Mode 0), each group of 12 I/O lines can be programmed in sets of four to be either input or output. In Mode 1, each group of 12 can be programmed to have eight lines of input or output. Of the remaining four lines in each group, three are used for handshaking and interrupt control signals. Mode 2 is a bidirectional bus mode which uses eight lines for a bidirectional bus, and five lines, borrowing one from the other group, for handshaking.

Complete programming information for the 8255A-5 and an application example have been included in the zSBX 30 manual.

Specifications Compatibility

 Size- and backplane-compatible with the MULTIMODULE® (IEEE 959) specification

Electrical

- 48 digital I/O lines, programmable in groups of eight or twelve
- Data Rates

Mode 0: 2.2 MHz typical Mode 1: 1.125 MHz typical Mode 2: 115 kHz typical

Power Req.	Min.	Тур.	Мах.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V		120mA	240mA

Mechanical

- The zSBX 30 is size- and backplane-compatible with the MULTIMODULE (IEEE 959) specification
- Connectors

J1-J6: 16-pin (8-pin dual-row) on 0.1" (2.5mm) center

Environmental	noleneux e na riffy
Operating Temperature	0° to 55° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 90% at 40° Celsius

Reliability

- MTBF: 90 years
- MTTR: five minutes (based on board replacement)

Ordering Information

zSBX 30 Parallel I/O Interface (SBX module) ZT MzSBX 30 zSBX 30 manual

Accessories

Cables (see Data Book cable section for details):

ZT 90021 10' (30.5cm), flat digital I/O, 50-pin to 50-pin card

ZT 90028 40" (1m), printer emulation, 50-pin to 25-pin

ZT 90072 10' (30.5cm), flat digital I/O, 50-pin both ends

ZT 90137 2' (61cm), flat digital I/O, 50-pin both ends

Boards (see separate data sheets for details):

ZT 2224 24-Line Termination Assembly ZT 2226 24-Channel I/O Mounting Rack

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

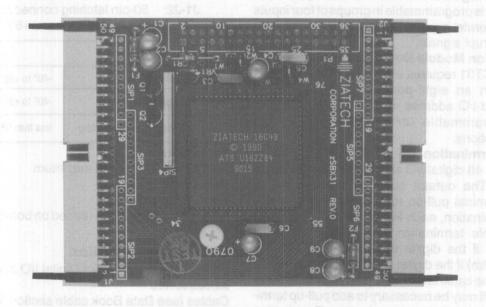
Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.



SBX expansion module interface provides 48 points of digital I/O to industrial computers

The zSBX CT31 expansion module interface provides 48 points of bidirectional digital I/O to any computer that utilizes the standard SBX I/O bus. This interface allows computers to connect to instruments, peripherals, and I/O mounting racks that use industry standard modules such as those manufactured by Ziatech, Opto 22, Gordos, Crydom, Grayhill, or equivalents.

The expansion module format can reduce system costs by providing I/O without the use of additional computer boards or card slots. The zSBX CT31 utilizes Application Specific Integrated Circuit (ASIC) technology to consolidate its I/O capabilities into the small expansion module format.



- zSBX-, SBX-, BLX-, expansion modulecompatible
- 48 bidirectional I/O signals with termination
- No power-up glitching on I/O lines
- 12mA sink current at V_{OL} of 0.4V

- · Write-protect mask register for output registers
- Self-contained power-up reset circuitry
- · Eight event sense inputs for interrupts
- Low power/extended temperature operation
- Compatible with industry standard I/O module mounting racks

Note: CT denotes CMOS, TTL-compatible, and extended temperature operation of -40° to +85° C. (Users should make adjustments for temperature rise resulting in enclosures.)



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Functional Considerations Digital I/O Operation

The zSBX CT31 includes 48 digital I/O signals. Each signal is individually programmable for input, output, or output with readback operation. The 48 signals are provided through two 50-pin latching connectors. Each connector is organized to provide 24 digital I/O signals with alternating grounds to improve noise immunity. Each connector also includes fused power (+5V at 1A) on pin 49 to provide logic power to the modules on I/O mounting racks capable of using ribbon cable power, such as Ziatech's ZT 2226 and some racks from Opto 22.

When programmed for output, inverting open collector and non-glitching operation is provided. Non-glitching outputs are desirable to prevent inadvertent I/O operation of a critical nature. Extensive effort is directed toward providing non-glitching outputs.

Event Sense Operation

Eight of the 48 I/O lines on the zSBX CT31 can sense a positive or negative transition on the input. Input sense polarity is programmable in groups of four inputs and can generate an interrupt via the MINTRO or MINTR1 interrupt signals.

SBX Expansion Module Bus Addressing

The zSBX CT31 requires eight consecutive I/O port addresses on an eight-port I/O boundary within the host board I/O address map. The zSBX CT31 is jumper-programmable for MPS0 or MPS1 I/O address selections.

Digital I/O Termination

Each of the 48 digital I/O signals includes resistive termination. The default configuration includes a 100k ohm nominal pull-up resistor within the ASIC. With this termination, each I/O signal can sink 12mA of current. This termination is adequate for most environments if the digital I/O cable length is less than 10 feet (3m) If the digital cable length exceeds 10 feet (3m), or the cable is located in an electrically noisy environment, it may be necessary to add pull-up termination or pull-up/pull-down termination. Termination network locations are provided for user-installed termination networks.

Signal Conditioning Modules

The zSBX CT31 provides direct control of 48 signal conditioning modules on two 24-channel racks using the industry standard 50-pin I/O module bus. These industrial modules control machinery for process control, automation, etc., while providing optical isolation. **Software Support**

Ziatech provides a linkable device driver for the zSBX CT31 in its STD Device Driver Package (STD DDP).

Specifications

Electrical

- 48 terminated bidirectional I/O lines
 - Inverting open collector operation
 - 100k ohm nominal pull-up resistor
 - V_{OH} = 3V minimum at -4mA
 - V_{OI} = 0.4V maximum at 12mA Input
 - Inverting buffers
 - 100k ohm nominal pull-up resistor

Power Req.	Min.	Тур.	Мах.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	Sordgs,	26mA	52mA

Mechanical

- · Size- and backplane-compatible with the MULTIMODULE® SBX specification (8-bit data)
- Connectors

P1: 36-pin MULTIMODULE Bus

J1-J2: 50-pin latching connectors for parallel

I/O, including fused +5V

Environmental					
Operating Temperature	-40° to +85° Celsius				
Storage Temperature	-40° to +85° Celsius				
Non-Condensing Relative Humidity	less than 95% at 40° Celsius				

Data Rates

125 Kbytes/second maximum

Reliability

MTBF: 75 years

MTTR: five minutes (based on board replacement)

Ordering Information

zSBX CT31 48-Point Digital I/O Interface Accessories

Cables (see Data Book cable section for details):

ZT 90021 10' (3m), flat 50-pin card edge connector

ZT 90022 9.5" (24cm), flat 50-pin both ends

ZT 90072 10' (3m), flat 50-pin both ends

ZT 90137 2' (61cm), flat 50-pin both ends

Boards (see separate data sheet for details):

ZT 2224 24-Line Termination Assembly ZT 2226 24-Channel I/O Mounting Rack

(Accepts Opto 22 "G4" and Grayhill

"G5" modules)

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information. Warranty - Five years with an optional five-year extension. See the full warranty statement in the Technical Data Book appendix.



Centronics and Serial Interface

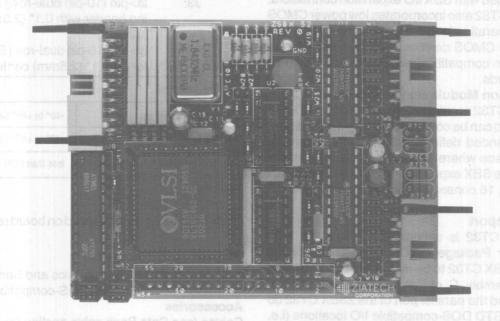
SBX expansion module interface provides two serial ports and a parallel I/O interface to industrial computers with SBX expansion capabilities

The zSBX CT32 SBX interface provides two serial ports and a parallel (Centronics) I/O port to any computer that utilizes the standard SBX I/O bus.

Either serial port on the zSBX CT32 can be configured for RS-232 or RS-485 DTE/DCE operation. The bidirectional, Centronics-compatible parallel port can operate as a byte-wide parallel I/O port when not being used as a printer interface. This flexibility allows

computers to expand their serial and parallel communications capabilities quickly and easily.

The SBX format reduces system costs by providing I/O without additional computer boards or card slots. The zSBX CT32 utilizes Application Specific Integrated Circuit (ASIC) technology to consolidate its I/O capabilities into this compact format.



- Operates with any SBX-equipped computer
- Exact SBX form factor, no porches or connector extensions
- Two fully programmable serial I/O channels, configurable for RS-232 or RS-485 operation
- Each serial channel is independently configurable as a DTE or DCE device
- Programmable baud rate generator and modem control signals for each serial channel
- Loopback controls for fault isolation on each serial channel

- Line break generation and detection for each serial channel
- Generation and stripping of serial data control bits (start, stop, parity)
- Software support via Ziatech's
 STD Device Driver Package (STD DDP)
- Complete status reporting capabilities
- Fully prioritized independent interrupt controls
- Bidirectional Centronics-compatible parallel port
- Low power and extended temperature operation (-40° to +85° C)

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40° to +85° C. (Users should make adjustments for temperature rise in enclosures.)



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Functional Considerations

Centronics and Serial SBX Interface

The 16C452 ASIC used by the zSBX CT32 features two fully programmable serial I/O channels with complete status reporting capabilities. The serial channels each have a programmable baud rate generator and modem control signals.

The data buffers for each channel are double buffered so that read and write operations can be performed at the same time the device is performing the parallel-to-serial and serial-to-parallel conversions. The interrupt structure of the 16C452 is fully prioritized with independent controls for each channel.

The 16C452 also features a bidirectional Centronics-compatible parallel port. When not being used as a printer interface, this port may be used as a byte-wide parallel I/O port.

The zSBX CT32 is compatible with all computer boards equipped with SBX I/O expansion connectors.

The zSBX CT32 also incorporates low power CMOS devices for operation in -40° to +85° Celsius environments. These CMOS devices are TTL-compatible to ensure system compatibility with both CMOS or TTL STD Bus boards.

SBX Expansion Module Bus Addressing

The zSBX CT32 requires eight consecutive I/O port addresses and can be configured to take advantage of Ziatech's extended definition of the SBX expansion module interface where additional address lines are provided to the SBX expansion module. When configured this way, 16 consecutive I/O port addresses are utilized.

Software Support

The zSBX CT32 is supported by Ziatech's STD Device Driver Package (STD DDP). This package allows the zSBX CT32 to be integrated into programs written in Assembly, C, or Pascal languages. The two serial ports and the parallel port of the zSBX CT32 do not reside at STD DOS-compatible I/O locations (i.e. COM1, COM2, and LPT1).

Specifications

Compatibility

 Size- and backplane-compatible with the MULTIMODULE® (IEEE 959) SBX specification

Electrical

· Data Rate: 56K baud maximum for serial ports

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.50V	5.00V	5.50V
Supply Current, V _{CC} =5.0V		55mA	55mA
Aux Voltage, V _{aux+}	10.8V	12.0V	13.2V
Aux Current, V _{aux+} = 12.0V	II SINDO	150mA	250mA
Aux Voltage, V _{aux} -	-13.2V	-12.0V	-10.8V
Aux Current V _{aux} - = -12.0V	M Interfac	150mA	250mA

Mechanical

- The zSBX CT32 is size- and backplanecompatible with the MULTIMODULE (IEEE 959) SBX specification
- Connectors

J1-J2:	14-pin (7-pin dual-row) male latching
	headers with 0.1" (2.5mm) lead
	spacing

J3: 20-pin (10-pin dual-row) male latching header with 0.1" (2.5mm) lead spacing

P1: 36-pin (18-pin dual-row) SBX connector on 0.1" (2.5mm) centers

Environmental				
Operating Temperature	-40° to +85° Celsius			
Storage Temperature	-40° to +85° Celsius			
Non-Condensing Relative Humidity	less than 95% at 40° Celsius			

Reliability

- MTBF: 70 years
- MTTR: five minutes (based on board replacement)

Ordering Information

zSBX CT32 Dual Centronics and Serial Interface (Not STD DOS-compatible)

Accessories

Cables (see Data Book cable section for details):

ZT 90014 40" (1m), 14-pin to 25-pin female D-shell ZT 90027 40" (1m), 14-pin to 25-pin

male D-shell

ZT 90074 32" (81cm), for printer, 20-pin to 25-pin female D-shell

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.

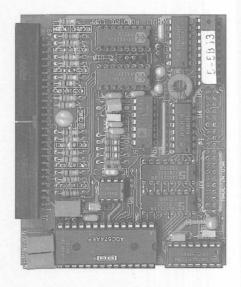


SBX Bus Analog I/O Products

from Robotrol Corporation

RBX 311 SBX Bus Analog Input Card

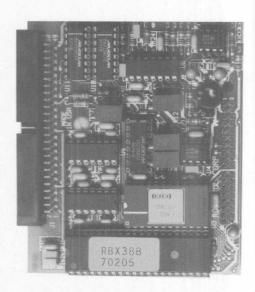
- 8 differential or 16 single-ended analog inputs
- 12-bit bipolar or unipolar resolution
- 30 kHz throughput rate (Optional 50 kHz throughput rate)
- Analog input ranges:
 50 mVolt to 10 Volt or ± 25 mVolt to ± 10 Volt
- · User installable input filters
- · Analog inputs protected to ±32 Volt
- Single-width SBX Module



RBX 311 SBX Bus Analog Input Card

RBX 388 SBX Bus Analog I/O Card

- · 8 differential or 16 single-ended analog inputs
- · Eight analog outputs
- 12-bit bipolar or unipolar resolution
- Analog input ranges:
 100 mVolt to 10 Volt or ± 100 mVolt to ± 10 Volt
- Analog output ranges:
 0 to +5 Volt, 0 to + 10 Volt, -5 to +5 Volt,
 -10 to +10 Volt
- · On-board microprocessor
- Analog inputs protected to ±32 Volt
- · Optional continuous input scan mode
- Single-width SBX Module



RBX 388 SBX Bus Analog I/O Card

ROBOTROL CORPORATION

Phone (408) 683-2000



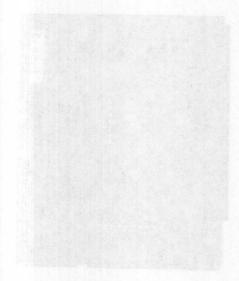
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SBX Bus Analog I/O Products

from Robotrel Corporation

RBX 311 SBX Bus Analog Input Card

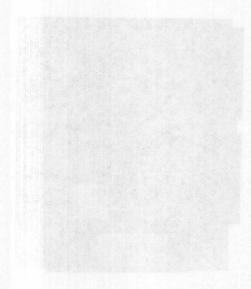
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Carrier Service Analog Property



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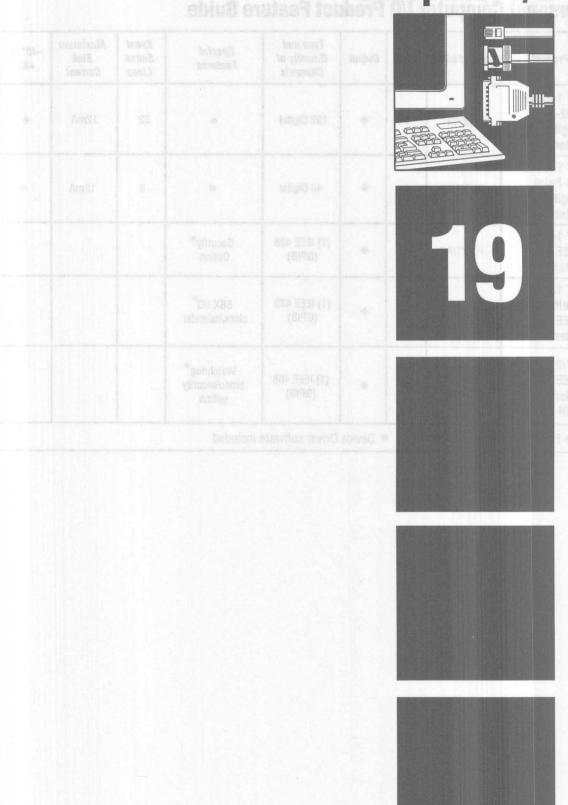


COMMISSION AND VICE SERVICE



ROBOT COL CORPORATION

Personal Computer I/O



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Personal Computer I/O Product Feature Guide

Product	Compatibility	Input	Output	Type and Quantity of Channels	Special Features	Event Sense Lines	Maximum Sink Current	-40° to +85°
ZT 14CT72 192-Point Digital I/O Interface	PC/XT/AT	•	•	192 Digital	•	32	12mA	٠
ZT 14CT73 48-Point Digital I/O Interface	PC/XT/AT	•	•	48 Digital	•	8	12mA	•
ZT 1444A IEEE 488 Interface	PC/XT/AT	٠	•	(1) IEEE 488 (GPIB)	Security Option			
ZT 1488A Multifunction IEEE 488 Interface	PC/XT/AT	•	•	(1) IEEE 488 (GPIB)	SBX I/0 [®] clock/calendar			
ZT/2 IEEE 488 Interface for IBM PS/2	Micro Channel	•	*	(1) IEEE 488 (GPIB)	Watchdog timer/security option			

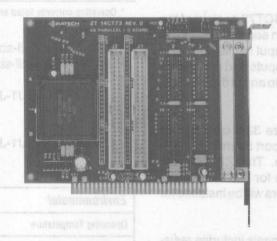
ZT 14CT72/14CT73

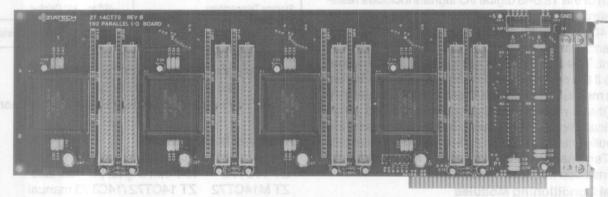
192-/48-Point Digital I/O Interface

Interfaces provide 192 and 48 digital lines for I/O-intensive ISA (PC/XT/AT®) Bus computer applications

Ziatech's ZT 14CT72 interface provides 192 points of bidirectional digital I/O to any computer that utilizes the Industry Standard Architecture (ISA), while the ZT 14CT73 provides 48 points. These interfaces allow computers to connect to instruments, peripherals, and standard optically isolated I/O modules such as those manufactured by Opto 22, Gordos, Crydom, Grayhill, Analog Devices, or equivalents.

These two boards feature low power consumption and an extended temperature operating range to provide exceptional reliability in harsh industrial and outdoor environments. They utilize CMOS components that are TTL backplane-compatible. The interfaces operate in temperatures ranging from -40° to +85° Celsius.





- Compatible with IBM PC/XT/AT and equivalent
- · Selectable I/O addressing
- 192/48 bidirectional digital I/O signals with termination
- 12mA sink current at V_{OL} of 0.4V
- · Write-protect mask register for output
- · Device driver software included

- Non-glitching power-up/power-down
- Thirty-two (14CT72) and eight (14CT73) event sense inputs for interrupts
- Low power/extended temperature operation (-40° to +85° C)
- · Compatible with Opto 22 or equivalent module

Note: CT denotes CMOS, TTL backplane-compatible, and extended temperature operation of -40° to +85° C. (Users should make adjustments for temperature rise in enclosures.)



Functional Considerations

Digital I/O Operation

The ZT 14CT72/14CT73 provide 192/48 digital I/O signals. Each signal is individually and easily programmable for input, output, or output with readback operation. The signals are provided through 50-pin latching connectors. Each connector is organized to provide 24 digital I/O signals with alternating grounds to improve noise immunity. Each connector also includes fused power (+5V at 1A) required by many industry standard I/O signal conditioning racks, such as Opto 22.

When programmed for output, inverting open collector, non-glitching operation is provided. Non-glitching outputs are desirable to prevent inadvertent I/O operation of a critical nature. Ziatech is careful to provide non-glitching outputs.

Event Sense Operation

Thirty-two I/O lines on the ZT 14CT72 or eight of the 48 I/O lines on the ZT 14CT73 can sense a positive or negative transition on the input. Input sense polarity is programmable in groups of four inputs and can generate an interrupt that is jumperable to any of the interrupt signals.

PC Bus Addressing

The ZT 14CT72/14CT73 require 32/8 consecutive I/O port addresses on a 32/8 I/O port boundary within the processor I/O address map. The ZT 14CT72/14CT73 is jumper-programmable for I/O address decoding. Default I/O address jumpers will be installed for ICO-IDF or ICO-IC7 hex.

Digital I/O Termination

Each of the 192/48 digital I/O signals includes resistive termination. The default configuration includes a 50k-140k ohm pull-up resistor within the ASIC. With this termination, each I/O signal can sink 12mA of current. This termination is adequate for most environments if the digital I/O cable length is less than 10 feet (three meters). If the digital I/O cable length exceeds 10 feet (three meters), or the cable is located in an electrically noisy environment, it may be necessary to add pull-up termination or pull-up/pull-down termination. Termination network locations are provided for user-installed termination networks.

Signal Conditioning Modules

The ZT14CT72/14CT73 allows direct control of 192/48 signal conditioning modules using the industry standard I/O module bus. Each bank also has its own fused, 1A 5-volt logic supply for the modules. These industrial modules control machinery for process control, automation, etc.

Software Support

The ZT 14CT72/14CT73 manual includes several examples of software routines used to drive the ZT 14CT72/14CT73. A linkable device driver for the ZT 14CT72/14CT73 is also included.

Specifications

Electrical

192/48 terminated bidirectional I/O lines

Output

- Inverting open collector operation
- · 100k ohm nominal pull-up resistor
- V_{OH} = 3V minimum at -4mA
- V_{OL} = 0.4V maximum at 12mA

Input

- Inverting input buffers
- · 100k ohm nominal pull-up resistor

Power Req.	Min.	Тур.	Max.
Supply Voltage, V _{CC}	4.75V	5.00V	5.25V
Supply Current, V _{CC} = 5.0V* (ZT 14CT72) (ZT 14CT73)	15mA 10mA	40mA 26mA	80mA 52mA

^{*} Operating currents listed are without output loading.

Mechanical

- ZT 14CT72: Full-size PC slot
- ZT 14CT73: Half-size PC slot
- Connectors

ZT 14CT72, J1-J8: 50-pin latching connec-

tors for parallel I/O, including fused +5V

ZT 14CT73, J1-J2: 50-pin latching connectors for parallel I/O,

tors for parallel I/O, including fused +5V

Environmental			
Operating Temperature	-40° to +85° Celsius		
Storage Temperature	-40° to +85° Celsius		
Non-Condensing Relative Humidity	less than 95% at 40° Celsius		

Reliability

- MTBF: 40 years (ZT 14CT72), 60 years (ZT 14CT73)
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 14CT72 192-Point Digital I/O Interface ZT 14CT73 48-Point Digital I/O Interface ZT M14CT72 ZT 14CT72 /14CT73 manual

Accessories

Cables (see Data Book cable section for details):

ZT 90021 10' (3m), flat card edge connector

ZT 90072 10' (3m), flat 50-pin both ends

Boards (see separate data sheet for more details): ZT 2224 24-Line Termination Assembly

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.



ZT 1444A/1488A

IEEE 488 Interfaces for Personal Computers

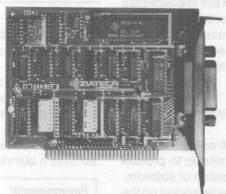
High-speed IEEE 488 controllers plus additional features for IBM PC and compatibles

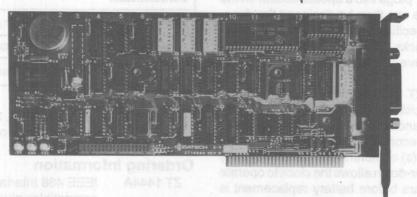
Ziatech's ZT 1444A IEEE 488 interface and ZT 1488A multifunction interface make it easy to integrate test and measurement systems. Over 4,000 IEEE 488-compatible instruments and devices interface with Ziatech's controllers through a patented backplate connector. Up to 15 devices can be attached to each port. Data transfer rates of up to 450 Kbytes/second are possible when used with DMA.

The ZT 1444A can occupy a short I/O slot and features an on-board, hardware-based security option. This option lets OEM product developers protect their software investment from unauthorized copying. The ZT 1488A does not offer the security option, but it

features two additional capabilities: a real-time clock/ calendar with battery backup, and an expansion module (SBX) socket for on-board I/O expansion. More than 100 SBX boards are available from various vendors, including four available from Ziatech. One of Ziatech's, the zSBX 20, provides a second, independent IEEE 488 port. The ZT 1488A occupies a full-sized I/O slot.

DOS and Windows device drivers are included with the purchase of both the ZT 1444A and the ZT 1488A interfaces. Several other driver options are also available. The manual includes detailed hardware descriptions to provide trouble-free implementation.





- Optional security key prevents unauthorized software duplication (ZT 1444A)
- EZ.488 and WIN.488 installable driver software included
- Complete IEEE 488 controller and talker/listener capability

- Data transfer speeds to 450 Kbytes/second with DMA
- Compatible with IBM PC/AT and equivalents
- Clock/calendar with two-year battery, expansion module (SBX) socket (ZT 1488A)
- Burned in at 55° C and tested to guarantee reliability



Functional Considerations

Two IEEE 488 Choices

The ZT 1444A and ZT 1488A are powerful IEEE 488 interfaces. The ZT 1488A gives the extra capabilities of a real-time clock/calendar and an SBX expansion socket. The ZT 1444A includes a socket for an optional security key. These two controllers are hardware- and software-compatible.

Complete GPIB Controller or Device

IEEE 488-compatible equipment is typically divided into two categories: controllers (masters) and talker/listeners (slaves). The ZT 1444A and ZT 1488A can operate in either mode. They each support all functions defined by the "IEEE Standard Digital Interface for Programmable Instrumentation." Functions include the capability to pass control as well as to respond to interrupts from devices. If interrupts are required, a language other than BASIC should be used because BASIC does not support this function.

The GPIB (General Purpose Interface Bus) functions on the ZT 1444A and ZT 1488A are implemented with the TMS9914A GPIB chip from Texas Instruments. This GPIB control chip has gained widespread popularity for use in IEEE 488 devices and controllers because of its straightforward operation, speed, and second-sourcing.

Software

DOS and Windows drivers are included with the purchase of a ZT 1444A/1488A.

Security Device Option (ZT 1444A only)

An optional security device is available to provide protection from unauthorized duplication of software. This electronic "key" plugs into a special socket on the ZT 1444A. Software can then be designed that functions only when a specific key is in place. When copied to a system that lacks a key, the software will not operate. This prevents unauthorized usage or duplication.

Real-time Clock (ZT 1488A only)

The real-time clock/calendar on the ZT 1488A provides time in thousandths of seconds, hundredths of seconds, tenths of seconds, seconds, minutes, hours, day(s) of week, day(s) of month, and months. Battery backup during power-down allows the clock to operate for at least two years before battery replacement is necessary.

SBX Expansion Socket (ZT 1488A only)

The ZT 1488A allows on-board I/O expansion through an expansion module (SBX) socket. The "piggy-back" arrangement enables the user to tailor the PC to a particular application. More than 100 different SBX I/O boards are available. The ZT 1488A supports DMA and interrupts for SBX boards with these features. Refer to Ziatech's SBX data sheets and reference list for additional information.

Specifications

Compatibility

- Compatible with IBM Personal Computer bus and equivalent
- IEEE 488.1 and IEEE 488.2-compatible
- SBX socket's electrical characteristics conform to SBX Expansion Module (MULTIMODULE®) Standard

Electrical

- Data Rate: 450 Kbytes per second (using DMA)
- Data Rate: 21 Kbytes per second (programmed IO)

Power Req.(ZT 1444A)	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, VCC = 5.0V	ad with D	340mA	700mA

Power Req.(ZT 1488A)	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	di rello re	550mA	1090mA

Mechanical

- ZT 1444A occupies one short I/O slot
- ZT 1488A occupies one long I/O slot
- · Connectors:

Socket for optional electronic security device (ZT 1444 only)

36-pin connector for SBX expansion module (ZT 1488A only)

Both interfaces incorporate a patented backplate that accepts a standard GPIB connector.

Environmental				
Operating Temperature	0° to +65° Celsius			
Storage Temperature	-40° to +85° Celsius			
Non-Condensing Relative Humidity	less than 90% at 40° Celsius			

Reliability

- MTBF: 55 years (ZT 1444A), 31 years (ZT 1488A)
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 1444A IEEE 488 Interface for IBM PC and compatibles plus EZ.488 and

WIN.488 IEEE 488 Device Drivers for Microsoft® MS-DOS® and

Windows™

ZT 1488A Multifunction IEEE 488 Interface for

IBM PC and compatibles plus EZ.488 and WIN.488 IEEE 488 Device Drivers for Microsoft® MS-DOS® and Windows™

ZT M1444A/1488A ZT 1444A /1488A manual

ZT 1444A/1488A IEEE 488 Interfaces for Personal Computers

Hardware Option

ZT 98010 Electronic Security Key (ZT 1444A only)

Software Options

ZT 97092M C.488 IEEE 488 Device Driver

Software

ZT 97094M OS2.488 IEEE 488 Device Driver

Software for Operating System/2®

Accessories

Cables (see cable section for details):

ZT 90008 13' (4m) round cable, with stackable

IEEE 488 connectors on both ends

ZT 90016 6.5' (2m) round cable, with stack-

able IEEE 488 connectors on both

ends

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.



ardware Coticn ZT 98010 Electronic Security Key CZT 1444A octy

offware Options
ZT 97092M C 468 IEEE 488 Device Driver
Software
ZT 97694M OS2,488 IEEE 468 Device Driver
Software for Operating System/2*

Spies (see dable section for details):

27 90008 13' (4m) round cable, with stackable
1EEE 486 connectors on both ands
27 90016 6.5' (2m) round cable, with stack
able IEEE 488 connectors on both
ends

All products are shipped FOB San Luis Oblago, OA, USA, OEM discounts are available for quantity purchases, Contact Zigtech for additional information.

Warranty — Five years with an optional five-year extension. See the full warranty statement in the *Technical* Data Book accensix.

IEEE 488 Interface for IBM Personal System/2

IEEE 488 interface makes the IBM® Personal System/2® a personal instrumentation workstation for test and measurement applications

Ziatech's ZT/2 IEEE 488 Interface brings IEEE 488 capability to IBM Personal System/2 computers that feature the Micro Channel bus.

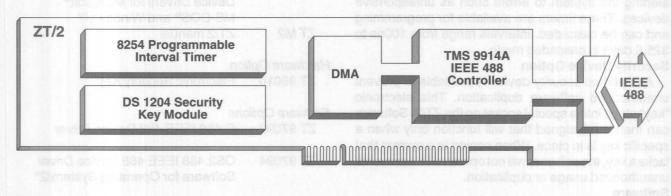
Each ZT/2 can connect to up to 15 IEEE 488-compatible devices for Micro Channel-based test and measurement applications. The interface can operate as either a controller or a talker/listener.

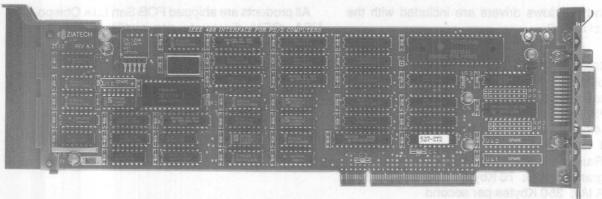
The Adapter Description File (ADF) on the ZT/2 eliminates the need for on-board jumpers and dipswitches for setting system configuration parameters.

This file lets users configure the interface through software at system start-up.

An on-board "private" interval timer can be used as a watchdog timer to prevent system hang-ups caused by unresponsive devices.

The ZT/2 also features an on-board hardware-based security option that lets OEM product developers protect their software investment from unauthorized duplication.





- EZ.488 and WIN.488 driver software included
- Complete IEEE 488 Controller and Talker/Listener capability
- Compatible with Micro Channel-based IBM Personal System/2 models
- Adapter Description File (ADF) for software interface configuration
- Data transfer rates to 350 Kbytes/second with DMA
- Watchdog timer
- Optional security key to prevent unauthorized software duplication
- Burned in at 55° C and tested to guarantee reliability

ZIATECH

Functional Considerations

Complete IEEE 488 Controller or Device

IEEE 488 (GPIB) compatible equipment is typically divided into two categories: controllers (masters) and talker/listeners (slaves). The ZT/2 can operate in either mode and supports all functions defined by the "IEEE Standard Digital Interface for Programmable Instrumentation." Functions include the capability to pass and to receive control. The IEEE 488 functions on the ZT/2 are implemented with the TMS9914A GPIB chip from Texas Instruments. This chip is widely used in IEEE 488 devices and controllers because of its straightforward operation, speed, and second-sourcing.

Interval Timer

An on-board "private" programmable interval timer lets users generate a periodic interrupt or set up event timing. Event timing can be used in a "watchdog timer" function, preventing potential system hang-ups by alerting the system to errors such as unresponsive devices. Three timers are available for programming and can be cascaded. Intervals range from 100ns to 325.8 days in cascaded mode.

Security Device Option

An optional security device is available to prevent unauthorized software duplication. This electronic "key" plugs into a special socket on the ZT/2. Software can then be designed that will function only when a specific key is in place. When copied to a system that lacks a key, the software will not operate. This prevents unauthorized usage or duplication.

Software

DOS and Windows drivers are included with the purchase of a ZT/2.

Specifications

Compatibility

- Compatible with Micro Channel-based (MCA) IBM PS/2 models
- IEEE 488.1 and IEEE 488.2-compatible

Electrical

• Data Rates:

Programmed I/O: 70 Kbytes per second DMA I/O: 350 Kbytes per second

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	are to the	940mA	1.5A

Mechanical

- · Occupies one MCA I/O slot
- Connectors

Socket for optional electronic security device J2: Female IEEE 488 connector

Environmental				
Operating Temperature	0° to +65° Celsius			
Storage Temperature	-20° to +100° Celsius			
Non-Condensing Relative Humidity	less than 90% at 40° Celsius			

Reliability

- MTBF: 29 years
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT/2 IEEE 488 Interface for IBM PS/2.

plus EZ.488 and WIN.488 IEEE 488

Device Drivers for Microsoft® MS-DOS® and Windows™

ZT M2 ZT/2 manual

Hardware Option

ZT 98010 Electronic Security Key

Software Options

ZT 97092 C.488 IEEE 488 Device Driver

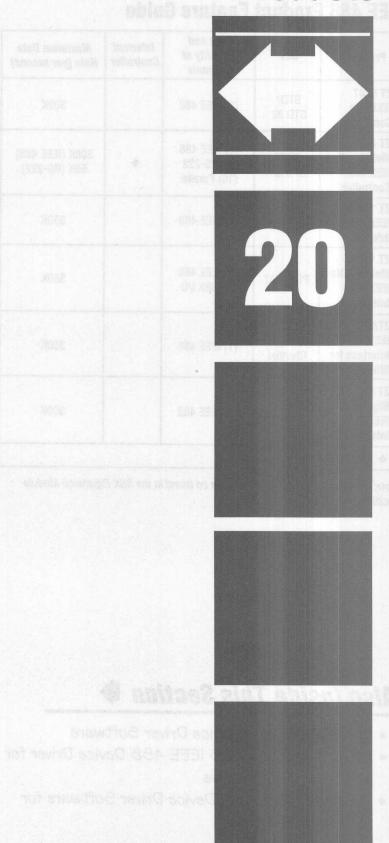
ZT 97094 OS2.488 IEEE 488 Device Driver Software for Operating System/2®

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.



IEEE 488 Products



IEEE 488 Product Feature Guide

Product	Bus	Type and Quantity of Channels	Interrupt Controller	Maximum Data Rate (per second)
ZT 8847 IEEE 488 Controller	STD/ STD 32	(1) IEEE 488		300K
ZT 8848 Multifunction IEEE 488 Controller	STD/ STD 32	(1) IEEE 488 (1) RS-232 (16) Parallel	•	300K (IEEE 488) 56K (RS-232)
ZT 1444A IEEE 488 Interface	PC/XT/AT	(1) IEEE 488		350K
ZT 1488A Multifunction IEEE 488 Interface	PC/XT/AT	(1) IEEE 488 (1) SBX I/O		350K
ZT/2 IEEE 488 Interface for IBM PS/2	Micro Channel	(1) IEEE 488		350K
ZT 87A High-speed IEEE 488 Interface	MULTIBUS	(1) IEEE 488		300K

Note: Additional IEEE 488 products can be found in the SBX Expansion Module section of this data book.

Also Inside This Section



- C.488 IEEE 488 Device Driver Software
- EZ.488 and WIN.488 IEEE 488 Device Driver for MS-DOS and Windows
- 052.488 IEEE 488 Device Driver Software for Operating System/2

ZT 8847/8848

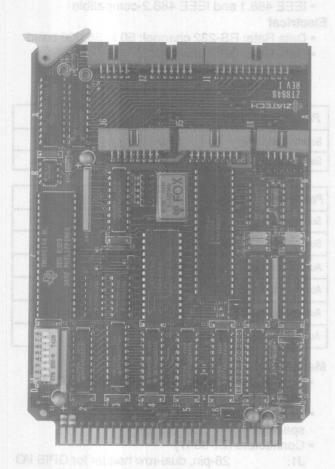
Multifunction IEEE 488 Interfaces

IEEE 488 interface and general purpose I/O functions for use with STD Bus systems

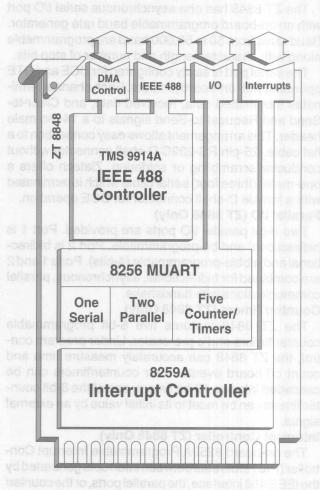
The ZT 8847/8848 Interfaces provide IEEE 488 capabilities for STD Bus systems. These products are intended for use in STD test and measurement system controllers or STD-based IEEE 488 devices. The IEEE 488 controller on the ZT 8847/8848 allows up to 15 of the over 4,000 compatible devices to be interfaced through one STD I/O slot. The off-board DMA capability of the ZT 8847/8848 allows data transfer speeds of over 300 Kbytes-per-second. External DMA

controllers can be used with non-DMA-equipped 80x86 processor boards. Several software driver options are available for the ZT 8847/8848.

The ZT 8848 provides additional I/O and vectored interrupt control with the on-board interrupt controller (8259) and MUART (8256). Separate connectors are provided for each function to simplify system cabling and debugging.



- Complete IEEE 488 controller capability
- DMA-compatible: 300 Kbytes/second
- IEEE 488 slave mode for use in IEEE 488 talker/ listener devices
- ZT 8848 supports 5 and 8 MHz operation
- Interrupt Controller (8259) (ZT 8848)



- Serial port for RS-232C (ZT 8848)
- Two 8-bit parallel I/O ports (ZT 8848)
- Several GPIB drivers available on diskette
 - Burned in at 55° C and tested to quarantee reliability

interrigits. Foul of these interrupts



Functional Considerations

Complete IEEE 488 Controller or Device I/O

Devices with IEEE 488 (GPIB) interfaces are typically divided into two categories: controllers (masters) and talker/listeners (slaves). The ZT 8847/8848 can operate in either mode. Both boards support all functions defined by the "IEEE Standard Digital Interface for Programmable Instrumentation." Functions include the capability to pass control and respond to interrupts from devices.

The GPIB functions are implemented with the TMS9914A GPIB chip. This chip is widely used in IEEE 488 devices and controllers because of its straightforward operation, speed, and the availability of second-sourcing.

Serial I/O (ZT 8848 Only)

The ZT 8848 has one asynchronous serial I/O port with an on-board programmable baud rate generator. Baud rates from 50 to 56,000 baud are programmable along with character length and number of stop bits.

The serial port is easily configured for DCE and DTE operation with on-board jumpers. Each channel terminates transmitted data, received data, and Clear-to-Send and Request-to-Send signals to a 14-pin male header. This arrangement allows easy connection to a flat cable, 25-pin RS-232C D-shell connector without conductor scrambling or soldering. Ziatech offers a one-meter (three foot) serial cable which is terminated with a female D-shell connector for DCE operation.

Parallel I/O (ZT 8848 Only)

Two 8-bit parallel I/O ports are provided. Port 1 is bidirectional and bit-programmable. Port 2 is bidirectional and nibble-programmable (4-bits). Ports 1 and 2 are combined for bidirectional, asynchronous, parallel communications with handshake.

Counter/Timers (ZT 8848 Only)

The ZT 8848 features five 8-bit programmable counter/timers and a pre-scaler. Under program control, the ZT 8848 can accurately measure time and count off-board events. Four counter/timers can be cascaded into two 16-bit timers; one of the 8-bit counter/timers can be reset to its initial value by an external signal.

Interrupt Controller (ZT 8848 Only)

The on-board 8259A Programmable Interrupt Controller (PIC) arbitrates between interrupts generated by the IEEE 488 interface, the parallel ports, or the counter/ timers on the ZT 8848. The PIC may be configured either to act as a single buffered master to expand the number of interrupt levels from eight to 36, or as a slave to another master interrupt controller.

When operating in the master mode, the 8259A can support up to 36 interrupts. Four of these interrupts are generated on-board while the remaining interrupts are generated by four off-board 8259A slave interrupt

controllers. The slave interrupt controllers request service over the frontplane via an 8-pin right-angle connector located at the top of the board. The cascade address is output on address bus lines A8 to A10 to select the appropriate slave interrupt controller.

When operating as a slave, the 8259A cascade address is supplied to the ZT 8848 interrupt controller over STD Bus address lines A8 to A10 as defined in the STD-80 Specification.

Software

All of Ziatech's IEEE 488 software options, including the popular DOS and Windows drivers, are fully compatible with the ZT 8847/8848.

Specifications

Compatibility

- EIA RS-232C drivers for serial communication
- IEEE 488.1 and IEEE 488.2-compatible

Electrical

- Data Rate: RS-232 channel: 50 to 56,000 baud
- Data Rate: GPIB channel 30 Kbytes-per-second using programmed I/O 300 Kbytes-per-second using DMA

Power Req.(ZT 8847)	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	-	400mA	700mA

Power Req. (ZT 8848)	Min.	Тур.	Max.
Supply Voltage, V _{CC}	4.75V	5.00V	5.25V
Supply Current, VCC = 5.0V		800mA	1.60A
Aux Voltage, V _{aux+}	10.8V	12.0V	13.2V
Aux Current, Vaux+ = 12.0V		20mA	35mA
Aux Voltage, V _{aux} -	-10.8V	-12.0V	-13.2V
Aux Current, Vaux- = -12.0V		20mA	35mA

Mechanical

- Size- and backplane-compatible with STD 32 and STD-80 mechanical specifications
- Occupies one STD slot (0.625" [1.6026cm] spacing)
- Connectors (ZT 8847)

J1: 26-pin, dual-row header for GPIB I/O J2, J3: 10-pin, dual-row header for DMA and interrupts

Connectors (ZT 8848)

J1: 26-pin, dual-row header for GPIB I/O J2: 14-pin dual-row header for serial I/O J3, J4: 10-pin dual-row header for interrupts

and DMA

J5, J6: 16-pin dual-row header for parallel I/O

Environmental	
Operating Temperature	0° to +55° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 90% at 40° Celsius

STD 32 Compliance Level (ZT 8847)

• I/O Slave: SA8-I, SDMA8

STD 32 Compliance Level (ZT 8848)

• I/O Slave: SA8-I, ICA, SDMA8

Note: SA8 is equivalent to STD-80 Series Rev. 2.3

(5 and 8 MHz)

Reliability

• MTBF: 80 years (ZT 8847), 46 years (ZT 8848)

• MTTR: five minutes (based on board replacement)

Ordering Information

ZT 8847 IEEE 488 Interface with ZT 90010 cable

ZT M8847 ZT 8847 manual

ZT 8848 Multifunction IEEE 488 Interface with

ZT 90010 cable

ZT M8848 ZT 8848 manual

Software Options

ZT 97044 EZ.488 and WIN.488 IEEE 488

Device Drivers for Microsoft® MS-DOS® and Windows®

ZT 97092 C.488 IEEE 488 Device

Driver Software

ZT 97094 OS2.488 IEEE 488 Device Driver

Software for Operating System/2®

Accessories

Cables (see cable section for details):

ZT 90002 40" (1m) round, 26-pin to female

IEEE 488 connector

ZT 90003 40" (1m) flat, 26-pin to female

IEEE 488 connector

ZT 90005 82" (2m) round, 26-pin to stackable

IEEE 488 connector

ZT 90014 40" (1m) flat, 14-pin to 25-pin female

D-shell connector (for ZT 8848 only)

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.





ZT 1444A/1488A

IEEE 488 Interfaces for Personal Computers

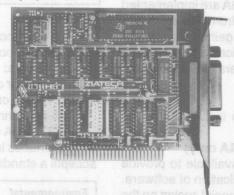
High-speed IEEE 488 controllers plus additional features for IBM PC and compatibles

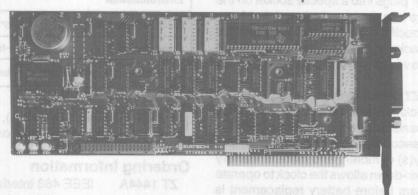
Ziatech's ZT 1444A IEEE 488 interface and ZT 1488A multifunction interface make it easy to integrate test and measurement systems. Over 4,000 IEEE 488-compatible instruments and devices interface with Ziatech's controllers through a patented backplate connector. Up to 15 devices can be attached to each port. Data transfer rates of up to 450 Kbytes/second are possible when used with DMA.

The ZT 1444A can occupy a short I/O slot and features an on-board, hardware-based security option. This option lets OEM product developers protect their software investment from unauthorized copying. The ZT 1488A does not offer the security option, but it

features two additional capabilities: a real-time clock/calendar with battery backup, and an expansion module (SBX) socket for on-board I/O expansion. More than 100 SBX boards are available from various vendors, including four available from Ziatech. One of Ziatech's, the zSBX 20, provides a second, independent IEEE 488 port. The ZT 1488A occupies a full-sized I/O slot.

DOS and Windows device drivers are included with the purchase of both the ZT 1444A and the ZT 1488A interfaces. Several other driver options are also available. The manual includes detailed hardware descriptions to provide trouble-free implementation.





- Optional security key prevents unauthorized software duplication (ZT 1444A)
- EZ.488 and WIN.488 installable driver software included
- Complete IEEE 488 controller and talker/listener capability

- Data transfer speeds to 450 Kbytes/second with DMA
- Compatible with IBM PC/AT and equivalents
- Clock/calendar with two-year battery, expansion module (SBX) socket (ZT 1488A)
- Burned in at 55° C and tested to guarantee reliability



Functional Considerations

Two IEEE 488 Choices

The ZT 1444A and ZT 1488A are powerful IEEE 488 interfaces. The ZT 1488A gives the extra capabilities of a real-time clock/calendar and an SBX expansion socket. The ZT 1444A includes a socket for an optional security key. These two controllers are hardware- and software-compatible.

Complete GPIB Controller or Device

IEEE 488-compatible equipment is typically divided into two categories: controllers (masters) and talker/listeners (slaves). The ZT 1444A and ZT 1488A can operate in either mode. They each support all functions defined by the "IEEE Standard Digital Interface for Programmable Instrumentation." Functions include the capability to pass control as well as to respond to interrupts from devices. If interrupts are required, a language other than BASIC should be used because BASIC does not support this function.

The GPIB (General Purpose Interface Bus) functions on the ZT 1444A and ZT 1488A are implemented with the TMS9914A GPIB chip from Texas Instruments. This GPIB control chip has gained widespread popularity for use in IEEE 488 devices and controllers because of its straightforward operation, speed, and second-sourcing.

Software

DOS and Windows drivers are included with the purchase of a ZT 1444A/1488A.

Security Device Option (ZT 1444A only)

An optional security device is available to provide protection from unauthorized duplication of software. This electronic "key" plugs into a special socket on the ZT 1444A. Software can then be designed that functions only when a specific key is in place. When copied to a system that lacks a key, the software will not operate. This prevents unauthorized usage or duplication.

Real-time Clock (ZT 1488A only)

The real-time clock/calendar on the ZT 1488A provides time in thousandths of seconds, hundredths of seconds, tenths of seconds, seconds, minutes, hours, day(s) of week, day(s) of month, and months. Battery backup during power-down allows the clock to operate for at least two years before battery replacement is necessary.

SBX Expansion Socket (ZT 1488A only)

The ZT 1488A allows on-board I/O expansion through an expansion module (SBX) socket. The "piggy-back" arrangement enables the user to tailor the PC to a particular application. More than 100 different SBX I/O boards are available. The ZT 1488A supports DMA and interrupts for SBX boards with these features. Refer to Ziatech's SBX data sheets and reference list for additional information.

Specifications

Compatibility

- Compatible with IBM Personal Computer bus and equivalent
- IEEE 488.1 and IEEE 488.2-compatible
- SBX socket's electrical characteristics conform to SBX Expansion Module (MULTIMODULE®) Standard

Electrical

- Data Rate: 450 Kbytes per second (using DMA)
- Data Rate: 21 Kbytes per second (programmed IO)

Power Req.(ZT 1444A)	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	l rilliuv bes	340mA	700mA

Power Req.(ZT 1488A)	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V	thresho to	550mA	1090mA

Mechanical

- ZT 1444A occupies one short I/O slot
- ZT 1488A occupies one long I/O slot
- · Connectors:

Socket for optional electronic security device (ZT 1444 only)

36-pin connector for SBX expansion module (ZT 1488A only)

Both interfaces incorporate a patented backplate that accepts a standard GPIB connector.

Environmental	
Operating Temperature	0° to +65° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 90% at 40° Celsius

Reliability

- MTBF: 55 years (ZT 1444A), 31 years (ZT 1488A)
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 1444A IEEE 488 Interface for IBM PC and compatibles plus EZ.488 and WIN.488 IEEE 488 Device Drivers

for Microsoft® MS-DOS® and Windows™

ZT 1488A Multifunction IEEE 488 Interface for

IBM PC and compatibles plus EZ.488 and WIN.488 IEEE 488 Device Drivers for Microsoft® MS-DOS® and Windows™

ZT M1444A/1488A ZT 1444A /1488A manual

ZT 1444A/1488A IEEE 488 Interfaces for Personal Computers

Hardware Option

ZT 98010 Electronic Security Key

(ZT 1444A only)

Software Options

ZT 97092M C.488 IEEE 488 Device Driver

Software

ZT 97094M OS2.488 IEEE 488 Device Driver

Software for Operating System/2®

Accessories

Cables (see cable section for details):

ZT 90008 13' (4m) round cable, with stackable

IEEE 488 connectors on both ends

ZT 90016 6.5' (2m) round cable, with stack-

able IEEE 488 connectors on both

ends

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.



IEEE 488 Interface for IBM Personal System/2

IEEE 488 interface makes the IBM® Personal System/2® a personal instrumentation workstation for test and measurement applications

Ziatech's ZT/2 IEEE 488 Interface brings IEEE 488 capability to IBM Personal System/2 computers that feature the Micro Channel bus.

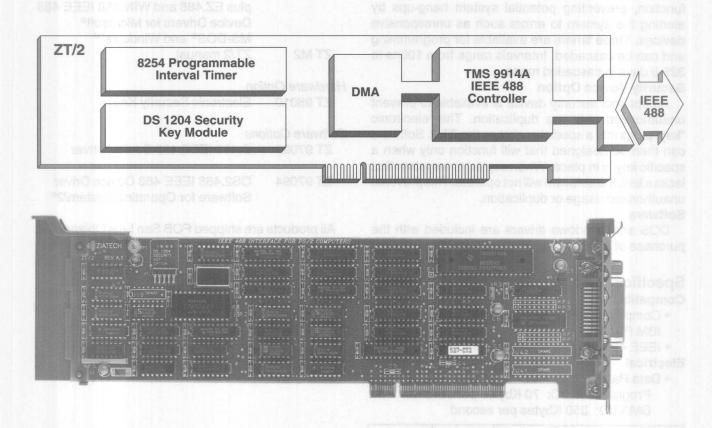
Each ZT/2 can connect to up to 15 IEEE 488-compatible devices for Micro Channel-based test and measurement applications. The interface can operate as either a controller or a talker/listener.

The Adapter Description File (ADF) on the ZT/2 eliminates the need for on-board jumpers and dipswitches for setting system configuration parameters.

This file lets users configure the interface through software at system start-up.

An on-board "private" interval timer can be used as a watchdog timer to prevent system hang-ups caused by unresponsive devices.

The ZT/2 also features an on-board hardware-based security option that lets OEM product developers protect their software investment from unauthorized duplication.



- EZ.488 and WIN.488 driver software included
- Complete IEEE 488 Controller and Talker/Listener capability
- Compatible with Micro Channel-based IBM Personal System/2 models
- Adapter Description File (ADF) for software interface configuration
- Data transfer rates to 350 Kbytes/second with DMA
- Watchdog timer
- Optional security key to prevent unauthorized software duplication
- Burned in at 55° C and tested to guarantee reliability



Functional Considerations

Complete IEEE 488 Controller or Device

IEEE 488 (GPIB) compatible equipment is typically divided into two categories: controllers (masters) and talker/listeners (slaves). The ZT/2 can operate in either mode and supports all functions defined by the "IEEE Standard Digital Interface for Programmable Instrumentation." Functions include the capability to pass and to receive control. The IEEE 488 functions on the ZT/2 are implemented with the TMS9914A GPIB chip from Texas Instruments. This chip is widely used in IEEE 488 devices and controllers because of its straightforward operation, speed, and second-sourcing.

Interval Timer

An on-board "private" programmable interval timer lets users generate a periodic interrupt or set up event timing. Event timing can be used in a "watchdog timer" function, preventing potential system hang-ups by alerting the system to errors such as unresponsive devices. Three timers are available for programming and can be cascaded. Intervals range from 100ns to 325.8 days in cascaded mode.

Security Device Option

An optional security device is available to prevent unauthorized software duplication. This electronic "key" plugs into a special socket on the ZT/2. Software can then be designed that will function only when a specific key is in place. When copied to a system that lacks a key, the software will not operate. This prevents unauthorized usage or duplication.

Software

DOS and Windows drivers are included with the purchase of a ZT/2.

Specifications

Compatibility

- Compatible with Micro Channel-based (MCA) IBM PS/2 models
- IEEE 488.1 and IEEE 488.2-compatible

Electrical

Data Rates:

Programmed I/O: 70 Kbytes per second DMA I/O: 350 Kbytes per second

Power Req.	Min.	Тур.	Max.
Supply Voltage, Vcc	4.75V	5.00V	5.25V
Supply Current, Vcc = 5.0V		940mA	1.5A

Mechanical

- · Occupies one MCA I/O slot
- Connectors
 Socket for optional electronic security device
 J2: Female IEEE 488 connector

Environmental	
Operating Temperature	0° to +65° Celsius
Storage Temperature	-20° to +100° Celsius
Non-Condensing Relative Humidity	less than 90% at 40° Celsius

Reliability

- MTBF: 29 years
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT/2 IEEE 488 Interface for IBM PS/2,

plus EZ.488 and WIN.488 IEEE 488

Device Drivers for Microsoft® MS-DOS® and Windows™

ZT M2 ZT/2 manual

Hardware Option

ZT 98010 Electronic Security Key

Software Options

ZT 97092 C.488 IEEE 488 Device Driver

ZT 97094 OS2.488 IEEE 488 Device Driver

Software for Operating System/2®

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.



ZT 87A

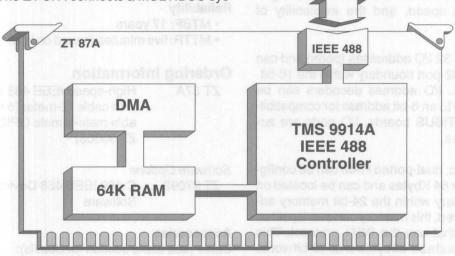
High-Speed IEEE 488 Interface

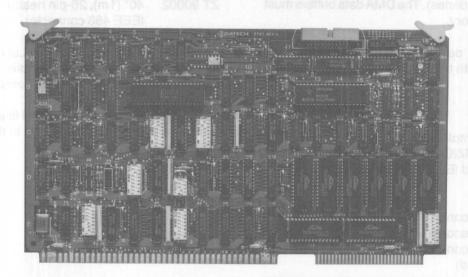
IEEE 488 Interface for use with MULTIBUS™ I systems

The ZT 87A brings all the benefits of the IEEE 488 General Purpose Interface Bus (GPIB) to single board computers or MULTIBUS systems. The multidrop feature of GPIB I/O can cut MULTIBUS system costs dramatically. The ZT 87A connects a MULTIBUS sys-

tem to up to 15 of the more than 4,000 IEEE 488-compatible instruments, peripherals, and computers.

A GPIB local network can consist of a mix of GPIB-compatible computers, instruments, and peripherals.





- Complete IEEE 488 controller, talker, and listener capability
- MULTIBUS-compatible
- High-speed data rate (300 Kbytes/second) with on-board DMA
- · Several GPIB drivers available
- · 64 Kbytes size-configurable dual-ported RAM
- Burned in at 55° C and tested to guarantee reliability



Functional Considerations

Complete IEEE 488 Controller Device I/O

Devices with IEEE 488 interfaces are typically divided into two categories: controllers (masters) and talker/listeners (slaves). The ZT 87A can operate in either mode. It supports all functions defined by the "IEEE Standard Digital Interface for Programmable Instrumentation." Functions include the capability to pass control and to respond to interrupts from devices.

The GPIB functions are implemented with the TMS9914A GPIB chip. This chip is widely used in IEEE 488 devices and controllers because of its straightforward operation, speed, and the availability of second-sourcing.

Input/Output

The ZT 87A uses 32 I/O addresses (ports) and can be located on any 32-port boundary within the 16-bit I/O address space. I/O address decoders can be optionally restricted to an 8-bit address for compatibility with older MULTIBUS boards. I/O ports are accessed only as bytes.

Memory

64 Kbytes of static, dual-ported RAM can be configured as 8, 16, 32, or 64 Kbytes and can be located on any 8 Kbyte boundary within the 24-bit memory address space. If desired, this memory can overlap other system memories that use the INH1 protocol. This RAM may be accessed as 8-bit bytes or as 16-bit words (on even byte boundaries). The DMA data buffers must reside in this memory.

Software

Ziatech's C.488 device driver package is recommended for use with the ZT 87A.

Specifications

Compatibility

- MULTIBUS compliance: Slave D16 M24/20/16 I16 V0
- IEEE 488.1 and IEEE 488.2-compatible

Electrical

· Data Rate:

30 Kbytes/second - Programmed I/O

300 Kbytes/second - DMA

20 Kbytes/second - Command rate

(ATN asserted)

Power Req.	Min.	Тур.	Max.	
Supply Voltage, Vcc	4.75V	5.00V	5.25V	
Supply Current, Vcc = 5.0V	idanugilna	2.0A	3.2A	

Mechanical

- Size- and backplane-compatible with MULTIBUS mechanical specifications
- Connectors

J1: 24-pin header connector

Environmental	
Operating Temperature	0° to 65° Celsius
Storage Temperature	-40° to +85° Celsius
Non-Condensing Relative Humidity	less than 90% at 40° Celsius

Reliability

- MTBF: 17 years
- MTTR: five minutes (based on board replacement)

Ordering Information

ZT 87A High-speed IEEE 488 Interface

with cable (2-meter [6.6 feet], stackable male-female GPIB connector,

ZT 90005)

Software Options

ZT 97092 C.488 IEEE 488 Device Driver

Software

Accessories

Cable (see cable section for details):

ZT 90002 40" (1m), 26-pin header to female

IEEE 488 connector

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

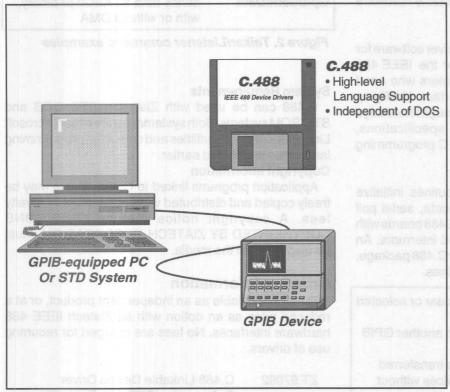
Warranty – Five years with an optional five-year extension. See the full warranty statement in the *Technical Data Book* appendix.





C.488

IEEE 488 Device Driver Software



Device Driver Software for IEEE 488 Controllers and Talker/Listeners

Ziatech offers high-level, language linkable software support for both IEEE 488 controllers and talker/ listeners. The C.488 software package provides extremely efficient code for accessing the IEEE 488 bus in a friendly development environment. C.488 saves time because it doesn't access DOS or the BIOS and therefore doesn't compromise IEEE 488 operation, making it the perfect choice for embedded applications. In addition, C.488 saves memory because only the actual routines used are placed into the final program.

C.488

C.488 includes DOS- and BIOS-independent C source and object code for Ziatech's linkable IEEE 488 drivers. The source code can be compiled from either Microsoft C or Borland C/C++, while the object modules can

be linked from most popular languages.

C.488 includes the source code for Ziatech's linkable IEEE 488 drivers. The source code is IEEE 488.2 compliant C code for developers who wish to customize their IEEE 488 interfaces. Ziatech's linkable driver for IEEE 488 is written in Ziatech's standard Device Driver Protocol. This protocol is used for all device drivers in Ziatech's STD Device Driver Package (STD DDP) and is completely independent of any DOS or BIOS functions. This independence allows the developer to easily develop code for non-DOS target systems. The C.488 package also contains linkable libraries for developers who do not need to modify source code, or who are not using C but still wish to link to Ziatech's IEEE 488 drivers.

Linkable GPIB Software Support

- IEEE 488.2 Operation
- C Source Code
 Included
- Support for Controller or Talker/Listener
 Operation
- DOS- and BIOS-Independent
- Synchronous or Asynchronous DMA Support
- Interrupt or Polled Operation
- No Recurring License Fees



Ziatech provides an interactive test program with the C.488 software package. This program lets programmers fully test the capabilities of their device through screen oriented commands. The interactive test program tests any device or controller function in the IEEE 488.2 interface standard, and helps ensure a stable hardware environment for program development.

C Source Code

Ziatech strongly recommends using driver software for system development. Source code for the IEEE 488 linkable package is provided for customers who need maximum control over the IEEE 488 interface. Modifying the source code of C.488 requires a thorough knowledge of the IEEE 488.1 and IEEE 488.2 specifications, Ziatech's IEEE 488 interfaces, and the C programming language.

Controller Operation

The controller software driver subroutines initialize IEEE 488 devices, send and receive data, serial poll IEEE 488 devices, support multiple IEEE 488 boards with the same driver, and support DMA and interrupts. An IEEE 488 test routine is included with the C.488 package, for testing any of the IEEE 488 subroutines.

GpibDevClr	 sends a device clear or selected device clear 	ted
GpibPassControl	 passes control to another GP controller 	IB
GpibTransfer	 allows data to be transferred between two devices without controller intervention 	
GpibSerPoll	 serial polls the device list instruments 	
GpibSrqStatus	- returns status of SRQ line on IEEE 488 bus	

Figure 1. Frequently used controller software commands

Device Operation

Ziatech's IEEE 488 software for talker/listener devices allows any Ziatech IEEE 488 interface to act as a device on the bus. The driver subroutines support the same types of functions as the controller software, including DMA and interrupt capability.

These talker/listener subroutines respond to the need for high-speed communications between multiple computers functioning as instruments. To allow computers to act as talker/listeners, Ziatech has taken certain considerations into account. For example, software routines are included that provide interrupt support. See Figure 2.

GpibDmaStatus	checks for successful completion of DMA, or for error codes
GpibRecvData	- receives data from instruments
GpibSendData	on the bus, with or without DMA - sends data as ASCII or binary, with or without DMA

Figure 2. Talker/Listener command examples

System Requirements

C.488 can be used with Ziatech's STD DOS and STD ROM systems. Both systems require either Microsoft Link or Borland Tlink utilities and one of the programming languages mentioned earlier.

Copyright Information

Application programs linked to C.488 drivers may be freely copied and distributed without payment of royalty fees. A copyright notice reading "PORTIONS COPYRIGHTED BY ZIATECH CORPORATION" must be displayed on the media.

Ordering Information

C.488 is available as an independent product, or at a reduced price as an option with all Ziatech IEEE 488 hardware interfaces. No fees are charged for recurring use of drivers.

ZT 97092 C.488 Linkable Device Driver Software for IEEE 488 Controllers and Talker/Listeners. (3.5" diskette)

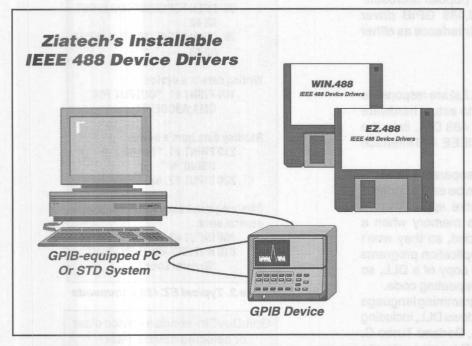
All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.





EZ.488 and WIN.488

IEEE 488 Device Drivers for Microsoft® MS-DOS® and Windows™



Installable drivers speed the integration of IEEE 488 interfaces

Ziatech's EZ.488 package contains drivers for Microsoft MS-DOS and Windows. The DOS portion of the package contains a DOS installable driver, while the Windows portion of the EZ.488 package contains a Windows Dynamic Link Library (DLL).

EZ.488 is Ziatech's DOS installable driver. EZ.488 allows IEEE 488 interfaces to be configured as controllers or talker/listeners.

Application examples accompany the EZ.488 driver disk and reference manuals. The disk contains an installation module which automatically installs the device driver into the system. From then on, the driver is loaded into the operating system automatically every time the system is booted up. A menu driven test program tests the functionality of IEEE 488 systems prior to application code development as well as any device or controller function available to the IEEE 488 standard.

EZ.488 - Easy to Use

EZ.488 is included with the purchase of Ziatech's IEEE 488 interfaces for personal computers. It has a simple, clear interface with HP 85-compatible syntax and the ability to access IEEE 488 devices from most high-level languages. For example, BASIC PRINT# and INPUT# commands can be used to access most functions available on the IEEE 488 interface. Figure 1 lists the commands most often used. Figure 2 illustrates simplified examples of typical EZ.488 commands.

The EZ.488 driver is the best choice for applications requiring a driver that is accessible from any language. A typical example is the instrument manufacturer that buys an IEEE 488 interface from Ziatech to sell it, along with their instrument, to an end user. Since the interface is designed to support many different types of instruments made by the manufacturer,

- •Support for Controller or Talker/ Listener Operation
- No Recurring License Fees
- •IEEE 488.2 Compatibility for Windows Drivers
- •Interactive Test Programs for DOS and Windows

ABORTIO **CLEAR** CONTROL **ENTER GET ERROR** HALT LOCAL **LOCAL LOCKOUT** OUTPUT **PASS CONTROL** PPOLL REMOTE REQUEST RESET RESUME SEND **SET TIMEOUT** SPOLL STATUS TRIGGER

Figure 1. EZ.488 command summary



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and will be utilized by instrument purchasers for a variety of applications, it should be supported by a flexible, easy-to-use software driver such as EZ.488.

WIN.488

WIN.488 supports the increasingly popular Microsoft® Windows™ environment. The WIN.488 GPIB driver package supports Ziatech IEEE 488 interfaces as either controllers or talker/listeners.

Dynamic Link Library

Windows Dynamic Link Libraries (DLLs) are responsible for interfacing application programs to actual hardware interfaces. WIN.488, Ziatech's IEEE 488 DLL, links the user's program to the actual Ziatech IEEE 488 interface board.

Dynamic Link Libraries are loaded separately from the main application program, so they can be easily updated without having to recompile the entire application. In addition, DLLs are only loaded into memory when a program that needs the DLL is loaded, so they won't waste memory or time at startup. Application programs under Windows can also share one copy of a DLL, so there is no need to waste space by repeating code.

WIN.488 can be used with any programming language or environment that can access a Windows DLL, including Borland Turbo Pascal, Borland C++, Borland Turbo C, Microsoft C, or Microsoft Visual BASIC (some packages may require Microsoft's Software Development Kit, SDK). WIN.488 supports re-entry for Windows programs, allowing multiple programs to access the DLL under one Windows session. WIN.488 supports Microsoft Windows version 3.0 and above.

GPIBTEST

The WIN.488 package contains GPIBTEST, an interactive Windows-based test program. GPIBTEST allows the user to interactively use the Windows DLL with a Ziatech IEEE 488 interface board. GPIBTEST can support Ziatech IEEE 488 cards as controllers or talker/listeners, with full support for command and data transmission and receipt.

Ordering Information

ZT 97044 EZ.488 a

EZ.488 and WIN.488 IEEE 488
Device Drivers for Microsoft®
MS-DOS® and Windows™

All products are shipped FOB San Luis Obispo, CA, USA. OEM discounts are available for quantity purchases. Contact Ziatech for additional information.

Establishing communications between driver and IEEE 488

10 OPEN "GPIBOUTO" FOR OUTPUT AS #1

20 OPEN "GPIBINO" FOR INPUT AS #2

30 OPEN "GPIBSTO" FOR INPUT AS #3

Writing data to a device 100 PRINT #1, "OUTPUT 704 DMA;ABCDEFG"

Reading data from a device 210 PRINT #1, "ENTER 710 USING'%'" 220 INPUT #2, B\$

Obtaining quick status, checking for general error 800 INPUT #3, ERR% 810 IF (ERR%<0) THEN PRINT "General Error."

Figure 2. Typical EZ.488 commands

GpibDevClr-sends a device clear or selected device clear.

GpibPassControl - passes control to another GPIB controller.

GpibTransfer - allows data to be transferred between two devices without controller intervention.

GpibSerPoll-serial polls the device list instruments.

GpibSrqStatus - return status or SRQ line on IEEE 488 bus.

Figure 3. Controller Command Examples (WIN.488)

GpibDmaStatus - check for successful completion of DMA, or for error codes.

GpibRecvData - receive data from instruments on the bus, with or without GPIB address.

GpibSendData - send data as ASCII or binary, with or without DMA.

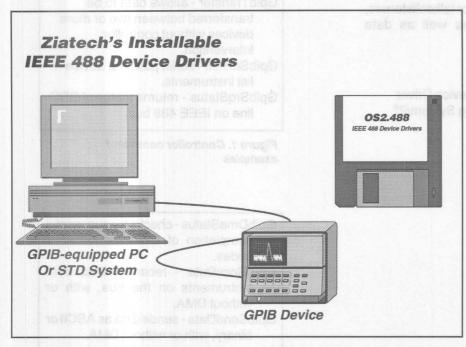
Figure 4. Talker/Listener Command Examples (WIN.488)





OS2.488

IEEE 488 Device Driver Software for Operating System/2®



- IEEE 488.2 Operation
- Controller or Talker/ Listener Operation
- Interactive Test Program
- No Recurring License Fees

Linkable Device Driver for IEEE 488 Controllers and Talker/ Listeners

OS2.488 supports the IBM® OS/2® Operating System. The OS2.488 GPIB driver package supports Ziatech IEEE 488 interfaces as either controllers or talker/listeners.

Dynamic Link Library

OS/2 Dynamic Link Libraries (DLLs) interface application programs to actual hardware interfaces. Ziatech's OS2.488 DLL links the user's program to the actual Ziatech IEEE 488 interface board.

Dynamic Link Libraries are loaded separately from the main application program, so they can be easily updated without having to recompile the entire application. OS/2 DLLs are loaded into memory only when a program that needs the DLL is loaded. This saves memory and time at system startup. Application programs under OS/2 can share one copy of a DLL, so memory resources aren't wasted by repeating code.

OS2.488

OS2.488 contains an IEEE 488.2-compatible OS/2 DLL for driving Ziatech GPIB cards. OS2.488 can be used with any programming language or environment that can access an OS/2 DLL. OS2.488 supports re-entry for OS/2 programs, allowing multiple programs to access the DLL. OS2.488 supports IBM's OS/2 Version 1.0 and above.



OS2TEST

The OS2.488 package contains OS2TEST, an interactive IEEE 488 interface test program. OS2TEST allows the user to interactively use the OS/2 DLL with a Ziatech IEEE 488 interface board. OS2TEST can support Ziatech IEEE 488 cards as controllers or talker/listeners, with full support for commands, as well as data transmission and receipt.

Ordering Information

ZT 97094

OS2.488 IEEE 488 Device Driver Software for Operating System/2®

- GpibDevClr sends a device clear or selected device clear.
- GpibPassControl passes control to another GPIB controller.
- GpibTransfer allows data to be transferred between two or more devices without controller intervention.
- GpibSerPoll serial polls the device list instruments.
- GpibSrqStatus returns status of SRQ line on IEEE 488 bus.

Figure 1. Controller command examples

- GpibDmaStatus checks for successful completion of DMA, or for error codes.
- GpibRecvData receives data from instruments on the bus, with or without DMA.
- GpibSendData sends data as ASCII or binary, with or without DMA.

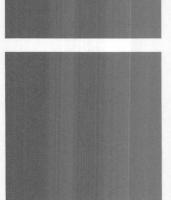
Figure 2. Talker/listener command examples



Appendices



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Inside This Section

- A: Application Note and Technical Brief Directory
- B: Bulletin Board Service
- C: Systems Engineering Course
- D: STD 32® Bus Overview
- E: STD 32 Connector Test Summary
- F: Battery Life
- G: Detailed Cable Descriptions
- H: Ziatech Warranty

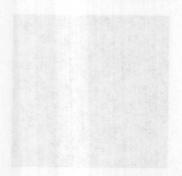
Appendices











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- A: Application Note and Yeshnizal Brief Directo
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Ap Notes and Tech Briefs

development process.

A Directory of Ziatech Technical Articles

Ziatech offers a series of application notes and technical briefs designed to provide detailed technical explanations and program

code for selected products.

The Ziatechnique Series
features extensive articles
exploring particular technical
issues as they relate to
Ziatech products. These
articles provide information
designed to simplify the
implementation of Ziatech
products.

Tech Briefs, as the name implies, are short articles detailing technical solutions for specific Ziatech products.

Contact Ziatech to request any of these articles.

Ziatechniques—Application Notes

Developing Software for an ARCNET Network Interface An explanation of how to program an ARCNET network interface card. Specific examples show how to use the ARCNET controller in a polled mode. Using the controller in an interrupt-driven application is also discussed.

Developing a ROM-based System A discussion of isssues involved with developing a ROM-based STD Bus system, using high-level languages and ROM-based utilities. This note examines the benefits and difficulties of "ROMing", and compares these to the development of operating system-based STD Bus systems. Included is a review of the compilers, device driver software, and development tools available for developing ROM-based systems, providing examples of how these software products can speed the ROM

Interrupt Handling with STD Bus Systems A look at how interrupts work with particular reference to the Intel 80 Series of microprocessors and the STD Bus. This note examines the programming aspects of interrupt handling in an STD DOS (MS-DOS on the STD Bus) environment, with special reference to shared and cascaded interrupts.

Expanding STD Bus Performance through Multiprocessing An overview of multiprocessing in STD Bus-based test and control applications. Included is a look at the STD 32 STAR SYSTEM and the Intelligent Control Processor (ICP). Interprocessor communication is also discussed.

Memory Configurations in STD DOS Systems 10 Detailed advice on memory types as they relate to STD DOS, single board computers, and I/O boards. Includes several helpful diagrams.

Direct Memory Access Techniques on the STD Bus An examination of the hardware and software issues involved in developing systems which use DMA. Ziatech STD Bus products are individually discussed for both DOS and non-DOS systems. Hardware initialization routines are discussed for three different board. Sample code is

Developing STD DOS-based Control System Applications 12 A description of the particular features of STD DOS systems that best suit the embedded and control environment, and discussion of issues that arise in the design of a DOS-based control applications.

Developing STD 32-based Fault Tolerant Control System Applications An examination of a system architecture which addresses the most stringent fault tolerance and redundancy requirements such as recover-

stringent fault tolerance and redundancy requirements such as recoveries in less than a tenth of a second, separate system backplanes and power supplies, primary and backup application software, and physical separation of systems.

Note: The Ziatechnique Series continues to expand to meet your technical needs. Contact Ziatech for the latest additions to this valuable resource.

Tech Briefs

1	Using the Event Interrupt of the Ziatech ZT 8845	
2	Using the Ziatech ZT 8825 EMS Memory Card with the ZT 8816/8817 CPU Card	
3	Running Novell Advanced NetWare on Ziatech's STD DOS Systems	
4	Using Turbo Debugger with Ziatech CPU Boards	
5	Networking Ziatech STD Systems to VAX Computers	
6	Using the Ziatech ZT 1490 PC Bus ARCNET Cards in S	Systems with VGA
7	Developing PROM disks for Ziatech CPU Cards	
8	Expanding System Memory in a Ziatech ZT 8808 STD DOS System	
9	The Ziatech Bookshelf	
10	Ziatech's ZT 8844 Compatibility Issues	
11	Printer Support Issues in DOS Systems	
12	Building Code with STD DDP: Using the Serial I/O Drive	er
13	Ziatech's ZT 8816/8817 Revision B	
14	Building Code with DDP: QuickBASIC Support	
15	Converting the MS-DOS Standard I/O Functions into User-customized I/O with STD ROM	
16	3.0 BIOS Considerations	
17	C Programming Notes: Accessing "far" Memory	
18	What Does CMOS Really Mean to STD Board-level Pro	ducts?
19	I/O Trapping on Ziatech's ZT 8816/17 Rev. B	
20	Flash EPROM on The ZT 8808/8809 SBCs and ZT 882	5 Memory Boards
21	Flat Panel Displays: An Overview	
22	ARCNET Timeout Requirements	
23	Using Timer/Counter 2 on the ZT 8910 CPU	
24	Ordering STD DOS 2.x Target Systems	
25	Using the Bernoulli Removable Media Disk Drive with Zi STD DOS Computer Systems	iatech
26	Understanding ZT 8910 Interrupt Architecture	
27	Dynamic Memory Management in STD ROM Systems	
28	Creating STD DDP Quick Libraries	
29	Using QuickBASIC on Ziatech STD Bus Computers	

Tech Briefs

30	Writing Interrupt Service Routines in C
31	STD DOS Usage of Timer/Counter 0
32	GENESIS Software on Ziatech Systems
33	Interfacing OPTO Racks to Ziatech I/O Boards
34	Configuring S: RAM Drives on Ziatech CPU Boards
35	Development Considerations for the Ziatech ZT 8801
36	ZT 8901 Memory Management
37	Selecting Encoders and Resolvers for Motion Control Feedback
38	Using Counter/Timers 0 and 1 in STD DOS Applications
39	TouchBase Drivers in Ziatech STD DOS Systems
40	Creating Message ROMs with STD ROM
41	Tempasonic Interfaces for STD Bus Applications
42	Accessory Options for the ZT 8931

Note: New *Tech Briefs* are continually added to this valuable reference library. Contact Ziatech or log on to our electronic bulletin board system (BBS) for the latest additions. The Ziatech BBS phone number is (805) 541-8218 with a format of 1200 or 2400 baud, 8 data bits, no parity, and 1 stop bit.

SteinE Hoef

TouchBase Drivers in Zigtech STD DOS Sycients	

Note: New Fedh Exters are continually added to this valuable inference library.

Contact Zialech or log on to our alectronic bulletin bound system (RRS) for the
ligners additions. The Zialech BBs prope number is (abs) 541-6218 with a
formal of 1200 or 2400 band. 6 data bits, no pasity, ext. 1 stop bit.



BBS # (805) 541-8218

BBS

Bulletin Board Service*

24 hour-a-day, on-line service provides customers with software updates, technical support, and new product information

The Ziatech Bulletin Board Service (BBS) provides electronic product information and technical support, 24 hours a day, year-round. Ziatech customers can exchange information, leave messages for Ziatech Technical Support, and upload and download files.

The Ziatech BBS also gives customers access to periodic software updates and Tech Briefs, which are "to-the-point" technical articles addressing common user problems. The service is implemented on Ziatech's ZT 8910 386SX Industrial Single Board Computer, operating STD DOS with modem services provided by the US Robotics Sportster 9600 Modem.

Accessing the BBS

A 1200 to 9600 baud modem and communications software (such as ProComm or Crosstalk) are necessary to access the BBS. The serial protocol is 8 bits, no parity, 1 stop bit. (In ProComm, "ALT-P" provides the configuration menu.)

Registering on the BBS

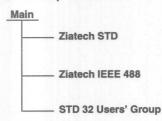
The BBS is open to all Ziatech customers at no charge; however, to make the most of its features it is necessary to receive a security upgrade. First time callers should register and then request an upgrade by leaving a message for the System Operator (SYSOP). Security will be upgraded within one working day.

Callers who do not register or receive an upgrade will not be able to access other conferences or download files.

With full user status, all of the BBS features, including uploads and downloads, are available.

The BBS Structure

The BBS is set up as follows:



The main board contains Tech Briefs, sample code and general files, bulletins, and messages. This area is available for access as soon as a user completes registration information. A conference contains its own set of bulletins, messages, and files that relate to the subject of the conference.

The BBS conferences are titled:

ZIATECH STD — this conference contains support and technical information relating to STD Busbased products. All Ziatech software and firmware are in the conference. Some files are password protected. These passwords can be obtained (from the Ziatech sales department) by purchasing the software or firmware.

ZIATECH IEEE 488 — this conference contains support information and software updates for Ziatech's GPIB products.

STD 32° USERS' GROUP – this conference is a forum for STD 32 designers.

Typing "J" at the main conference brings up a menu of available conferences. Entering the appropriate number transfers the user to the conference, which has its own message base, bulletins, and download files.

Downloading Files

The BBS contains many useful programs, software product updates, and technical information in files. Downloading of files from the BBS is restricted to upgraded users.

The "F" command displays the download directories available in a conference. A number selects the directory and displays the files in the directory. Typing "D" will initiate the download process. The BBS will prompt the user for the name of the file to be downloaded and the transfer protocol required. The transfer screen displays the number of (512 byte) blocks to be transferred. At this time, the user initiates the transfer from the local communications program.

(Continued on next page)



^{*}This is a general introduction to Ziatech's BBS. For more details on features and capabilities, call the Ziatech Technical Support department.

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Uploading Files

Customers may upload programs for Ziatech Technical Support to review, or upload programs of general interest to other users. Uploading a file is similar to downloading a file. Once connected to the Bulletin Board, typing "U" selects upload. The BBS will ask the name of the file to be uploaded and the protocol being used. The user then initiates the transfer.

Details

Hours of Operation — On-going, 24 hours-a-day
Protocol — 1200 to 9600 baud, 8 data bits, one stop
bit, no parity
BBS Phone Number — 805-541-8218

DOS Development, Hardware Overview, Interrupts, STD 32[®] Systems, and More . . .



Systems Engineering Course



Agenda:

STD Bus Computers

This course is designed to teach programmers and engineers the important aspects of implementing STD Bus systems. It will cover all the features of the STD Bus as well as useful programming techniques and applications for real-time control and automation systems. The course, outlined on the back, will include class exercises and handson lab time.

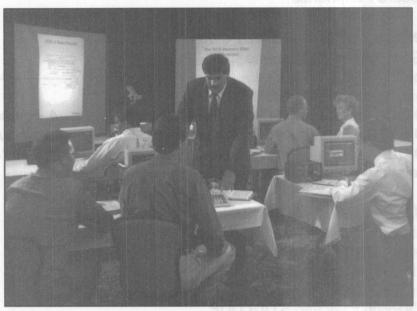
Prerequisites: MS-DOS Know-how

Those enrolling in this course should have a working knowledge of MS-DOS or substantial experience with another comparable operating system. Experience with a high-level language ("C" preferred) and a working knowledge of assembly language programming is strongly recommended.

Location:

California's Central Coast

San Luis Obispo is located on the beautiful Central Coast of California, halfway between Los Angeles and San Francisco. It is serviced by regular commuter flights from airports in both cities.



Each participant has hands-on access to a manual and system, reinforcing the concurrent classroom education.

Course Details:

- Length: 3 days (Call for current dates)
- Times: Day 1 8:30 A.M. 4:30 P.M.

Day 2 . 8:30 A.M. - 4:30 P.M.

Day 3 . 8:30 A.M. - 2:00 P.M.

- Maximum Class Size: 15 participants (register early!)
- Fee includes all classroom materials and lunches; it does not include accommodations.

To register and secure accommodations, contact Janice Legreid at (805) 541-0488. Payment in advance is required and may be made by check, purchase order, VISA, or Master Card. Cancellations made less than two weeks prior to the course are subject to a \$100 cancellation fee. A company group of three or more participants is eligible for a 10% registration discount. Special accommodation rates are available. Contact Ziatech for details.



FAX (805) 541-5088 • Telephone (805) 541-0488

Topics Covered in the System Engineering Course

STD Bus Characteristics

STD-80 Series STD 32[®]

PC Bus Comparison

Ziatech Single Board Computers

CPU Comparison Memory I/O On-board Peripherals

Development Considerations

DOS vs. Non-DOS Systems
Cost
Features and Functionality
STD DOS, PC-Assisted Development System
STD ROM, PROM-based Development System
STD DDP, Device Driver Package
Development for Multiprocessor Systems

Multiprocessing Systems

Master/Slave Systems
Ziatech I/O Control Processors
Multiple Master Systems
The STD 32 STAR SYSTEM™
STARWindows and STAR DDE
ZT 8911, ZT 8901, and ZT 8902

DOS-based System Considerations

Block Diagram of a DOS System DOS INT 21H BIOS Interrupts Hardware Interrupts Boot Behavior RAM and PROM Disks

ROM-based System Considerations

Choosing the Right Language
How to Debug Your Code
Paradigm DEBUG/RT
PDREMOTE/ROM
How to ROM Your Code
Start-up Code
Initialization
STD ROM Locate
Burning PROMs

Networking Considerations

ARCNET Ethernet

Systems and Enclosures

ZT 1000 Industrial Workstation
ZT 250 and ZT 300 Industrial Enclosures
DOS Licensing

Factory Tour (Optional)

A number of "hands-on" exercises are provided throughout the course to emphasize the course material, and demonstrate the use of development tools.

Total Course Length: 19.5 hours



One-on-one instruction is emphasized.



High Performance
COMPACT COMPUTERS FOR CONTROL

"We chose the high-performance STD 32 Bus because it is cost-effective, compact, and quick to implement."

Project Engineer, GM Delco Remy

"STD 32 retains the small STD Bus form factor and PC/AT capability... yet has a 16- and 32-bit data path that provides 386/486 processors on a full-power backplane."

Control Engineering Magazin

Compact, High-Performance Computers for Control Applications

The STD 32 Bus combines a small, industrial-strength architecture with the functionality and performance of today's high-end personal computers. This versatile 8-, 16-, and 32-bit scalable computer is the right choice for demanding real-time control and data acquisition applications where system size and cost are important.

Big Performance in a Small Way

Like larger, more expensive buses such as VME and MULTIBUS II, the STD 32 Bus supports 16- and 32-bit data transfers across the backplane, without the multiplexing of signals.

The STD 32 Bus can run at 32 Mbytes per second for very high-speed data-passing applications. Yet its EISA-like architecture provides more than just a high-performance data path. Other performance characteristics include:

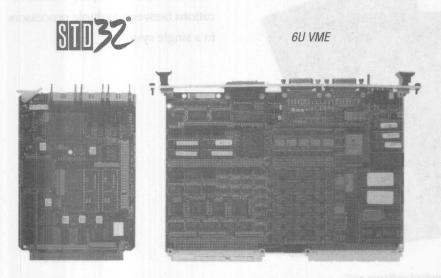
STD 32°, like EISA, provides a 32-bit growth path.

☐ Multiprocessing, with centralized arbitration logic to monitor access to the bus, allows the implementation of multiple processors in a single STD 32 system. The 32-bit throughput of the bus is crucial to interprocessor communication in real-time multiprocessing applications.

□ 32-bit addressing and pipelining dramatically improves throughput for block data transfers by reducing bus cycle time and increasing bus bandwidth.

☐ High-speed Direct Memory Access (DMA) over the backplane streamlines the operation of data-intensive applications.

☐ Slot-specific interrupts expand the number of available system interrupts for servicing system requests.



STD 32 provides a much smaller form factor than 6U VME, yet yields 32-bit performance and PC/AT compatibility that doesn't require special software or interfaces to operate. 3U VME supports a form-factor comparable in size to STD 32, but lacks its 32-bit, high-performance capability, and PC/AT I/O compatibility.

Extensive SOFTWARE

Software Support

STD 32 provides control system designers access to the variety of operating systems, software development tools, and control programs developed for personal computers. STD 32's alignment with the EISA and Intel 80x86 architectures enable it to operate MS-DOS®, Microsoft Windows™, OS/2®, UNIX®, and the countless programs that run on these software platforms.

Alignment with the Intel processor/EISA architecture also allows standard PC peripherals to be distributed on separate cards across the STD 32 bus. This is possible because STD 32 peripheral cards are mapped into a system the same way as PC peripherals, needing no special software to access them on the bus. The resultant modularity contrasts with other industrial buses that must con-

fine their peripherals to a single CPU card in order to run PC-oriented software and emulate PC functionality.

STD 32 software support goes beyond the typical single-user PC environment into real-time applications requiring multiprocessing. A standard for Interprocessor Communication (IPC) software incorporates a NetBIOS layer to simplify communications between multiple processors in a single system.



STD 32 takes advantage of industry standard software and operating systems.

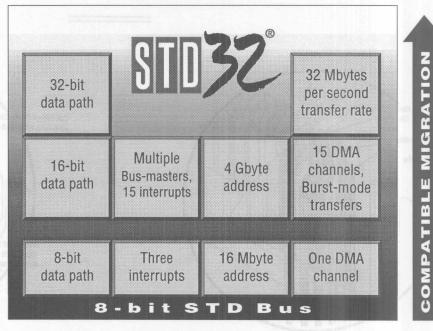
STD 32 is more than an extension to the traditional STD Bus architecture.

Compatibility is Assured

STD 32's "big bus" performance features are implemented on its Extended Architecture (EA) signals, which are interleaved with 8-bit Standard Architecture (SA) signals. The 8-bit SA signals assure STD 32's compatibility with 8-bit STD Bus cards designed to The STD-80 Bus Specification (IEEE 961). This gives STD 32 control systems access to the large variety of industrial interface cards built to the STD-80 specification, while at the same time providing a migration path for next generation "burst mode" and 32-bit data path products.

STD 32's backward compatibility also lets manufacturers build products that will operate in both STD 32 and STD Bus systems. This open bus standard is licensed to ensure 100% compatibility to the specification, so that a control system designer can use products from any STD 32 manufacturer and be confident of compatibility. The comprehensive STD 32 specification clearly defines electrical and mechanical details, including connector and plating information, and a description of the timings associated with each transaction.

(For details, see the "Short Form Specification" found at the back of this brochure).



STD 32, a superset of the STD Bus standard, incorporates all the features of the 8-bit STD Bus while providing a migration path to more demanding designs.

New Connector COMPATIBILITY

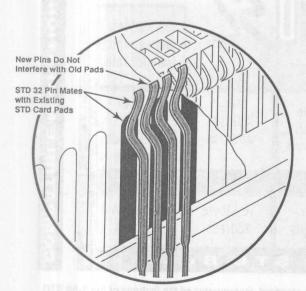
New, High Technology Connector Increases Performance and Reliability

The STD 32 connector provides a mechanism for more performance, while maintaining 8-bit compatibility. The STD 32 card edge accommodates 136 contacts, interleaving 80 additional signals with the original 8-bit signals.

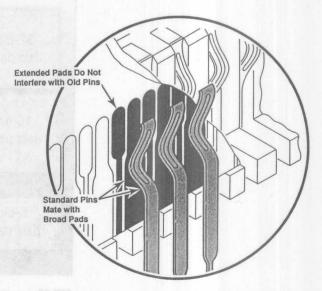
The STD 32
connector
interleaves the
new signals
with the old for
compatibility.

A state-of-the-art "hemispherical" contact design allows this increase in connector density without increasing connector dimensions, and offers better contact pressure, conductivity, and resistance to shock and vibration than the older STD Bus connector design.

The STD 32 connector also provides 75% more power and ground connections to further improve current handling and reliability.



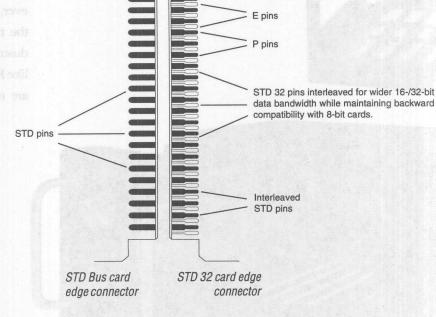
Existing 8-bit STD board inserted into a connector on the STD 32 backplane (enlarged view).

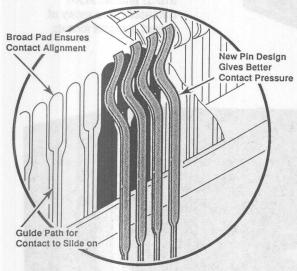


STD 32 board inserted into a connector on an 8-bit, STL backplane (enlarged view).

In a series of tests conducted by the independent testing lab of Contech Research Inc., (Attleboro, MA) the STD 32 connector performed comparably, and in some cases better than DIN connectors. The STD 32 connector also tested better than the 8-bit STD, ISA, and EISA connectors.

The Contech tests demonstrated the STD 32 connector's superiority over DIN relative to current carrying capacity, its contact pressure advantage over the 8-bit STD and ISA buses, and its better resistance to shock and vibration than EISA.





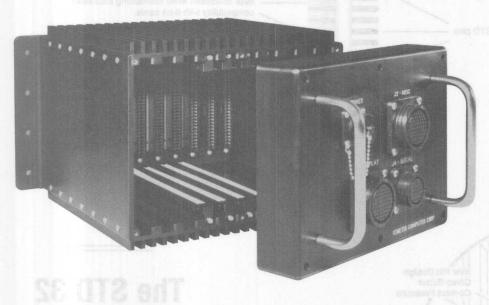
STD 32 board inserted into an STD 32 backplane (enlarged view).

The STD 32 connector measures up to DIN reliability.

Industrially RUGGED.

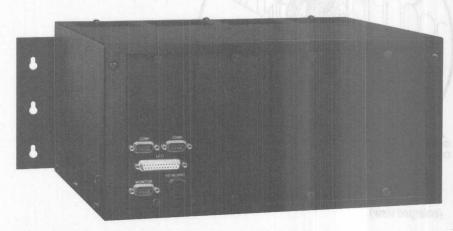
Industrial Alternative to Personal Computers

The small format, PC/AT-compatibility, functionality, and performance of the industrial STD 32 Bus make it a more rugged and reliable alternative to "industrialized" (passive backplane) PC systems. However, STD 32 systems can still utilize the multitude of PC-compatible industrial software available today. Unlike PC-based systems, STD 32 cards are retained on four sides and en-



STD 32 provides PC/AT compatibility in a variety of rugged, industrial formats.

connector measures up to DIN reliability.



closed in rugged cages and boxes. Many STD 32 products are available in versions capable of operating in extreme heat or cold (-40° to +85° Celsius). An STD 32 computer can load an operating system, Windows, and/or a control application from ROM or flash Memory, providing a fast boot-up. This eliminates the need for less reliable rotating disk drives and battery-backed RAMs.

The semiconductor industry's trend toward smaller circuitry favors STD 32, as the performance and features of high-end 80x86 computers are compressed onto a single 4.5-by 6.5-inch STD 32 computer card.

features on a small, rugged computer bus

The adaptation of EISA technology allows STD 32 to deliver its 32-bit performance and PC/AT software compatibility in a format that is not only smaller, but also less expensive than larger industrial buses.

The bus comparison chart on this page illustrates how the modular STD 32 approach combines the best of both personal and industrial computers into a compact, cost-effective control solution.

Bus Type	Most Popular CPU Type Used	Board Area (sq. inches)	Maximum Data Width (bits)	Max. Backplane Transfer (Mbytes/second)	Supports Multiprocessing Standard
PC/AT	Intel	62	16	8	No
EISA	Intel	62	32	32	Yes
STD	Intel	26	8/16*	4	No
STD 32	Intel	26	32	32	Yes
MULTIBUS I	Intel	70	16	10	No
MULTIBUS II	Intel	71	32	40	Yes
3U VME	Motorola	24	16**	20	Yes
6U VME	Motorola	57	32	40	Yes

* 8-bit multiplexed to 16-bit

^{**}A proposed standard would multiplex 16-bit designs to achieve 32-bit performance

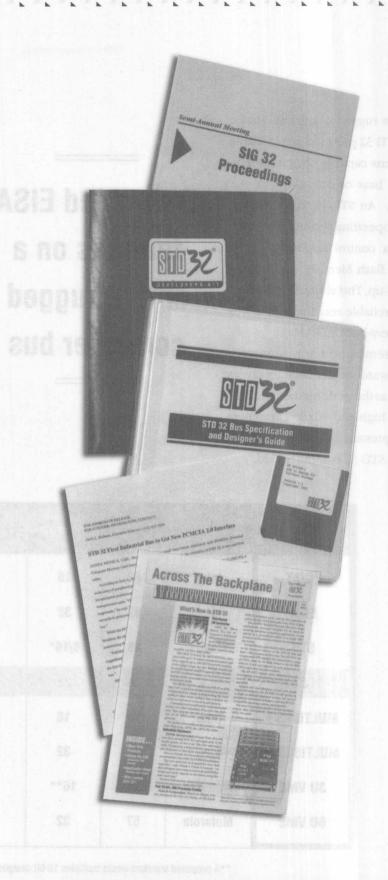
Broad SUPPORT

STD 32 Special Interest Group

The STD 32 Special Interest Group (SIG 32) provides a forum for users and manufacturers to exchange information and expand on this popular bus architecture. Since its inception, SIG 32 has acted on proposals for military ruggedization specifications for STD 32, and an open Interprocessor Communication (IPC) for STD 32 Multiprocessing.



The complete, 200-page *STD 32 Bus Specification* and STD 32 Prototyping Kit are available from SIG 32. Those interested in more STD 32 information can contact SIG 32's toll free numbers. Phone: (800) 733-2111, FAX: (800) 733-3959. A list of STD 32 manufacturers, available from SIG 32, also makes it possible to contact individual STD 32 companies.



Short-form SPECIFICATION

The STD 32 Bus Specification: A Brief Overview

The STD 32 Bus Specification extends the capabilities of the STD-80 Series standard, while remaining compatible with existing STD Bus cards. These excerpts from the specification provide mechanical and electrical details pertinent to a technical evaluation of the bus. For the complete specification, contact SIG 32.

Mechanical

Connectors

The 136-pin STD 32 card connectoruses cantilever beam construction with a hemispherical contact point. This connector/contact style is similar to EISA and Micro Channel designs, and is considered one of the most reliable in the industry (see **Figure 1**).

Connector Specifications

- Number of Contacts: 136
- Contact Design:
 Cantilever beam, hemispherical contact point
- Contact Plating: 30 µinches of gold over 50 µinches nickel (minimum)
- Current Capacity: 1.0 Amp (minimum per pin)
- Mating PCB Thickness: 0.062 inch ±0.007 inch
- *Operating Temperature:* -40° to +85° C
- Mating Cycles: 500 (minimum)
- *Insertion Force:* 6 ounces per contact pair

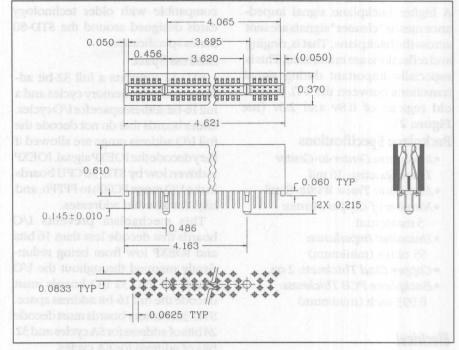


Figure 1. The STD 32 connector contacts are arranged as 68 directly opposed pairs. The center section of 57 contact pairs provide backward compatibility with older STD-style cards and expansion to 16-bit non-multiplexed transfers. The remaining 11 contact pairs on the card extensions allow 32-bit non-multiplexed data transfers while maintaining compatibility with older 8-bit STD I/O cards.

- Vibration:
 10 Hz to 2 KHz at 15 Gs with
 0.06-inch displacement
- Contact Normal Force: 135 grams per contact
- Connector Body:
 Glass-filled polyphenylene sulfide, UL 94V-0
- Insulation Resistance:
 Greater than 50,000 Megohms
- Operating Humidity:
 0 to 95% with no condensation

Connector Mating Surfaces

The design of the connector mating surface (or "gold fingers") is the core of the *STD 32 Bus Specification*. This design not only allows the number of contacts to increase from 56 to 136 but also provides a backward-compatible platform for the thousands of older STD I/O cards currently available for the STD Bus.

Mating Surface Specifications

- PCB Thickness: 0.062 Inch ±0.007 inch
- Plating:30 μinches of gold over50 μinches of nickel
- Design:
 Conforms to STD 32 P/E finger dimensions

Backplane

Another critical component in an STD 32 system is the backplane. The backplane design incorporates several important features including increased backplane signal impedance.

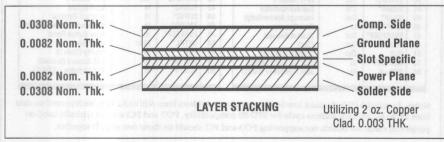


Figure 2. Backplane signal impedance is enhanced by maximizing the separation of the signal planes from the power and ground planes. Minimizing the trace width and maximizing its height also enhances impedance.

A higher backplane signal impedance means "cleaner" signals are sent across the backplane. That is, ringing and reflections are minimized. This is especially important during signal transitions between the TTL threshold regions of 0.8v and 2.0v (see **Figure 2**).

Backplane Specifications

- Minimum Center-to-Center Trace Spacing: 16 mil
- Minimum Trace Width: 8 mil
- Number of Copper Planes: 5 maximum
- *Unloaded Impedance*: 55 ohms (minimum)
- Copper Clad Thickness: 2 oz.
- Backplane PCB Thickness: 0.093-inch (minimum)

Electrical

Pin Descriptions

See Figures 3 and 4.

Clock Frequency

The STD 32 Bus uses the signal CLOCK* for synchronous communication between Bus Masters (CPUs) and peripheral boards, and for other system management features such as arbitration. The Permanent Master is responsible for driving CLOCK* in all systems. The CLOCK* frequency is 8 MHz.

Transfer Types

STD 32 defines five classes of backplane transfers for communication between Bus Masters and peripherals. Standard Architecture (SA) transfers define compatible cycles for older STD-80 Series peripherals. Both 8and 16-bit SA transfers are allowed through dynamic bus sizing. Extended Architecture (EA) transfers support 8-, 16-, and 32-bit data widths with a transfer cycle as short as one CLOCK* cycle. The maximum bandwidth for EA transfers is 32 Mbytes/second (see Figure 5). The cycle performed is dynamically sensed by the Bus Master from control signals that the peripheral returns. The default cycle is an SA 8-bit (SA8) cycle to remain

compatible with older technology cards designed around the STD-80 Series specification.

Address Space

STD 32 supports a full 32-bit address space for memory cycles and a full 16-bit address space for I/O cycles. Older boards that do not decode the full I/O address range are allowed if they decode the IOEXP signal. IOEXP is driven low by STD 32 CPU boards in the I/O range FC00h to FFFFh, and high for all other addresses.

This mechanism prevents I/O boards that decode less than 16 bits and IOEXP low from being redundantly mapped throughout the I/O space. All STD 32 I/O boards must decode the full 16-bit address space. STD 32 memory boards must decode 24 bits of address for SA cycles and 32 bits of address for EA cycles.

Standard Architecture (SA) Cycles

SA cycles are nominally five CLOCK* cycles. The upper 8 bits of

memory address (A16 to A23) is multiplexed with the data lines to allow the full, 16 Mbyte address range required by 286 and 386SX processors. This multiplexing scheme is compatible with STD-80 Series boards. 8-bit data transfers are performed unless the memory board being accessed returns MEM16* at the beginning of the cycle. When MEM16* is returned, a 16-bit SA cycle is defined (SA16), and the additional data signals D8 to D15 are driven on non-multiplexed pins. I/O cycles can also be 16 bits if the signal IO16* is driven by the I/O board during the transfer.

Extended Architecture (EA) Cycles

STD 32's default transfer is an SA class cycle. If, during the beginning of a cycle, EX8*, EX16*, or EX32* is driven low by a peripheral board, then Extended Architecture cycles are performed. EX8*, EX16*, and EX32* define 8-, 16-, and 32-bit EA transfer capability, respectively. Burst cycles

	60	MPONENT	SIDE			C
Pin	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Sign
1	+5VDC	In	Logic Power	2	+5VDC	In
3	GND	In \	Logic Ground	4	GND	In
5	VBAT	Bidir	Battery Power	6	DCPDN*	Bio
7	A19/D3	Out/Bidir	Address/Data	8	A23/D7	Ou
9	A18/D2	Out/Bidr	Address/Data	10	A22/D6	Ou
11	A17/D1	Out/Bidr	Address/Data	12	A21/D5	Ou
13	A16/D0	Out/Bidr	Address/Data	14	A20/D4	Ou
15	A7	Out	Address	16	A15	Ou
17	A6	Out	Address	18	A14	Ou
19	A5	Out	Address	20	A13	Ou
21	A4	Out	Address	22	A12	Ou
23	A3	Out	Address	24	A11	Ou
25	A2	Out	Address	26	A10	Ou
27	A1	Out	Address	28	A9	Ou
29	A0	Out	Address	30	A8	Ou
31	WR*	Out	Write Mem or I/O	32	RD*	Ou
33	IORQ*	Out	I/O Address Select	34	MEMRQ*	Ou
35	IOEXP	Out	I/O Expansion	36	BHE*	Ou
37	INTRQ1*	In	Interrupt Request 1	38	ALE*	Ou
39	STATUS1*	Out	CPU Status 1	40	STATUSO*	Our
41	BUSAK*	Out	Bus Acknowledge	42	BUSRQ*	In
43	INTAK*	Out	Interrupt Acknowledge	44	INTRQ*	In
45	WAITRQ*	In	Wait Request	46	NMIRQ*	In
47	SYSRESET*	Out	System Request	48	PBRESET*	In
49	CLOCK*	Out	Clock	50	CNTRL*	Bid
51	PCO	Out	Priority Chain Out	52	PCI	In
53	AUX GND	In	AUX Ground (bussed)	54	AUX GND	In
55	AUX +V	In	AUX Positive (+12VDC)	56	AUX -V	In

CIRCUIT SIDE				
Pin	Mnemonic	Signal Flow	Description	
Pin 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36 38 40	#5VDC GND DCPDN* A23/D7 A22/D6 A21/D5 A20/D4 A15 A14 A13 A12 A11 A10 A9 A8 RD* MEMRQ* BHE* ALE* STATUSO*	In In In Sidir Out/Bidir Out/Bidr Out/Bidr Out/Bidr Out/Bidr Out/Bidr Out/Bidr Out	Description Logic Power Logic Ground DC Power Down Address/Data Address/Data Address/Data Address/Data Address/Data Address	
42 44 46 48 50 52 54 56	BUSRQ* INTRQ* NMIRQ* PBRESET* CNTRL* PCI AUX GND AUX -V	In In In In Bidir In In	Bus Request Interrupt Request Non-Maskable Int Request Push-Button Reset Aux Timing Priority Chain In AUX Ground (bussed) AUX Negative (-12VDC)	

Notes: An asterisk (*) indicates a low level active signal. Address lines A16 to A23 are multiplexed on data lines D0 to D7 on each address cycle for STD-80 compatibility. PCO and PCI are not typically used on peripheral cards. All boards not supporting PCO and PCI should tie these two signals together.

Figure 3. This table illustrates the STD 32 Bus P Pinouts (Table 3-2 in the STD 32 specification). See the next page for a description of the E Pinouts.

are also possible for EA devices when the peripheral drives SLBURST*, while the Bus Master is driving MSBURST*. Burst cycles allow up to 32 bits of data to be transferred on every CLOCK*, for a 32 Mbyte/second transfer rate. The nominal cycle (non-burst) is a two-CLOCK* cycle. EA cycles use separate data and address signals (not multiplexed) to allow pipelined execution of the transfer.

Direct Memory Access (DMA)

Backplane Direct Memory Access (DMA) transfers are also defined for the Extended Architecture, at up to 32 Mbytes/second. Each of the first 15 slots in an STD 32 card cage has a dedicated set of DMA control signals to allow for true backplane DMA transfers. Older technology DMA mechanisms on the STD bus have required front plane cabling.

Interrupt Topology

STD 32 defines five bussed interrupt signals and one slot-specific interrupt for application use and system management.

Bussed Interrupts

INTRQ*, INTRQ1*, INTRQ2*,INTRQ3*,and NMIRQ* are bussed sig-

nals between all STD 32 connectors, including Slot X. Bus Masters use these signals for interrupt signaling between peripherals or Bus Masters and other Bus Masters.

Slot-Specific Interrupts

Each of the first 15 slots of the STD 32 card cage has a dedicated interrupt between it and the Slot X connector (the last connector on the left side of the backplane). For Bus

CIRCUIT SIDE

Transfer CLASS	Nominal Transfer Rate	Burst Transfer Rate	
SA8	2 Mbytes/second	N/A	
SA16	4 Mbytes/second	N/A	
EA8	4 Mbytes/second	N/A	
EA16	8 Mbytes/second	16 Mbytes/second	
EA32	16 Mbytes/second	32 Mbytes/second	

Figure 5. Theoretical bandwidths for STD 32 transfer types

Masters that can interface to Slot X, this allows up to 15 interrupt sources in addition to the five bussed interrupts.

Multiprocessor Arbitration

The Slot X connector on STD 32 backplanes allows for a centralized arbitration scheme for up to 15 Bus Masters. Each slot has dedicated arbitration signals (MREQx*/MAKx*) which are used to gain control of the bus. EA Temporary Masters use the MREQx*/MAKx* signals for bus arbitration. SA Temporary Masters use a similar approach, but use the DREQx*/DAKx* signals for bus ownership. A centralized arbiter manages bus ownership between Temporary Masters and the Permanent Master. Rotating priority or optional fixed priority can be selected.

Compliance Levels

Compliance levels specify the capabilities of STD 32 board designs. Each bus-related feature, such as the ability to support EA or SA transfers, is given a mnemonic description to be used on data sheets and board specifications to assist customers in system configuration.

Board MODES

There are five board MODES within STD 32 as defined in **Figure 6**. MODES define how a board may be used. For instance, a CPU board would normally be a Permanent Master but when another Bus Master has control it might also support memory cycles to or from it by the Temporary Master. In this case the board would have two board MODES, Permanent Master and Memory Slave.

	CO	MPONENT:	SIDE
Pin	Mnemonic	Signal Flow	Description
1	+5 VDC	In	Logic Ground
3	XA19	Out	Address
5	XA18	Out	Address
7	XA17	Out	Address
9	XA16	Out	Address
11	NOWS*	In	No Wait States
13	+5VDC	In	Logic Power
15	DAKx*	Out	DMA Acknowledge
17	GND	In	Logic Ground
19	D27	Bidir	Data
21	D26	Bidir	Data
23	D25 D24	Bidir Bidir	Data
27	D24 D23	Bidir	Data Data
29	D23	Bidir	Data
31	D21	Bidir	Data
33	D20	Bidir	Data
35	GND	In	Logic Ground
37	D19	Bidir	Data
39	D18	Bidir	Data
41	D17	Bidir	Data
43	D16	Bidir	Data
45	GND	In	Logic Ground
47	IRQx	In .	Interrupt Request
49	BE1*	Out	Byte Enable 1
51	BEO*	Out	Byte Enable 0
53	MEM16*	In	Memory 16-bit
55	M-10	Out	Memory or I/O
57	DMAIOW*	Out	DMA I/O Write
59 61	I016* CMD*	In Out	I/O 16-bit
63	EX16*	In	Command Exchange 16-bit
65	EXRDY	in in	Exchange Ready
67	INTRQ3*	In	Interrupt Request 3
69	MAKx*	Out	Master Acknowledge
71	SLBURST*	In	Slave Burst
73	XA27*	Out	Address
75	XA26*	Out	Address
77	XA25*	Out	Address
79	XA24*	Out	Address

	GIRGUH SIDE				
Pin	Mnemonic	Signal Flow	Description		
2 4 6 8 10 12	LOCK* XA23 XA22 XA21 XA20 RSVD	Out Out Out Out Out	Lock Address Address Address Address Reserved		
14 16 18 20 22 24 26 28 30 32 34 36 38 40 42 44 46 48 50 52 54 56 66 66 67	+5VDC DREQX* GND D31 D30 D29 D28 GND D15 D14 D13 D12 D11 D10 D9 D8 MASTER16* AENX* BE3* BE2* GND W-R GND W-R START* EX32* T-C +5VDC* MREQX*	In In Bidir Out Out Out In Out In Out In Out In In Didir In Bidir	Logic Power DMA Request Logic Ground Data Data Data Data Logic Ground Data Data Data Data Data Data Data Dat		
72 74 76 78 80	MSBURST* XA31* XA30* XA29* XA28*	Out Out Out Out Out	Master Burst Address Address Address Address		

Figure 4. This table illustrates STD 32 Bus E Pinouts. (Table 3-3 in the STD 32 specification)

STD 32 Board MODE **Definition** Bus master that drives CLOCK*, monitors PBRESET*, **Permanent Master** and drives SYSRESET* **Temporary Master** Bus Master that requests the bus via BUSRQ*, MREQx, or DREQx* Slave that decodes and responds to SA or EA I/O cycles I/O Slave **Memory Slave** Slave that decodes and responds to SA or EA memory cycles System arbiter that manages n MREQx*/MAKx* signals Arbiter (Mn, Dn) and/or n DREQx*/DAKx* signals for arbitration

Figure 6. STD 32 compliance board MODES

Compliance CLASSES

For each board MODE, there are several CLASSES of transfers supported

for that CLASS. Standard Architecture (SA) 8-bit and 16-bit transfer CLASSES are defined as SA8 and SA16 respec-

Feature	Description	Additional Signal Support
A16	SA 16-bit I/O address decode (I/O Slave)/ generation (master)	A0-A15
A24	SA 24-bit memory address decode (Memory Slave)/generation (master)	A0-A24
D8	SA 8-bit data transfer, masters/slaves	D0-D7
D16	SA 16-bit transfer, masters/slaves	D0-D15,MEM16*,BHE*,I016*
EBURST	EA Burst transfer capability, masters/slaves	SLBURST*,MSBURST*
EDMAA	EA type A DMA transfers supported, masters/slaves	DMAIOW*,DMAIOR*, DRQx,DAKx*,T-C
EDMAB	EA type B DMA transfers supported, masters/slaves	DMAIOW*,DMAIOR*, DRQx, DAKx*,T-C
EDMAC	EA type C DMA transfers supported, masters/slaves	DMAIOW*,DMAIOR*, DRQx, DAKx*,T-C SLBURST*, MSBURST*
GAX	EA geographical address support masters/slaves	AENx* (masters)
DOKO !	SA (STD-80) interrupt generation (slaves)/ servicing (masters) on INTRO*, INTRO*, NMIRO*, CNTRL* (INTRO2*), or INTRO3*	INTRQ*,INTRQ1*,NMIRQ* [CNTRL* (INTRQ2*)], INTRQ3*
ICA	Cascadable interrupt address support, masters/slaves	A8-A10 during INTA
IXP	Slot-specific interrupt servicing (Permanent Masters)/ generation (slaves), positive edge-triggered	IRQx
IXL	Slot-specific interrupt servicing (Permanent Masters)/ generation (slaves), low-level asserted	IROx and
МВ	Bus arbitration via BUSRQ*/BUSAK* - SA Masters only	BUSRQ*,BUSAK*
MD	Bus Arbitration via DREQx*/DAKx* - SA Masters only	DREQx*, DAKx*
мх	Bus Arbitration via MREQx*/MAKx* (Permanent Master)/ request (Temporary Slave)	MREQx*,MAKx*
NOWS	No wait-state (NOWS*) support	NOWS*
SDMA8	8-bit SA frontplane DMA as specified in Chapter 2, masters/slaves	
SDMA16	16-bit SA frontplane DMA as specified in Chapter 2, masters/slaves	
KA16	EA 16-bit address decode, I/O transfers	A2-A15, BE0*-BE3* as per Chapter 3
(A32	Full 32-bit EA address space driven, masters may pull XA24*-XA31* passively high Full 32-bit EA address decoded by Memory Slaves	A2-A15, XA16-XA23, XA24* XA31*, BE0*-BE3*
KD8	8-bit EA data transfer, masters/slaves	D0-D7
KD16	16-bit EA data transfer, masters/slaves	D0-D15, EX16*, BE0*-BE3*
(D32	32-bit EA data transfer, masters/slaves	D0-D31, EX16*, EX32*, EX32* BE0* BE3

Figure 7. STD 32 compliance product descriptor feature listing

tively. Extended Architecture (EA) 8-, 16-, and 32-bit transfer CLASSES are defined as EA8, EA16, and EA32, respectively.

Compliance Product Description Features (Requirements/Options)

Listed after the CLASS support for each board MODE is a string of features that are requirements and/or options that the board supports. Requirements are items such as interrupt support or DMA that a board needs in order to operate. Options are items that may be used by a board but are not required for operation. Possible features for STD 32 compliance codes are found in **Figure 7.**

Compliance Style

Technical data sheets for STD 32-compatible boards include a product descriptor. This shows that the board complies with the STD 32 specification in all board MODES, transfer CLASSES, and required or optional features listed (see **Figure 8**).

For example, a board that can be either a Permanent Master or a Temporary Master with full EA8, EA16, EA32, SA8, and SA16 transfer CLASS support, interrupt support, cascade interrupt control, and that supports SA8 memory transfers to or from it when it is not in control would have the following product descriptor:

STD 32 Compliance

Permanent Master: EA32, EA16, EA8, SA16, SA8 - MX, MB, ICA, I Temporary Master: EA32, EA16, EA8, SA16, SA8 - {MX}, MB, ICA, I Memory Slave: SA8

STD 32 Compliance

Permanent Master: Classes supported-(Requirements) Options
Temporary Master: Classes supported-(Requirements) Options
I/O Slave: Classes supported-(Requirements) Options
Memory Slave: Classes supported-(Requirements) Options
Arbiter (Mn, Dn): Classes supported-(Requirements) Options

Figure 8. STD 32 compliance format

STD 32[®] Connector Test Summary

This report summarizes the results of a series of tests performed on the STD 32 connector by Contech Research in June of 1992.

Ziatech and SIG 32 (the STD 32 Special Interest Group) sponsored these tests to determine if the STD 32 connector is suitable for use in harsh environments. For comparison purposes, the same tests were performed on a VME-style DIN connector.

All tests were performed in accordance with the appropriate MIL standard where applicable. Acceptance/ rejection criteria are defined for each test. In most cases, Low-Level Contact Resistance (LLCR) measurements were taken on each contact before and after the test to identify any changes that may have occurred as a result of the test.

LLCR changes indicate likely changes in connector performance as a result of the conditions encountered in each of the tests. Some change is to be expected and the classification of the magnitude of the change is as follows:

< 5.0 milliohms	Stable ROLL RESPONSED
5.1 to 10.0 milliohms	Stable with minor changes
10.1 to 15.0 milliohms	Stable with significant change
15.1 to 25.0 milliohms	Marginal stability in non-benign applications
25.1 to 50.0 milliohms	Unstable in non-benign, marginal in benign applications
>50.1 milliohms	Unstable

Tests results were grouped into different test types.

Group A. Durability

Test Title	Durability		
Measures	Durability over a number of m Used to determine wear char the life of the connector.		
Test Procedure	MIL-STD-1344, Method 2016	3	
	STD 32	DIN	
Visual Inspection for Damage	No Damage	No Damage	
Mating Force (lbs.)	<31.3	<21.2	
After 25 Cycles	<27.0	<17.2	
After 50 Cycles	<28.0	<20.1	
Unmating Force (lbs.)	>6.8	>17.5	
After 25 Cycles	>7.2	>15.5	
After 50 Cycles	>6.5	>19.2	
Change in LLCR			
After 25 Cycles	<0.7mΩ	<0.3mΩ	
After 50 Cycles	<0.4mΩ	<0.4mΩ	



Group A. Durability (continued)

Test Title	Thermal Shock		
Measures	Changes in resistance of connectors after repeated exposures to extremes of temperature and rapid temperature changes. MIL-STD-1344, Method 1003 Maximum temperature: 105°C Time at temperature: 30 minutes Transition: Immediate		
Test Procedure			
	STD 32	DIN	
Visual Inspection for Damage	No Damage	No Damage	
Change in LLCR	elda	milliohms St	
After 25 Cycles	<1.2mΩ	<0.6mΩ	
After 50 Cycles	<1.9mΩ	<0.7mΩ	

Test Title	Humidity	
Measures	Stability of connector when expose temperature and humidity. Resista penetration and migration.	
Test Procedure	MIL-STD-1344, Method 1002, Prod Relative Humidity: 90 - 95% Temperature: 25°C to 65°C Duration: 240 Hours	cedure II
	STD 32	DIN
Visual Inspection for Deterioration	No Damage	No Damage
Change in LLCR	6.16>	
After 25 Cycles	<1.0mΩ	<0.6mΩ
After 50 Cycles	<1.2mΩ	<0.3mΩ

Group B. Electrical Characteristics

Test Title	Dielectric Withstanding Voltage		
Measures O n	Ability to operate at rated voltage and withstand overvoltages at ambient temperature and after exposure to temperature extremes.		
Test Procedure	MIL-STD-1344, Method 3001, and Method 1003 Hold Time: 60 seconds Test Voltage: 650 VAC Rate: 500 Volts/second		
	STD 32	DIN	
Test for arcing or breakdown at rated voltage	No arcing or breakdown	No arcing or breakdown	
After temperature Cycle	No arcing or breakdown	No arcing or breakdown	

Test Title	Insulation	Insulation Resistance	
Measures	Resistance of insulation to DC leakage current.		
Test Procedure	MIL-STD-1344, Method 3003 Hold Time: 2 minutes Test Voltage: 100 VDC	Test Cu Daration	
amade	STD 32	DIN	
Insulation Resistance	>50,000MΩ	>50,000MΩ	

Test Title	Insulation Resistance with Humidity				
Measures	Resistance of insulation to DC leakage current after humidity cycling.				
Test Procedure	MIL-STD-1344, Method 1002 Hold Time: 2 minutes Relative Humidity: 90 to 95% Duration: 240 hours Test Voltage: 100 Temperature: 20°0				
	STD 32	DIN			
Visual Inspection for Deterioration	No Damage	No Damage			
Insulation Resistance	>50,000MΩ	>50,000MΩ			

Group C. Shock and Vibration

Test Title	Shock			
Measures	Effect of shock on the connectors.			
Test Procedure	MIL-STD-1344, Method 2004, Test Condition C Peak: 50G Duration: 6msec Wave Form: Half sine Velocity: 12.3 feet per second Number of shocks: 3 shocks per axis, 3 axes			
	STD 32 4 038 (specie)	DIN		
Visual Inspection for Deterioration	No Damage	No Damage		
No interruption of	50 011			
greater than one microsecond	Pass Pass			
Change in LLCR	<6.2mΩ	<5.0mΩ		

Test Title	Vibration			
Measures	Short- and long-term effect of vibration on the connectors.			
Test Procedure	MIL-STD-1344, Method 2005, Test Condition III Frequency: 10 to 2000 Hz Amplitude: 0.06" (1.50mr Test Current: 100mA Sweep Time: 20 minutes Duration: 40 hours per axis, 3 axes total			
Visual Inspection for Deterioration	STD 32 OF Separito	DIN		
	No Damage	No Damage		
No interruption of greater than one microsecond	Pass	Pass		
Change in LLCR	<3.8mΩ	<4.8mΩ		

Group D. Gas Tightness

Test Title	Gas Tightness			
Measures	Effect of hostile gas atmospheres on connectors and integrity of the contact interface.			
Test Procedure	EIA RS-364, TP-36, Method I Gas: Nitric Acid Duration: One hour LLCR: Measured after drying	Isual inspection or Detariors registion		
	STD 32	DIN		
Change in LLCR	<3.3mΩ	<0.5mΩ		

Group E. Connector Performance

Test Title	Capacitance		
Measures	Capacitance between contacts		
Test Procedure	MIL-STD-202, Method 305 Frequency: 1MHz Acceptance Limit: 2.0pF	and Procedure Const.	
MO	STD 32	DIN	
Capacitance	<0.4pF	<0.5pF	

Test Title	Current Carrying Capacity			
Measures	Temperature rise at different current levels			
Test Procedure	IEC 512-3, Test 5 and EIA 364, TP 70			
erl	STD 32	edura NIC Connectors		
Temperature Rise	mber of times and contact had equal. After ough section, a	run belhasga		
1 Amp	0.4°C	0.6°C		
3 Amp	mexa vilati 2.6°C (1.7 desag	3.2°C		
5 Amp	4.1°C	8.9°C		
7.5 Amp	8.8°C	Exceeds rating		

Test Title	Plating Thickness		
Measures	Thickness of gold plating	ter 250 Cycles	
Test Procedure	X-ray florescence measurement	ter 500 Ovdies	
Average Gold	STD 32	DIN TO LETS THE	
Average Gold Thickness	37.9 microinches	4.3 microinches	

Note: The STD 32 Specification calls for a minimum of 30 microinches of gold for both the connector and card edge.

Test Title	Porosity		
Measures	Porosity and other imperfections on contact surfaces.		
Test Procedure	MIL-STD-1344, Method 1017		
20N 290 Class 1,	STD 32	DIN itsigns	
Observations	Generally pore free with evidence of minor porosity	Generally pore free with two contacts exhibiting porosity	

Group E. Connector Performance (continued)

Test Title	Normal F	Normal Force		
Measures	The normal force, a measure of contact pressure and integrity. Higher normal forces establish gas-tight seal and prevents oxide growth.			
Test Procedure	Connectors were dismantled and the contacts de and the force measured.			
	STD 32	DIN		
Normal Force Range	132 to 150 grams	7 to 75 grams		

Test Title	Wear Analysis				
Measures	The wear on contacts from repeated mating and unmating.				
Test Procedure	Connectors were mated and unmated for the specified number of times and contact resistance changes measured. After each section, a group of contacts were removed and exposed to hydrochloric acid and a DMG solution (in accordance with EIA 364, TP-85, Paragraph 7.1) and visually examined for exposure of nickel or base metal.				
malling his same	STD 32	DIN			
LLCR Change					
After 25 Cycles	0.0mΩ	<0.1mΩ			
After 100 Cycles	<0.2mΩ	<0.2mΩ			
After 250 Cycles	<0.1mΩ	<0.6mΩ			
After 500 Cycles	<0.5mΩ	<0.6mΩ			
General Comments	100 to 200 cycles can be obtained, possibly up to 500.	Acceptable up to 500 cycles due to low normal force, but this has other implications			

Conclusions:

The STD 32 connector passed all the essential tests and performed as well as the DIN connector overall. The STD 32 connector exceeded the DIN connector in gold plating and current carrying capacity by wide margins. STD 32 connector specifications are provided below. See also the Short Form Specification in the STD 32 brochure (Appendix D), or the complete STD 32 specification.

STD 32 Connector Specifications:

connector Specification	ns:
Contact type	Cantilever, hemispherical beam
Nickel underplating	100% pure Ni, electrolytically plated per QQN 290 Class 1, 50 microinches thick (Ni)
Gold plating	99.0% pure, per NIL G 45204, Type 2, Grade C 30 microinches thick (Au)
Solder lead plating	100 microinches tin/lead (Sn/Pb)
Manufacturer	Viking #S3VT68/5DP12





Battery Life

Average Battery Life of Ziatech Board-Level Products

Ziatech offers battery backup on some of its board-level products. The real-time clock/calendars and static RAM chips featured on these boards require batteries for backup power. The average life of the battery on each board has been calculated and is shown in the table below. Battery backup, which causes battery drain, occurs while the system power is off. Therefore, the frequency of battery replacement depends on how

often the battery backup is used. The drain on the battery also depends on the circuitry's current demands. Static RAM chips require the majority of the power on all of Ziatech's battery-backed boards, except the ZT 1488A. Substituting low-power RAM chips for higher power chips, and operating the boards at a lower temperature can greatly increase battery life. Ziatech's five-year warranty does not cover batteries.

PRODUCT	CURRENT DEMAND (WORST CASE)	DEMAND WORST CASE BATTERY LIFE (HOURS)					
		"CT/LT" Only -40° C	0° C	25° C	65° C	"CT" Onl +85° C	
ZT 1488A	30 μAmps	N/A	18,667	23,333	18,667	N/A	
ZT 8801/88CT01 with two 10µA SRAM: with two 50µA SRAM:	21 μAmps 101 μAmps	47,619 9,901	47,619 9,901	39,524 9,208	30,952 8,218	22,857 7,237	
ZT 8802/88CT02 with two 10µA SRAM: with two 50µA SRAM:	21 μAmps 101 μAmps	47,619 9,901	47,619 9,901	39,524 9,208	30,952 8,218		
ZT 8809A/88CT09A with 30µA SRAM: adding one 200µA SRAM: adding one 50µA SRAM:	111 µAmps 311 µAmps 161 µAmps	9,009 3,125 6,211	9,009 3,125 6,211	8,378 3,031 5,900	7,477 2,875 5,404	6,667 2,656 4,969	
ZT 8825/88CT25 with eight 50µA SRAM: with eight 10µA SRAM: with eight 1µA SRAM:	440 μAmps 120 μAmps 48 μAmps	2,273 8,333 20,833	2,273 8,333 20,833	2,204 7,916 18,750	2,091 7,250 16,250	1,932 6,666 13,958	
ZT 8832 with two 10µA SRAM: with two 50µA SRAM:	70 μAmps 150 μAmps	14,286 6,667	14,286 6,667	13,286 6,334	11,857 5,800	10,572 5,334	
ZT 8901/89CT01 with two 10µA SRAM: with two 50µA SRAM:	30 μAmps 110 μAmps	33,333 9,091	33,333 9,091	29,333 8,454	24,666 7,546	20,333 6,727	
ZT 8902/89LT02	5 μAmps	262,800	262,800	262,800	87,600	N/A	
ZT 8911/89LT11	11 μAmps	90,909	90,909	75,454	59,090	N/A	
ZT 8920/89CT20 with eight 50µA SRAM: with eight 10µA SRAM: with eight 1µA SRAM:	440 μAmps 120 μAmps 48 μAmps	2,273 8,333 20,833	2,273 8,333 20,833	2,204 7,916 18,750	2,091 7,250 16,250	1,932 6,666 13,958	
ZT 89CT30 with three 50μA SRAM:	150 μAmps	6,666	6,666	6,333	5,800	5,333	
ZT 8932/89CT32 with two 10µA SRAM: with two 50µA SRAM:	30 μAmps 110 μAmps	33,333 9,091	33,333 9,091	29,333 8,454	24,666 7,546	20,333 6,727	

Note: Batteries must NOT be stored at temperatures greater than 100° Celsius.



Battery Life

Average Battery Life of Zigtech Board-Level Products

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Detailed Cable Descriptions

A Supplement to Ziatech's Technical Data Sheets

Ziatech manufacturers a number of standard cables for connections to STD Bus and other cards. The following cable descriptions provide more detailed information than the brief descriptions in the data sheets.

ZT 90002 40-inch (1m) shielded round IEEE 488 cable. Connects to the 26-pin dual-row header used on several Ziatech boards, has a panel mount female IEEE 488 connector with standoffs on the other end. Recommended for high-speed DMA-type data transfers.

ZT 90003 40-inch (1m) IEEE 488 flat ribbon cable. Connects to the 26-pin dual-row header used on several Ziatech boards, and has a panel mount female IEEE 488 connector with standoffs on the other end.

ZT 90005 82-inch (2m) shielded round IEEE 488 cable. Connects to the 26-pin dual-row header used on several Ziatech IEEE 488 boards, and has a free standing male/female IEEE 488 connector on the other end. Recommended for high-speed DMA-type data transfers.

ZT 90008 13-foot (4m) shielded round IEEE 488 cable. Has free standing stackable male/female IEEE 488 connectors on both ends. Recommended for high-speed DMA-type data transfers.

ZT 90010 14-inch (35cm) IEEE 488 flat ribbon cable. Connects to the 26-pin dual-row header used on several Ziatech IEEE 488 boards, and has a panel mount female IEEE 488 connector with standoffs on the other end.

ZT 90011 RS-232 adapter board with 40-inch (1m) flat ribbon cable. Connects to the 16-pin dual-row headers used on the ZT 8806/07 and ZT 8830 (TTL level) serial ports. Includes RS-232 drivers, DTE/DCE configuration jumpers, and a 25-pin female D-shell connector on the PCB.

ZT 90012 RS-422/449 adapter board with 40-inch (1m) flat ribbon cable. Connects to the 16-pin dual-row headers used on the ZT 8806/07 and ZT 8830

(TTL level) serial ports. Includes RS-422 drivers, locations for termination resistors, DTE/DCE configuration jumpers, and a 37-pin RS-449 female D-shell connector on the PCB.

ZT 90014 40-inch (1m) flat ribbon serial cable. Connects to the 14-pin dual-row headers used for serial ports on several Ziatech single board computers and serial boards, and has a 25-pin panel mount female D-shell connector on the other end.

ZT 90016 6.5-foot (2m) shielded round IEEE 488 cable. Has free standing stackable male/female IEEE 488 connectors on both ends. Recommended for high-speed DMA-type data transfers.

ZT 90021 10-foot (3m) flat 50-pin digital I/O cable, connects to a 50-pin dual-row header on one end, 50-pin card edge on the other end. For interfacing 24-signal line digital I/O ports to I/O mounting racks utilizing 50-pin card edge connectors.

ZT 90022 9.5-inch (24cm) flat 50-pin digital I/O cable, connects to 50-pin dual-row headers on both ends. For short interfaces between 24-signal line digital I/O ports and I/O racks.

ZT 90027 40-inch (1m) flat ribbon serial cable. Connects to the 14-pin dual-row headers used for serial ports on several Ziatech single board computers and serial boards, and has a 25-pin panel mount male D-shell connector on the other end.

ZT 90028 40-inch (1m) flat ribbon printer emulation cable. Connects to 50-pin dual-row header of Ziatech digital I/O cards (ZT 8845, ZT 89CT61, ZT 8872) on one end, and a 25-pin D-shell connector on the other end. With DOS driver support, allows digital I/O port to emulate LPT1 or LPT2 in MS-DOS systems.



ZT 90031 22-inch (26cm) flat ribbon keyboard cable. Connects to 10-pin headers used on Ziatech boards, and has panel mount IBM-compatible DIN keyboard connector on other end.

ZT 90039 3-foot (91cm) flat ribbon printer cable for ZT 8808 or ZT 8809A. Converts ZT 8808/09A printer port 20-pin header into IBM compatible 25-pin female D-shell connector.

ZT 90063 8.25-inch (21cm) flat ribbon frontplane interrupt cable. Has one 26-pin connector and four 10-pin connectors. For routing interrupt signals across the front of I/O, peripheral and single board computers.

ZT 90066 11-inch (28cm) flat ribbon IEEE 488 cable. Connects to the 24-pin dual-row header of the zSBX 20, and has a female IEEE 488 connector on a PC back panel mounting bracket on the other end.

ZT 90068 40-inch (1m) flat digital I/O cable, converts the 26-pin dual-row header on the ZT 8832 and ZT 89CT30 to an Opto rack-compatible 50-pin card edge connector. Has additional 50-pin header for accommodating other digital I/O cables.

ZT 90069 39-inch (1m) shielded round serial cable. Connects to the 3-pin serial port connectors found on the ZT 8801, ZT 8802, ZT 8832 and ZT 8901 single board computers, and has a 25-pin female D-shell connector on the other end.

ZT 90071 24-volt AC wall transformer with cable and 2-pin female connector for interface to Ziatech single board computers with AC power-fail detection circuit.

ZT 90072 10-foot (3m) flat 50-pin digital I/O cable, connects to 50-pin dual-row headers on both ends. For interfacing 24-signal line digital I/O ports to I/O mounting racks utilizing 50-pin dual-row headers.

ZT 90076 32-inch (81cm) flat ribbon keyboard cable. Connects to 10-pin headers used on Ziatech boards, and has desktop style IBM-compatible DIN keyboard connector on other end.

ZT 90077 20-inch (51cm) flat ribbon dual floppy disk interface cable. Connects to the 34-pin dual-row header of the ZT 8950 floppy controller, and has a 34-pin female socket for 3.5-inch drive and a 34-pin card edge connector for 5.25-inch drives with 5.5-inch (14.0cm) cable length in between (overall length is more than 25.5 inches [64.8cm]).

ZT 90089 40-inch (1m) flat 56-pin digital I/O cable, connects to 56-pin dual-row headers on both ends. For interfacing 48-signal line I/O ports on the ZT 8801 and ZT 8901 single board computers to the ZT 2223 and ZT 2226.

ZT 90090 40-inch (1m) flat 26-pin digital I/O cable, connects to 26-pin dual-row headers on both ends. For connecting the 24-signal line I/O ports of the ZT 8832 and ZT 89CT30 to the ZT 2225.

ZT 90099 40-inch (1m) shielded round RS-232 DCE serial cable. Connects to the 5-pin serial connector on the ZT 89CT30, and has a 25-pin female D-shell connector on the other end.

ZT 90100 6.3-inch (16 cm) flat ribbon frontplane interrupt cable. Has one 16-pin connector and four 10-pin connectors. For routing interrupt signals across the front of I/O, peripheral and single board computers.

ZT 90104 13-inch (33 cm) flat cable, 10-pin header connectors on both ends

ZT 90105 9-inch (23cm) flat ribbon frontplane interrupt cable. Has one 20-pin connector, six 16-pin connectors, and one 10-pin connector. For routing interrupt signals across the front of ZT 8901 processors and a peripheral or I/O card in STD 32 STAR SYSTEMs.

ZT 90106 2-foot (61cm) LONWORKS cable with RJ-45 connectors on both ends.

ZT 90107 7-foot (2.1 m) LONWORKS cable with RJ-45 connectors on both ends.

ZT 90109 8-inch (20 cm) fiat RS-232 serial cable. Connects 14-pin connectors used for RS-232 serial ports on many Ziatech STD cards to the ZT 2592 RS-485 Optical Isolation plate, and has 14-pin dual-row sockets on both ends.

ZT 90136 40-inch (1m) flat ribbon serial cable. Connects to the 10-pin dual-row headers used for RS-232 serial ports on the ZT 8902 and ZT 8911, and has a 9-pin male D-shell connector on the other end.

ZT 90137 2-foot (61cm) flat 50-pin digital I/O cable, connects to 50-pin dual-row headers on both ends. For connecting 24-signal line digital I/O ports to I/O mounting racks and for the daisy-chain interface between ZT 2226 racks.

ZT 90143 10-foot (3m) shielded video data, touchscreen data and power cable

ZT 90147 12-foot (30cm) card cage power cable assembly

ZT 90156 8-inch (20cm) printer interface cable, 56-pin connector to 25-pin female D-shell

ZT 90157 3-foot (91cm) flat printer cable, 20-pin header to 25-pin female D-shell

ZT 90166 10-inch (25cm) video/keyboard cable, zVID2/ZT 8982 to panel mount connectors

ZT 90167 10-inch (25cm) video/keyboard cable, zVID2/ZT 8982 to desktop-style connectors

ZT 90182 10-inch (25cm) 40-pin header to four (10-pin) headers

ZT 90183 10-inch (25cm) 40-pin header to four (9-pin) male D-shell connectors

FAX (805) 541-5088 • Telephone (805) 541-0488





5+5 Warranty

For Ziatech Board- and System-Level Computer Products

FIVE-YEAR LIMITED WARRANTY

Products manufactured by Ziatech Corporation are covered from the date of purchase by a five-year warranty against defects in materials, workmanship, and published specifications applicable to the date of manufacture. During the warranty period, Ziatech will repair or replace, solely at its option, defective units provided they are returned at customer expense to an authorized Ziatech repair facility. Products which have been subjected to misuse, abuse, neglect, alteration, or unauthorized repair, determined at the sole discretion of Ziatech, whether by accident or otherwise, are excluded from warranty. The warranty on fans and disk drives is limited to two years, the warranty on software is limited to one year, and the warranty on flat panel displays is limited to nine months from date of purchase. Other products and accessories not manufactured by Ziatech are limited to the warranty provided by the original manufacturer. Consumable items (fuses, disk media, batteries,* etc.) are not covered by this warranty.

Ziatech may offer, where applicable and available, replacement products; otherwise, repairs requiring components, assemblies, and other purchased materials may be limited by market availability.

Ziatech assumes no liability resulting from changes to government regulations affecting use of materials, equipment, safety, and methods of repair. Ziatech may, at its discretion, offer replacement products.

The above warranty is in lieu of any other warranty, whether expressed, implied, or statutory, including, but not limited to, any warranty for fitness of purpose, merchantability, or freedom from infringement or the like, and any warranty otherwise arising out of any proposal, specifications, or sample. Ziatech neither assumes nor authorizes any person to assume for it any other liability. The liability of Ziatech under this warranty agreement is limited to a refund of the purchase price. In no event shall Ziatech be liable for loss of profits, use, incidental, consequential, or other damage, under this agreement.

SPECIAL EXTENDED WARRANTY OPTION

In addition to the standard five-year warranty, Ziatech offers, for a nominal fee, an extended period of warranty up to five extra years. This extended warranty period provides similar coverage and conditions as stated above in the five-year limited warranty agreement.

LIFE SUPPORT POLICY

Ziatech products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Ziatech Corporation. As used herein:

- 1. Life support devices or systems are devices or systems which support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- 2. A critical component is any component of a life support device or system whose failure to perform can be expected to cause the failure of the life support device or system, affect its safety, or limit its effectiveness.





S-5 Warranty

For Zigtech Board- and System-Level Computer Products

YTHARRAW CEITHILL SARVANIE

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garechti ay oner, who a application of the purchased meterials may be limited by market availability.

Zistech assumes no liability resulting from changes to government regulations affecting use or materials, southment, safety, and methods of repair. Zistech may, at its discretion, offer replacement products.

The above warranty is in lieu of any other warranty, whether expressed, implied, or freedom from including, but not limited to, any warranty for fitness of purpose, merchantability, or freedom from infringement or the like, and any warranty otherwise arising out of any proposal, specifications, or sample. Zietech neither assumes nor authorizes any person to assume for it any other liability. The sample. Zietech under this warranty agreement is limited to a retund of the purchase price, in no event shall Zietech be liable for loss of profits, use, incidental, consequental, or other damage, under this agreement.

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2. A critical component is any component of a life support device or system whose failure to perform can be expected to cause the failure of the life support device or system, effect its sately, or limit its effectiveness.



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